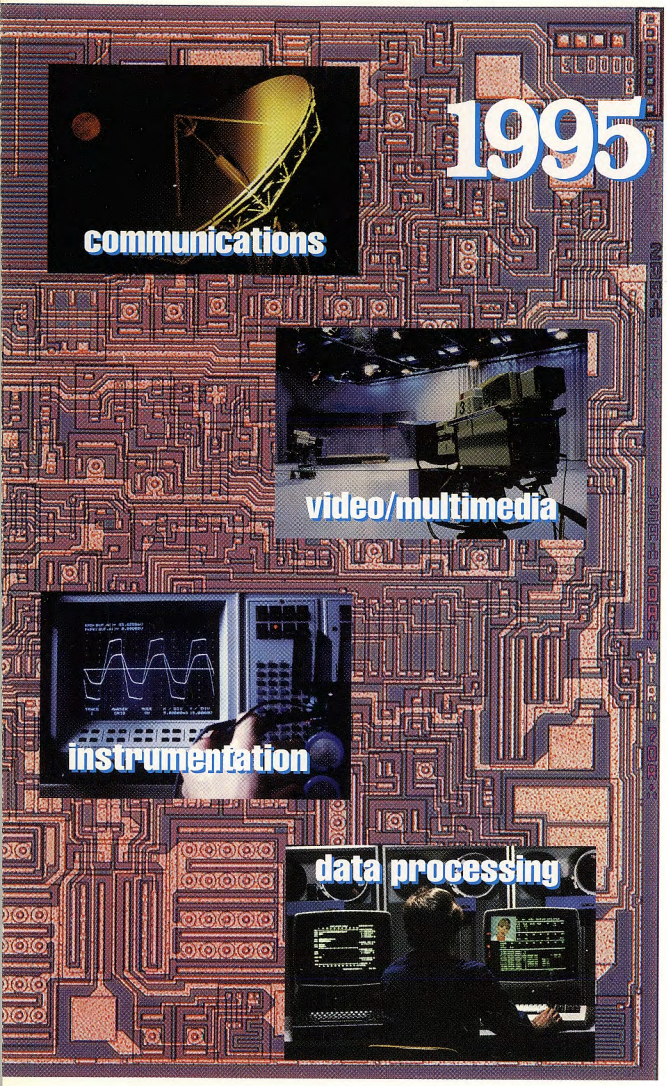

1995 New Products Supplement

High Performance Analog Integrated Circuits

élantec

A SUPPLEMENT TO THE 1994 FULL LINE DATA BOOK

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

New Products - 1995

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WARNING—Life Support Applications Policy

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General Disclaimer

Specifications contained in this databook are current as of the publication date shown. Each datasheet is a controlled document. Current revisions, if any, to these specifications are maintained at the factory and are available upon request. Elantec, Inc. reserves the right to make changes in the circuitry or specifications contained herein at any time without notice. Elantec, Inc. assumes no responsibility for the use of any circuits described herein and makes no representations that they are free from patent infringement. Products contained in this databook may be covered by one or more of the following patents. Additional patents are pending. For specific information, refer to the individual datasheets:

US Patent Numbers: 4,746,877 • 4,827,223 • 4,837,523 • 4,833,424 • 4,935,704 • 4,910,477 • 5,128,564 • 4,878,034 • 4,963,802 • 5,179,355 • 5,321,371 • 5,334,883 • 5,341,047 • 5,352,987 • 5,352,389 • 5,351,012 • 5,374,898 • 5,389,840

UK Patent Numbers: 2217135 • 2217134

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Full Product Line Index

The following is a complete list of devices currently available from Elantec.

Full Product Line Index

Full Product Line Index

Capabilities

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Mission

"To be a leading supplier of high performance analog solutions for the video/multimedia, data processing, communications and instrumentation markets."

Elantec, Inc., founded in 1983 and located in Milpitas, California, is a fully integrated semiconductor company focused on providing high performance analog intensive functions for growing markets. These markets are driven by the rapid advances in digital technology which in turn creates a demand for high speed and low power analog functions to complete the overall system. Elantec serves these markets with standard and application specific standard products (ASSP) using advanced bipolar and CMOS technologies.

Our strategy is to provide effective and timely solutions through market knowledge, advanced technologies, design expertise and close customer interface.

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Market	Typical Applications	Representative Elantec Products
Video/Multimedia	Displays	Cathode Ray Tube Drivers
	Personal Computer Add-on Boards	Video ASSPs, Faders, DC Restoration
	Set Top Converters	Video ASSPs, Faders, Amplifiers
	Special Effects Generators	Video ASSPs, Multipliers, PLL, Faders
	Studio Equipment	Video Amplifiers, Faders, Multiplexers
	Switchers/Routers	Multiplexers, Power Amplifiers
	Video Distribution Networks	High Power Amplifiers
	Workstations	Video Timing Circuits
	Video Cameras	CCD Drivers, Amplifiers
Instrumentation	Analyzers	High Speed Amplifiers, Comparators
	Automatic Testers	Pin Drivers/Receivers
	Measuring Instruments	High Speed Amplifiers, Comparators
	Medical Instrumentation	Mosfet Drivers
	Recorders	High Speed Amplifiers
	Portable Instrumentation	Low Power Amplifiers
Data Processing	Copiers	Video Amplifiers
	Document Scanners	Video Amplifiers
	Magnetic Disk Drives	Servo Motor Drivers
	Optical Disk Drives	High Speed Amplifiers, Laser Drivers
	Personal Computers	Video ASSPs, DC to DC Converters, System Managers
	Power Supplies	Mosfet Drivers
Communications	Fax Machines	High Speed Amplifiers
	Modems	High Speed Amplifiers
	Transmission Line Drivers	Power Amplifiers
	Transmission Line Receivers	High Speed Amplifiers, Transceivers
	Networks	Twisted Pair Drivers

Capabilities

Markets and Products

Elantec has over 150 products in its catalog to serve the target markets. Many of the standard products, such as amplifiers, are used in multiple markets while the application specific products are targeted for specific applications and group of customers.

The preceding table outlines the ranges of markets, applications and products which the company serves.

Technology

The company uses a variety of technologies for its products. In particular, Elantec has focused on developing an advanced complementary bipolar technology using dielectric isolation and silicon on insulator techniques for its high speed circuits. Complementary bipolar technology allows high speed analog signals to be processed efficiently in either signal polarity which greatly simplifies design methodology and substantially improves power dissipation. Because of the dielectric isolation technique, Elantec's complementary process has the additional inherent advantages of low capacitance, low crosstalk, no latch-up, high voltage, high temperature operation and improved speed.

For low power, analog switching and mixed signal applications, Elantec uses a variety of CMOS technologies ranging from 1.2μ to 2.0μ gate lengths.

Advances in technology together with outstanding design expertise will continue to provide superior solutions for Elantec's target markets.

Bipolar Technology Capabilities

Elantec utilizes a combination of internal capability and external world class bipolar foundries. We match the appropriate technology to best serve the requirements of our customers' demanding design problems. Elantec currently uses the following bipolar technologies:

- Standard Linear J.I. (Junction Isolation)
  40V, NPN Ft = 600 MHz, PNP Ft = 5 MHz
- High Voltage, Oxide Isolated—Fully Complementary Bipolar for high performance, high voltage circuit applications
  40V, NPN Ft = 800 MHz,
  PNP Ft = 800 MHz
  25V, NPN Ft = 1.5 GHz, PNP Ft = 1.5 GHz
- Low Voltage, Fast, Complementary Bipolar
  10V, NPN Ft = 4.0 GHz, PNP Ft = 3.0 GHz

CMOS Technology

Elantec uses a variety of CMOS technologies ranging from gate length of 1.2μ to 2.0μ. Each version is available in single or dual poly and single or dual metal and an epitaxial substrate to provide a solid ground plane.

The processes are suitable for analog, mixed signal and high speed applications with supply voltages ranging from 4.5V to 15V.

Design Capabilities

Elantec's engineering team has many years of experience defining, designing, manufacturing and testing analog and mixed signal devices, utilizing both Bipolar and CMOS technologies.

Functions we currently supply are: current and voltage feedback amplifiers, multipliers, video specific standard products, pin drivers and receivers, C.R.T. drivers, buffers, servo electronics, MOSFET and IGBT drivers, DC converters, instrumentation amplifiers, and precision amplifiers. Elantec also designs customer specific products where the unique technical and volume requirements of the system make this more desirable. Customers can discuss their challenging system requirements with out talented technical team of field and factory applications engineers.

Elantec provides each circuit designer and layout artist with the most up to date Sun workstations at their desk. All stations are networked together to a Sun server. Extra "computing engines" are also available on the network. The Sun network is connected to the corporate network to facilitate corporate wide communication. Elantec uses Cadence and MicroSim design software and Cadence IC layout software and design verification tools. The design tool suite can use the computing capability of the entire Sun network to allow extensive simulations covering the variations of the wafer fabrication process, based on data derived from capability studies.

Test Automation/Equipment Capability

Elantec utilizes the LTX Model 77 test system with TS80 and TS88 test stations for primarily DC testing operational amplifiers, buffers, comparators, and other linear devices. In general, custom socket adaptors have been developed for unique devices such as current feedback amplifiers, DC restored video amplifiers, sync separators and disk drive servo motors. A wide range of automatic handlers allow high speed, room temperature and extended range temperature testing of Dual in Line (DIP), Small Outline (SO) packages, metal cans such as TO3, TO99 and TO8.

The DC testing capability of the LTX Model 77 is augmented with rack mounted AC test systems which are integrated into the LTX. The time domain systems, which are used to measure very fast rise times, slew rates and propagation delays, are comprised of programmable pulse generators and 1 GHz digitizing oscilloscopes and are capable of measurements under 10 pS. The frequency domain systems which are used to measure bandwidth, differential phase, differential gain, phase linearity, gain flatness, distortion, etc. are composed of programmable signal sources and network analyzers and are capable of measurements to 500 MHz.

Elantec ensures the accuracy of all critical test parameters by testing using alternative devices to the LTX system.

Quality and Service

Elantec's commitment to quality begins with the product definition, design and characterization and continues through the complete process. We are a fully integrated semiconductor company with its own complete manufacturing facility, including wafer fabrication, assembly and test. Elantec continually improves its manufacturing and quality methods using SPC, Total Quality Management and ISO 9000 compatible techniques.

Superior product performance and quality are augmented by a commitment to customer service and technical support in order to make our customers successful. Technical customer support is provided through corporate applications, field applications engineers and technical seminars. Sales support is provided through the Elantec field sales force which directs a worldwide network of technical representatives and distributors.

Packaging Capability

Elantec supports most industry standard package types. Currently we are manufacturing standard products in the packages shown below:

Additionally, we can supply special packages upon request for volume and special applications. Contact Elantec's marketing department for availability.

P-DIP, SO	P-DIP Packages—8, 14, 16-Pin		SO Packages—8, 14, 16, 20, 28-Lead	
Power Packages	TO-220—5 Lead	TO-3—8 Lead	TO-5—10 Lead	TO-8—12 Lead

Amplifiers

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2165C

30 MHz Precision Current Mode Feedback Amplifier

Features

- 35 MΩ transimpedance
- 30 MHz −3dB bandwidth (A_V = +1)
- 30 MHz −3dB bandwidth (A_V = +2)
- 1 mV input offset voltage
- 2 μA negative input bias current
- 86 dB common mode rejection ratio
- 92 dB power supply rejection ratio
- Low supply current, 4 mA
- Wide supply range, ±4.5V to ±16.5V
- 55 mA output peak current
- High capacitive load toleration
- Low cost
- Input/output compliance to ±2V of supplies
- 500 V/μs slew rate
- 65 ns settling to 0.1%
- 110 ns settling to 0.01%
- −68 dBc distortion @ 1 MHz

Applications

- Instrumentation circuitry
- Current to voltage convertors
- DAC/ADC output amplifier/ buffer
- Cable drivers
- Low distortion communications
- Medical imaging
- CCD imaging
- Infrared image enhancement

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2165CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2165CS	−40°C to +85°C	8-Lead SOIC	MDP0027

General Description

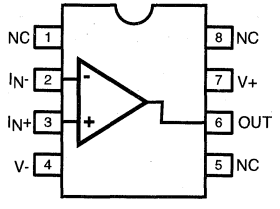
The EL2165C is a low offset, high transimpedance current mode feedback amplifier with a −3 dB bandwidth of 30 MHz at a gain of +2. Built on Elantec's proprietary monolithic complementary bipolar process, this amplifier uses current feedback to achieve more bandwidth at a given gain than conventional voltage feedback amplifiers.

The high 35 MΩ transimpedance gain and low input referred offset of the EL2165 will also bring the final settled output much closer to its ideal value than is possible with earlier CMF designs.

In addition, the common-mode and power supply rejection have been greatly improved over earlier current mode feedback amplifiers and the input offset voltage and current have been trimmed to rival that of good conventional voltage feedback amplifiers. The part has a typical slew rate of 500 V/μs and a 0.01% settling time of less than 110ns in inverting mode. At a gain of +2 and an output signal level of 2 Vp-p, the total harmonic distortion is only −68 dB at 1 MHz.

The amplifier can operate on any supply from 9V (±4.5V) to 33V (±16.5V), yet consumes only 4 mA at any supply voltage. Using the industry standard 8-pin pinout, the EL2165C is available in both P-DIP and SO packages.

Connection Diagram



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EL2165C

30 MHz Precision Current Mode Feedback Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_S+ and V_S-	+33V	Operating Junction Temperature	
Voltage between I_N+ and I_N-	±6V	Plastic Package	150°
Current into I_N+ and I_N-	4 mA	Storage Temperature Range	−65°C to +150°C
Operating Ambient Temperature Range	See Curves		

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

(V_S = ±15V, R_L = 500Ω, T_A = 25°C unless otherwise specified)

Parameter	Description	Conditions	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage		25°C		1	3	I	mV
TC V_{OS}	Average Offset Voltage Drift (Note 1)		Full		2		V	µV/°C
$I_{IN}+$	+Input Current		25°C		−1	±6	I	µA
$I_{IN}-$	−Input Current		25°C		±2	±7	I	µA
CMRR	Common Mode Rejection Ratio (Note 2)		25°C	79	86		I	dB
ICMR−	−Input Current Common Mode Rejection (Note 2)		25°C		23	100	I	nA/V
PSRR	Power Supply Rejection Ratio (Note 3)		25°C	84	93		I	dB
IPSR−	−Input Current Power Supply Rejection (Note 3)		25°C		75	225	I	nA/V
R_{OL}	Transimpedance (Note 4)	V_S = ±15V R_L = 500Ω	25°C		35		V	MΩ
		V_S = ±5V R_L = 150Ω	25°C	5.0	12.4		I	MΩ
$R_{IN}+$	+Input Resistance			18	36		I	MΩ
$C_{IN}+$	+Input Capacitance		25°C		2.5		V	pF
CMIR	Common Mode Input Range (Note 2)	V_S = ±15V	25°C	±12	±12.5		I	V
		V_S = ±5V	25°C	±2.0	±2.5		I	V

Open Loop DC Electrical Characteristics

(V_S = ±15V, R_L = 500Ω, T_A = 25°C unless otherwise specified) — Contd.

Parameter	Description	Conditions	Temp	Min	Typ	Max	Test Level	Units
V_O	Output Voltage Swing	R_L = 500Ω V_S = ±15V	25°C	±12.3	±13		I	V
		R_L = 150Ω V_S = ±15V	25°C		±11.6		V	V
		R_L = 150Ω V_S = ±5V	25°C	±2.7	±3.0		I	V
I_{SC}	Output Short Circuit Current (Note 4 and 5)		25°C	55	80		I	mA
I_S	Supply Current		25°C		4.0	5.25	I	mA

EL2165C
30 MHz Precision Current Mode Feedback Amplifier

Closed Loop AC Electrical Characteristics

(V_S = ±15V, A_V = +2, R_F = 1KΩ, R_L = 500Ω, T_A = 25°C unless otherwise specified)

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
BW	−3dB (Note 8)	V_S = ±15V, A_V = +2, R_F = 1K		30		V	MHz
		V_S = ±15V, A_V = +1, R_F = 1.3K		28		V	MHz
		V_S = ±5V, A_V = +2, R_F = 1K		30		V	MHz
		V_S = ±5V, A_V = +1, R_F = 1.3K		30		V	MHz
SR	Slew Rate (Notes 6 and 8)	R_L = 500Ω	250	500		I	V/μS
		R_F = 1 KΩ, R_G = 110Ω R_L = 400Ω		500		V	V/μS
t_r, t_f	Rise Time, Fall Time (Note 8)	V_{OUT} = ±500 mV		14		V	nS
t_{pd}	Propagation Delay (Note 8)			12		V	nS
O_S	Overshoot (Note 8)	V_{OUT} = ±500 mV		2		V	%
t_s	0.1% Settling Time (Note 8)	V_{OUT} = ±10V, A_V = 1		120		V	nS
		V_{OUT} = ±10V, A_V = −1		65			
		V_{OUT} = ±10V, A_V = 2		100			
t_s	0.01% Settling Time (Note 8)	V_{OUT} = ±10V, A_V = 1		750		V	nS
		V_{OUT} = ±10V, A_V = −1		110			
		V_{OUT} = ±10V, A_V = 2		500			

Note 1: Measured from T_{MIN} to T_{MAX}

Note 2: V_{CM} = ±12V for V_S = ±15V and T_A = 25°C
V_{CM} = ±2V for V_S = ±5V and T_A = 25°C
CMIR is guaranteed by the part passing CMRR at the rated common-mode swing.

Note 3: The supplies are moved from ±4.5V to ±15V.

Note 4: V_{OUT} = ±10V for V_S = ±15V, and V_{OUT} = ±2V for V_S = ±5V.

Note 5: A heat sink is required to keep junction temperature below absolute maximum when an output is shorted.

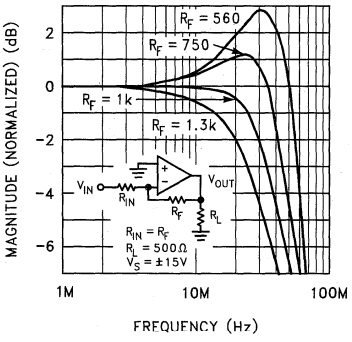
Note 6: Slew Rate is with V_{OUT} from +10V to −10V and measured at the 25% and 75% points.

Note 7: DC offset from −0.714V through +0.714V, AC amplitude 286 mV_{p-p}, f = 3.58 MHz.

Note 8: All AC tests are performed on a "warmed up" part, except for Slew Rate, which is pulse tested.

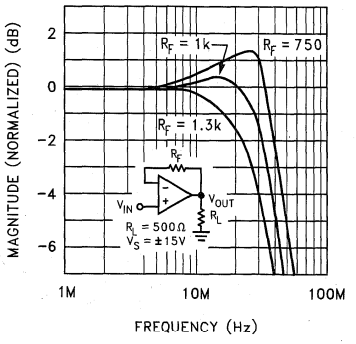
Typical Performance Curves

Frequency Response for $A_V = -1$ and for Various R_F Values



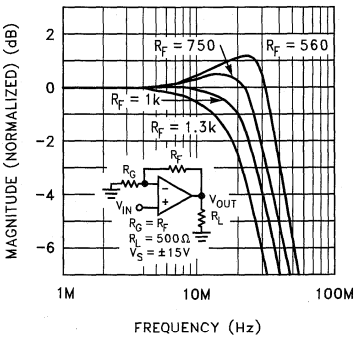
2165-2

Frequency Response for $A_V = +1$ and for Various R_F Values



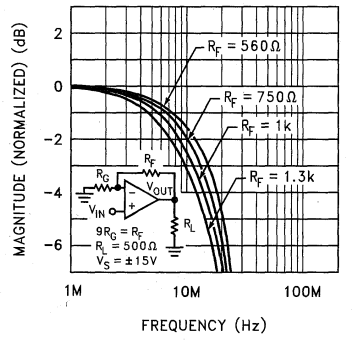
2165-3

Frequency Response for $A_V = +2$ and for Various R_F Values



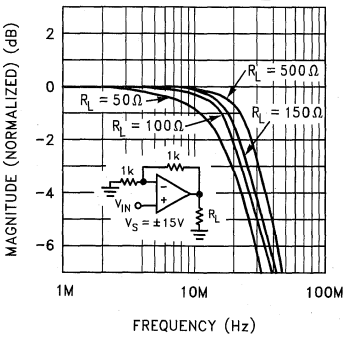
2165-4

Frequency Response for $A_V = +10$ and for Various R_F Values



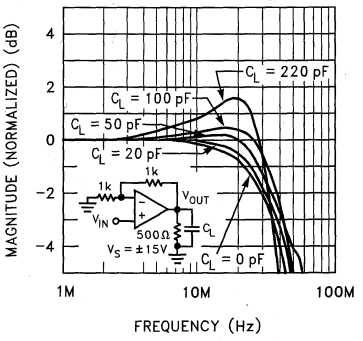
2165-5

Frequency Response for Various Values of R_L



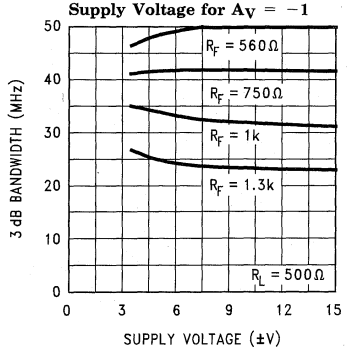
2165-6

Frequency Response for Various Values of C_L



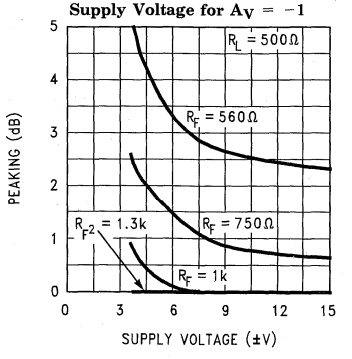
2165-7

3 dB Bandwidth vs Supply Voltage for $A_V = -1$



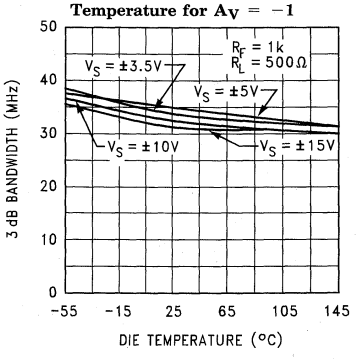
2165-8

Peaking vs Supply Voltage for $A_V = -1$



2165-9

3 dB Bandwidth vs Temperature for $A_V = -1$

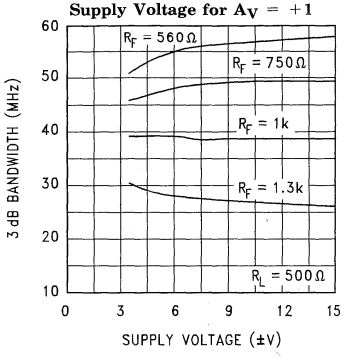


2165-10

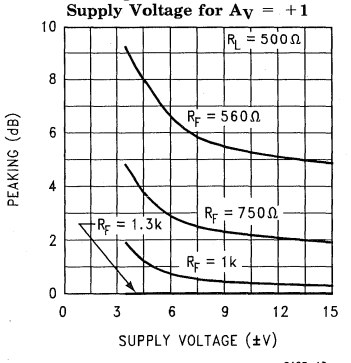
EL2165C
30 MHz Precision Current Mode Feedback Amplifier

Typical Performance Curves — Contd.

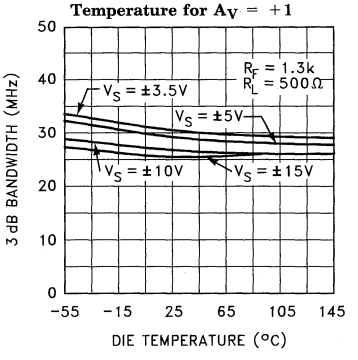
3 dB Bandwidth vs Supply Voltage for A_V = +1



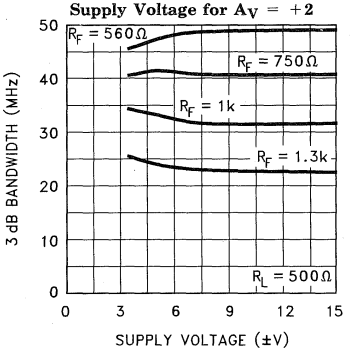
Peaking vs Supply Voltage for A_V = +1



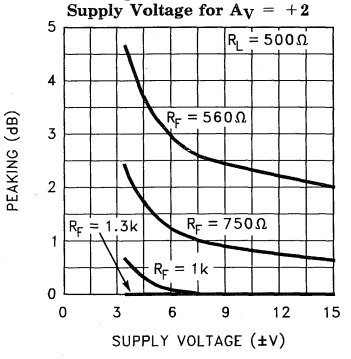
3 dB Bandwidth vs Temperature for A_V = +1



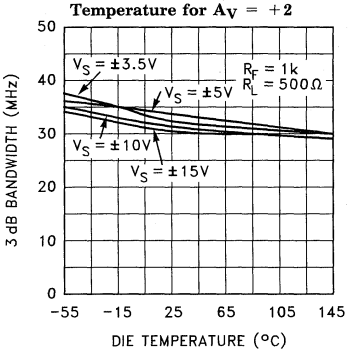
3 dB Bandwidth vs Supply Voltage for A_V = +2



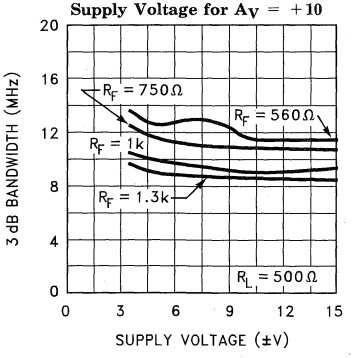
Peaking vs Supply Voltage for A_V = +2



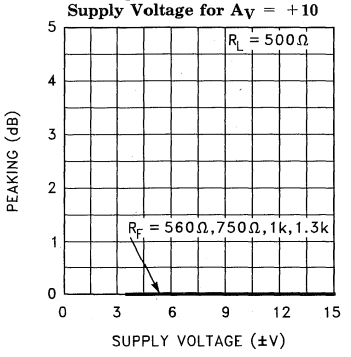
3 dB Bandwidth vs Temperature for A_V = +2



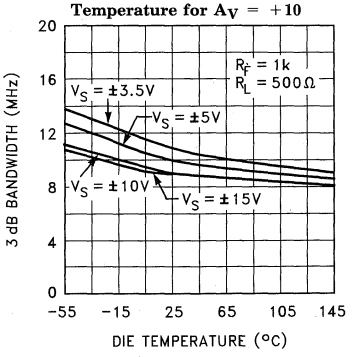
3 dB Bandwidth vs Supply Voltage for A_V = +10



Peaking vs Supply Voltage for A_V = +10

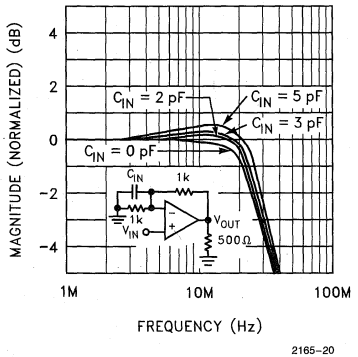


3 dB Bandwidth vs Temperature for A_V = +10



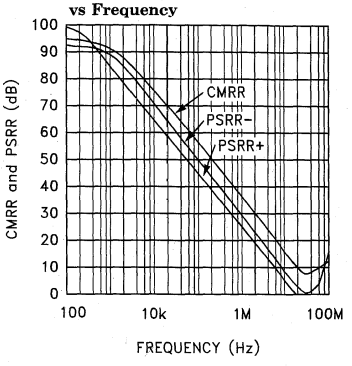
Typical Performance Curves — Contd.

Frequency Response for Various Values of C_{IN}



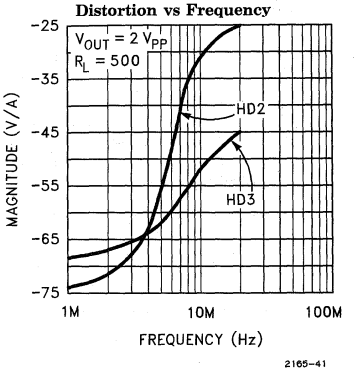
2165-20

PSRR and CMRR vs Frequency



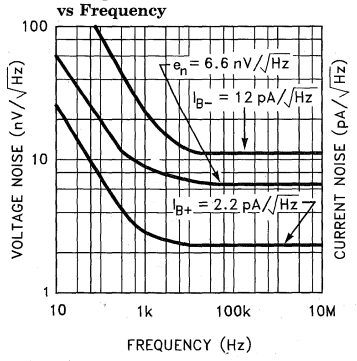
2165-21

Second and Third Hormonic Distortion vs Frequency



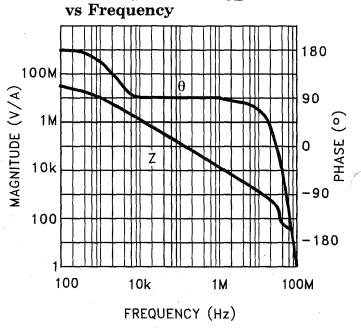
2165-41

Voltage and Current Noise vs Frequency



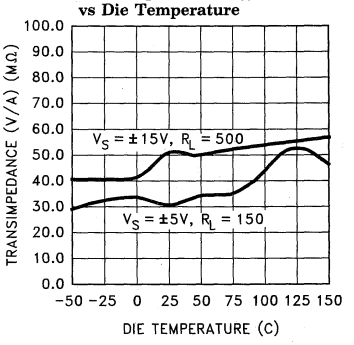
2165-22

Transimpedance (R_{OL}) vs Frequency



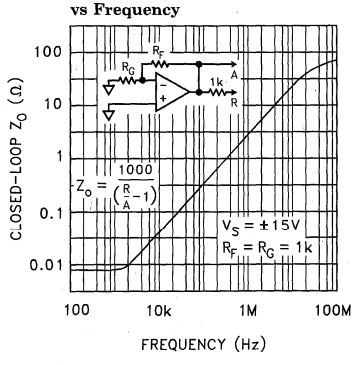
2165-23

Transimpedance (R_{OL}) vs Die Temperature



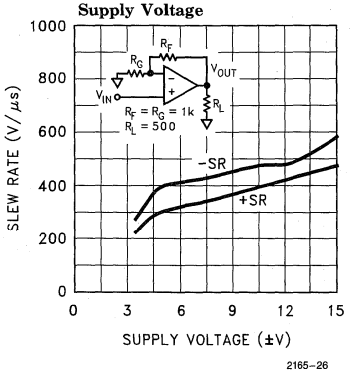
2165-24

Closed-Loop Output Impedance vs Frequency



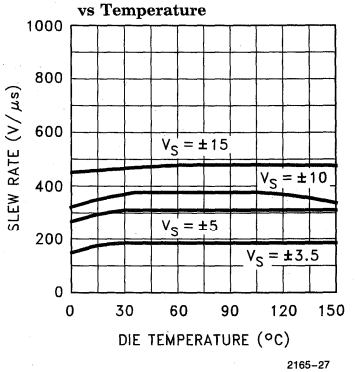
2165-25

Slew Rate vs Supply Voltage



2165-26

Slew Rate vs Temperature



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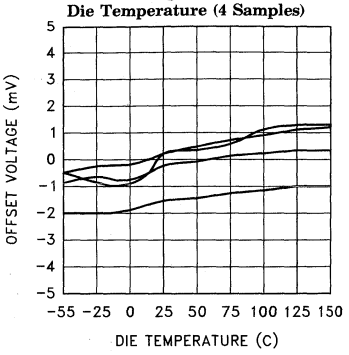
EL2165C
30 MHz Precision Current Mode Feedback Amplifier

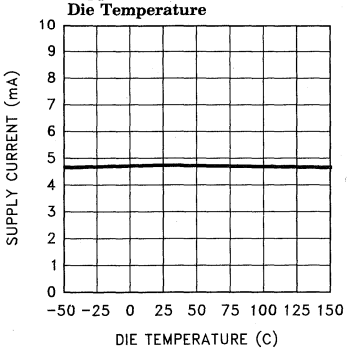
Typical Performance Curves — Contd.

Offset Voltage vs Die Temperature (4 Samples)



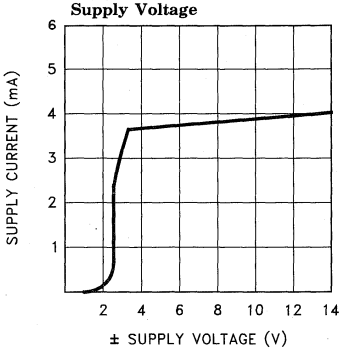
2165-28

Supply Current vs Die Temperature



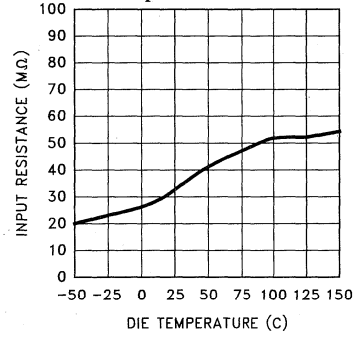
2165-29

Supply Current vs Supply Voltage



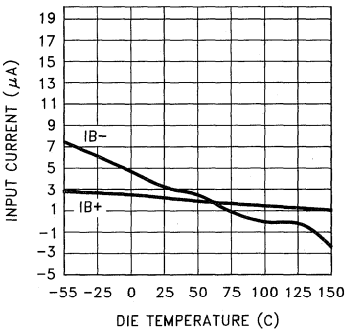
2165-30

Input Resistance vs Die Temperature



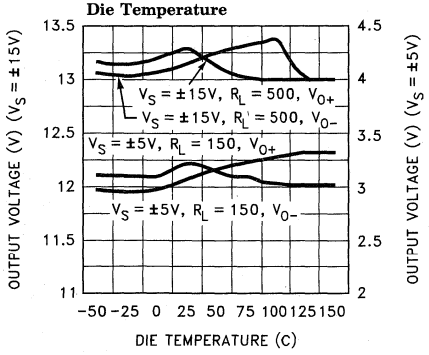
2165-31

Input Current vs Die Temperature



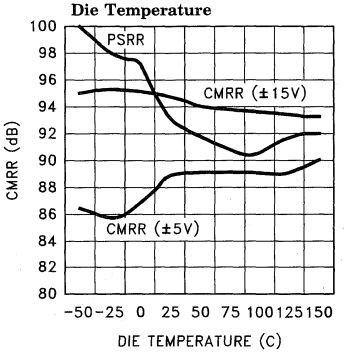
2165-32

Output Voltage Swing vs Die Temperature



2165-33

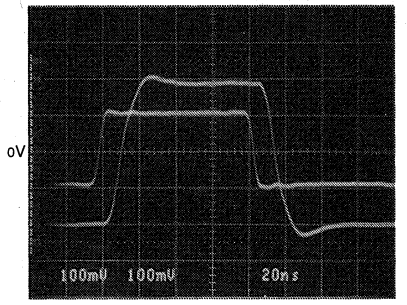
PSRR and CMRR vs Die Temperature



2165-34

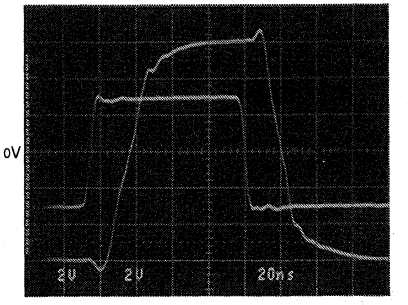
Typical Performance Curves — Contd.

Small Signal Pulse Response



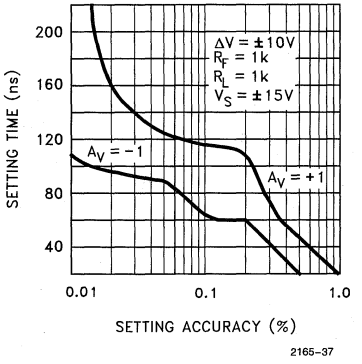
2165-35

Large Signal Pulse Response



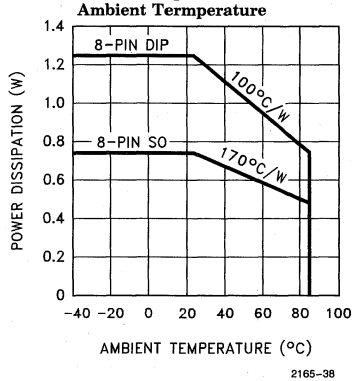
2165-36

Settling Time vs Settling Accuracy



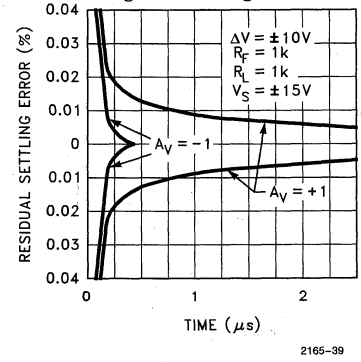
2165-37

8-Pin Package Power Dissipation vs Ambient Termperature



2165-38

Long Term Settling Error



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EL2165C
30 MHz Precision Current Mode Feedback Amplifier

Applications Information

Product Description

The EL2165C is a single current mode feedack amplifier that offers wide bandwidth, high gain, low distortion and exceptional DC specifications for a CMF type amplifier at moderate supply current. It is built using Elantec's proprietary complimentary bipolar process and is offered in the industry standard pin-out. Due to the current feedback architecture, the EL2165 closed loop 3 dB bandwidth is dependent on the feedback resistor. First the desired bandwidth is selected by choosing the feedback resistor, R_F, and then the gain is set by picking the gain set resistor, R_G. The curves at the beginning of the Typical Performance Curves section show the effect of varying both R_F and R_G. The 3 dB bandwidth is significantly less dependent on supply voltage than earlier CMF amplifiers where increasing junction capacitances with decreasing supply voltage caused a much larger reduction in bandwidth. To compensate for the remaining effect, smaller values of feedback resistor can be used at lower supply voltages.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible, below $\frac{1}{4}''$. The power supply pins must be well bypassed to ensure stability. A 1.0 μF tantalum capacitor in parallel with a 0.01 μF ceramic capacitor is adequate for each supply pin.

For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input (see Capacitance at the Inverting Input section). This implies keeping the ground plane away from this pin. Carbon resistors are acceptable, while wire-wound resistors should not be used because of their parasitic inductance. Similarly, capacitors should have low inductance for best performance. Use of sockets, particularly for SO packages, should be avoided. Sockets have parasitic inductance and capacitance which will cause peaking and overshoot.

Capacitance at the Inverting Input

Due to the topology of the conventional current feedback amplifiers, stray capacitance at the inverting input will affect their AC and transient performance when operating in the non-inverting configuration. This may cause design, development and production difficulties. The EL2165 has been designed in such a way as to largely ignore such strays. The characteristic curves of gain vs. frequency with varying values of C_{IN-} illustrate this effect which produces only a slight increase in peaking with C_{IN-} values up to 5 pF with almost no change in 3 dB bandwidth.

In the inverting gain mode, added capacitance at the inverting input has almost no effect at all. This is because the inverting input is now a virtual ground and the stray capacitance is not therefore "seen" by the amplifier.

Feedback Resistors Values

The EL2165 has been designed and specified with $R_F = 1\ K\Omega$ for $A_V = +2$. This value of feedback resistor yields an extremely flat frequency response with little or no peaking out to 30 MHz. As is the case with all CMF amplifiers, wider bandwidth, at the expense of peaking, can be obtained by reducing the value of the feedback resistor. Inversely, larger values of feedback resistor will cause rolloff to occur at lower frequency. For example, the 3 dB bandwidth of the EL2165 connected for $A_V = -1$ and $R_F = 1\ K\Omega$ is about 34 MHz. If R_F is reduced to 750Ω the bandwidth increases to 48 MHz. See the curves in the Typical Performance Curves section which show 3 dB bandwidth and peaking vs. frequency for various feedback resistors, supply voltages and temperature.

Bandwidth vs. Temperature

The supply current of many amplifiers, and consequently their 3 dB bandwidths, drop off significantly with increasing temperature. The EL2165 was designed to have nearly constant supply current over temperature resulting in a part with much less bandwidth vs. temperature sensitivity. With $V_S = \pm 15V$ and $A_V = +2$, the bandwidth only varies from 38 MHz to 29 MHz over the entire die temperature range of $0°C < T < 150°C$.

Applications Information — Contd.

Supply Voltage Range

The EL2165 has been designed to operate comfortably with supply voltages from ±5V to ±15V. AC characterization has been conducted down to supply voltages of ±3.5V. However, this low value will not allow the part to power up and function properly at the lowest portion of the part's operating temperature range (−40°C to +85°C). In general, bandwidth, slew rate and video characteristics will tend to improve with increasing supply voltages.

If a single supply is desired, values from +9V to +30V can be used as long as the input common mode range is not exceeded. When using a single supply, be sure to either 1) DC bias the inputs at an appropriate common mode voltage and DC couple the signal, or 2) ensure the driving a signal is within the input common mode range of the EL2165.

Settling Characteristics

The EL2165 offers superb settling characteristics to 0.1%, typically 65 ns operating in inverting mode. The inverting 0.01% settling time is about 110 ns. The EL2165 is not slew rate limited, therefore a step size up to ±10V gives the same settling time. The high 35 MΩ transimpedance gain and low input referred offsets of the EL2165 will also bring the final settled output much closer to its ideal value than is possible with earlier CMF designs.

The noninverting (A_V = +1) 0.1% settling time is about 120 ns. As can be seen from the Long Term Settling Error graph, for A_V = +1, there is approximately a 0.04% residual which tails away to 0.01% in about 750 ns. This is a thermal settling error caused by a power dissipation change in the input stage devices (before and after the voltage step). All others CMF amplifier exhibit 0.01% thermal settling tails of several tens of microseconds under the same conditions. The input stage of the EL2165 has been designed to greatly reduce this effect. For A_V = −1, the inverting input is a virtual ground, therefore this tail does not appear even in conventional CMF amplifiers since the input stage does not experience the large voltage change that it does in noninverting mode.

Distortion Performance

The distortion performance of all high frequency amplifiers degrade with increasing frequency. The EL2165 is no exception. However, due to the part's high transimpedance, its distortion performance at a given frequency can be 4 dB–8 dB better than other high speed amplifiers available, with the same power dissipation.

Power Dissipation

The EL2165 amplifier combines both high speed and large output drive capability at a moderate supply current in very small packages. It is possible to exceed the maximum junction temperature allowed under certain supply voltage, temperature and loading conditions. To ensure that the EL2165 remains within it's absolute maximum ratings, the following discussion will help to avoid exceeding the maximum junction temperature.

The maximum power dissipation allowed in a package is determined by it's thermal resistance and the amount of temperature rise according to:

$$P_{Dmax} = (TJ_{MAX} - TA_{MAX})/\theta_{JA}$$

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage plus the power dissipated in the IC due to the load, or:

$$P_{Dmax} = N \times (2 \times V_S \times I_S + (V_S - V_{OUT}) \times V_{OUT}/R_L)$$

where N is the number of amplifiers per package, and I_S is the current per amplifier. (To be more accurate, the quiescent supply current flowing in the output driver transistor should be subtracted from the first term when the output is driving a load. That is to say, due to the class AB nature of the output stage, the output driver current is now included in the second term.)

In general, an amplifier's AC performance degrades at higher temperatures and lower supply current. Unlike some amplifiers, the EL2165 and many other Elantec amplifiers maintain almost constant supply current over temperature so that

EL2165C
30 MHz Precision Current Mode Feedback Amplifier

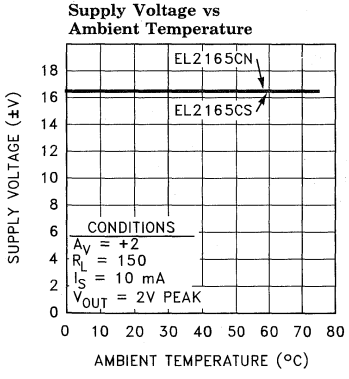
Applications Information — Contd.

the AC performance is not degraded as much at the upper end of the operating temperature range.

The EL2165 consumes typically 4 mA and a maximum of 5 mA. The worst case power dissipated in a IC amplifier operating from split supplies with a grounded load occurs when the output is between ground and half of one of its supplies or, if it can't go that far due to drive limitations, at its maximum value. If we assume that the EL2165 is used for double terminated cable driving application (R_L = 150Ω), and A_V = +2, then the maximum output voltage is 2V, and the average output voltage is 1.4V. If we set the two P_{Dmax} equations equal to each other, and solve for V_S, we get a family of curves for various packages options according to :

$$V_S = \frac{R_L \times (TJ_{MAX} - TA_{MAX}) / N \times \theta_{JA} + (V_{OUT}) \times (V_{OUT})}{(2 \times I_S \times R_L) + (V_{OUT})}$$

The following curve shows supply voltage ($\pm V_S$) vs. temperature for the EL2165's two packages assuming A_V = +2, R_L = 150, and V_{OUT} (peak) = 2V. The curves include the worst case supply specification (I_S = 5 mA).



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The curves do not include heat removal or forcing air, or the simple fact that the package will probably be attached to circuit board, which can also provide some form of heat removal. Larger temperature and voltage ranges are possible with heat removal and forcing air past the device.

Output Current Drive

The EL2165 does not have output short circuit protection. If the output is shorted to ground, the power dissipation could be well over 1W. Heat removal is required in order for the EL2165 to survive an indefinite short.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For these applications, the back termination series resistor will decouple the EL2165 from the capacitive cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without termination resistors. The EL2165 has particularly high capacitive load toleration and can drive a 50 pF load with only 0.3 dB of peaking and a 100 pF load with only 0.5 dB of peaking and without any instability. If higher capacitive loads must be driven or if little or no peaking is required, an additional small value (5Ω–50Ω) resistor can be placed in series with the output. The gain resistor, R_G, can be chosen to make up for the gain loss created by this additional series resistance at the output.

EL2166C

110 MHz Current Feedback Amplifier with Disable

Features

- 110 MHz 3 dB bandwidth ($A_V = +2$)
- 115 MHz 3 dB bandwidth ($A_V = +1$)
- 0.01% differential gain, $R_L = 500\Omega$
- 0.01° differential phase, $R_L = 500\Omega$
- Low supply current, 7.5 mA
- Fast disable < 75 ns
- Low cost
- 1500 V/μs slew rate

Applications

- Video amplifiers
- Cable drivers
- RGB amplifiers
- Test equipment amplifiers
- Current to voltage converters
- Broadcast equipment
- High speed communications
- Video multiplexing

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2166CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2166CS	−40°C to +85°C	8-Pin SOIC	MDP0027

General Description

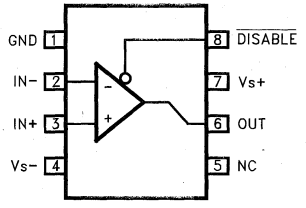
The EL2166C is a current feedback operational amplifier with −3 dB bandwidth of 110 MHz at a gain of +2. Built using the Elantec proprietary monolithic complementary bipolar process, this amplifer uses current mode feedback to achieve more bandwidth at a given gain than a conventional voltage feedback operational amplifier.

The EL2166C is designed to drive a double terminated 75Ω coax cable to video levels. Differential gain and phase are excellent when driving both loads of 500Ω (<0.01%/<0.01°) and double terminated 75Ω cables (0.025%/0.05° @ $V_S = \pm 15V$, 0.04%/0.02° @ $V_S = \pm 5V$).

The EL2166C has a superior output disable function. Time to enable or disable is < 75 ns. The $\overline{\text{DISABLE}}$ pin is TTL/CMOS compatible. In disable mode, the amplifier can withstand over 1500 V/μs signals at their outputs. The amplifier can operate on any supply voltage from 10V (±5V) to 33V (±16.5V), yet consume only 7.5 mA at any supply voltage. The EL2166C is available in 8-pin P-DIP and 8-pin SO packages.

Connection Diagram

EL2166C SO, P-DIP Packages



Top View

EL2166C
110 MHz Current Feedback Amplifier with Disable

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_S^+ and V_S^-	+33V	Voltage at IN+, IN−, V_{OUT}, $\overline{DISABLE}$, GND Pins	(V_{S-}) − 0.5V to (V_{S+}) +0.5V
Voltage between +IN and −IN	±6V	Internal Power Dissipation	See Curves
Current into +IN or −IN	10 mA	Operating Ambient Temperature Range	−40°C to +85°C
Output Current	±50 mA	Operating Junction Temperature	
Current into $\overline{DISABLE}$ Pin	±5 mA	Plastic Packages	150°C
Voltage between $\overline{DISABLE}$ Pin and GND Pin	±7V	Storage Temperature Range	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±15V, R_L = 150Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Temp	Limits			Test Level	Units
				Min	Typ	Max	EL2166C	
V_{OS}	Input Offset Voltage	V_S = ±5V, ±15V	25°C		2	10	I	mV
TC V_{OS}	Average Offset Voltage Drift (Note 1)		Full		10		V	µV/°C
$+I_{IN}$	+Input Current	V_S = ±5V, ±15V	25°C		0.5	5	I	µA
$-I_{IN}$	−Input Current	V_S = ±5V, ±15V	25°C		5	20	I	µA
CMRR	Common Mode Rejection Ratio (Note 2)	V_S = ±5V, ±15V	25°C	55	62		II	dB
−ICMR	−Input Current Common Mode Rejection (Note 2)	V_S = ±5V, ±15V	25°C		0.1	2	I	µA/V
PSRR	Power Supply Rejection Ratio (Note 3)		25°C	65	72		II	dB
−IPSR	−Input Current Power Supply Rejection (Note 3)		25°C		0.1	2	I	µA/V

Open Loop DC Electrical Characteristics — Contd.

V_S = ±15V, R_L = 150Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Temp	Limits			Test Level	Units
				Min	Typ	Max	EL2166C	
R_{OL}	Transimpedance (Note 4)	V_S = ±15V, R_L = 400Ω	25°C	500	2000		I	kΩ
		V_S = ±5V, R_L = 150Ω	25°C	500	1200		I	kΩ
$+R_{IN}$	+Input Resistance		25°C	2.0	5.0		I	MΩ
$+C_{IN}$	+Input Capacitance		25°C		2.5		V	pF
CMIR	Common Mode Input Range	V_S = ±15V	25°C	±12.6	±13.2		I	V
		V_S = ±5V	25°C	±2.6	±3.2		I	V
V_O	Output Voltage Swing	R_L = 400Ω, V_S = ±15V	25°C	±12	±13.5		I	V
		R_L = 150Ω, V_S = ±15V	25°C		±11.4		V	V
		R_L = 150Ω, V_S = ±5V	25°C	±3.0	±3.7		I	V
I_{SC}	Output Short Circuit Current (Note 5)	V_S = ±5V, V_S = ±15V	25°C	50	80	130	I	mA
I_S	Supply Current	V_S = ±15V, V_S = ±5V	25°C		7.5	10.0	I	mA
I_S, OFF	Supply Current Disabled, Pin 8 = 0V		25°C		7.3	10.0	I	mA
I_{OUT}, OFF	Output Current Disabled, Pin 8 = 0V	A_V = +1	25°C		2.0	50.0	I	µA
V_{IH}	$\overline{\text{DISABLE}}$ Pin Voltage for Output Enabled (Note 9)		25°C	2.0			I	V
V_{IL}	$\overline{\text{DISABLE}}$ Pin Threshold for Output Disabled		25°C			0.8	I	V
I_{DIS}, ON	$\overline{\text{DISABLE}}$ Pin Input Current, Pin 8 = +5V		25°C		70	150	I	µA
I_{DIS}, OFF	$\overline{\text{DISABLE}}$ Pin Input Current, Pin 8 = 0V		25°C	−150	−60		I	µA

EL2166C
110 MHz Current Feedback Amplifier with Disable

Closed Loop AC Electrical Characteristics

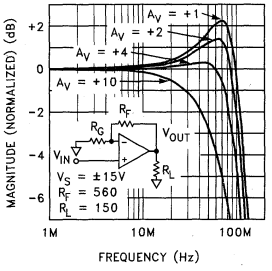
$V_S = \pm 15V$, $A_V = +2$, $R_F = 560\Omega$, $R_L = 150\Omega$, $T_A = 25°C$ unless otherwise noted

Parameter	Description	Conditions	Limits			Test Level	Units
			Min	Typ	Max	EL2166C	
BW	−3 dB Bandwidth (Note 8)	$V_S = \pm 15V$, $A_V = +2$		110		V	MHz
		$V_S = \pm 15V$, $A_V = +1$		115		V	MHz
		$V_S = \pm 5V$, $A_V = +2$		95		V	MHz
		$V_S = \pm 5V$, $A_V = +1$		100		V	MHz
SR	Slew Rate (Notes 6, 8)	$R_L = 400\Omega$	1000	1500		IV	V/μs
t_r, t_f	Rise Time, Fall Time, (Note 8)	$V_{OUT} = \pm 500mV$		3.2		V	ns
t_{pd}	Propagation Delay (Note 8)			4.3		V	ns
OS	Overshoot (Note 8)	$V_{OUT} = \pm 500$ mV		7		V	%
t_s	0.1% Settling Time (Note 8)	$V_{OUT} = \pm 10V$ $A_V = \pm 1$, $R_L = 1K$		35		V	ns
dG	Differential Gain (Notes 7, 8)	$R_L = 150\Omega$, $V_S = \pm 15V$		0.025		V	%
		$R_L = 150\Omega$, $V_S = \pm 5V$		0.05		V	%
		$R_L = 500\Omega$, $V_S = \pm 15V$		0.01		V	%
		$R_L = 500\Omega$, $V_S = 5V$		0.01		V	%
dP	Differential Phase (Notes 7, 8)	$R_L = 150\Omega$, $V_S = \pm 15V$		0.04		V	deg (°)
		$R_L = 150\Omega$, $V_S = \pm 5V$		0.02		V	deg (°)
		$R_L = 500\Omega$, $V_S = \pm 15V$		0.01		V	deg (°)
		$R_L = 500\Omega$, $V_S = 5V$		0.01		V	deg (°)
t_{DIS}	Disable/Enable Time (Note 10)			75		V	ns

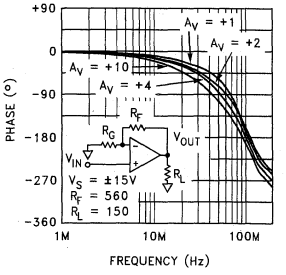
Note 1: Measured from T_{MIN} to T_{MAX}.
Note 2: $V_{CM} = \pm 12.6V$ for $V_S = \pm 15V$ and $T_A = 25°C$
$V_{CM} = \pm 2.6V$ for $V_S = \pm 5V$ and $T_A = 25°C$
Note 3: The supplies are moved from $\pm 5V$ to $\pm 15V$.
Note 4: $V_{OUT} = \pm 7V$ for $V_S = \pm 15V$, and $V_{OUT} = \pm 2V$ for $V_S = \pm 5V$.
Note 5: A heat sink is required to keep junction temperature below absolute maximum when an output is shorted.
Note 6: Slew Rate is with V_{OUT} from $+10V$ to $-10V$ and measured at the 25% and 75% points.
Note 7: DC offset from $-0.714V$ through $+0.714V$, AC amplitude 286 mV_{p-p}, f = 3.58 MHz.
Note 8: All AC tests are performed on a "warmed up" part, except for Slew Rate, which is pulse tested.
Note 9: The EL2166C will remain ENABLED if pin 8 is either left unconnected or V_{IH} is applied to pin 8.
Note 10: Disable/Enable time is defined as the time from when the logic signal is applied to the $\overline{DISABLE}$ pin to when the output voltage has gone 50% of the way from its initial to its final value.

Typical Performance Curves

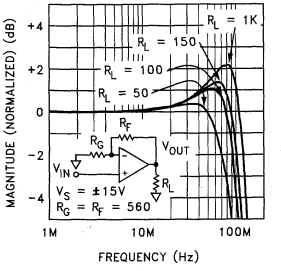
Non-Inverting Frequency Response (Gain)



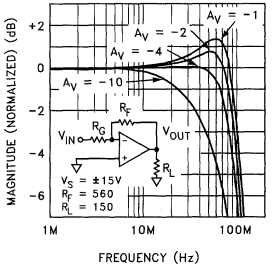
Non-Inverting Frequency Response (Phase)



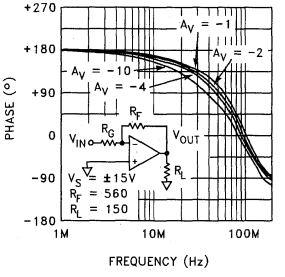
Frequency Response for Various R_L



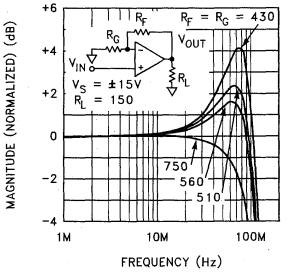
Inverting Frequency Response (Gain)



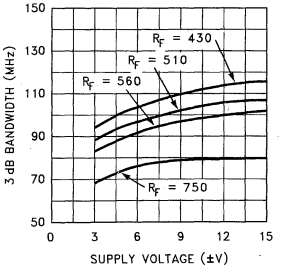
Inverting Frequency Response (Phase)



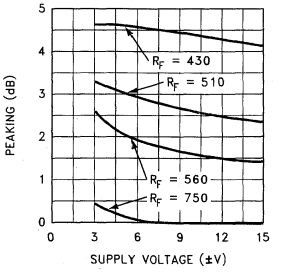
Frequency Response for Various R_F and R_G



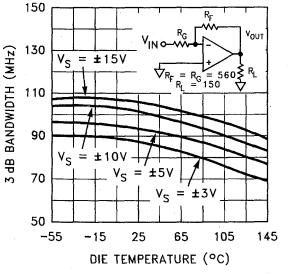
3 dB Bandwidth vs Supply Voltage for $A_V = -1$



Peaking vs Supply Voltage for $A_V = -1$



3 dB Bandwidth vs Temperature for $A_V = -1$



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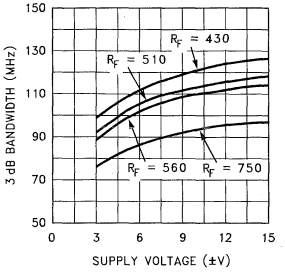
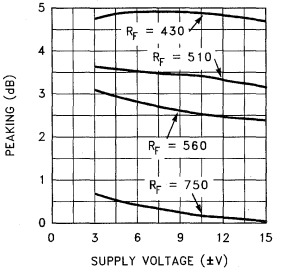
EL2166C
110 MHz Current Feedback Amplifier with Disable

Typical Performance Curves — Contd.

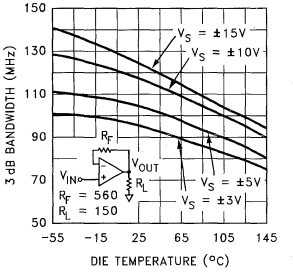
3 dB Bandwidth vs Supply Voltage for A_V = +1



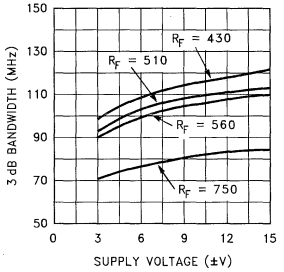
Peaking vs Supply Voltage for A_V = +1



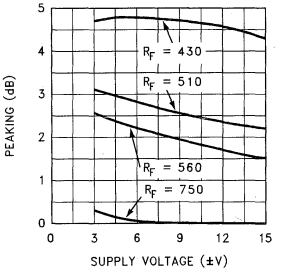
3 dB Bandwidth vs Temperature for A_V = +1



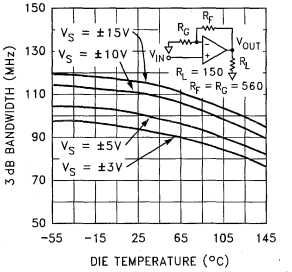
3 dB Bandwidth vs Supply Voltage for A_V = +2



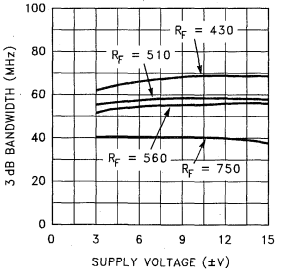
Peaking vs Supply Voltage for A_V = +2



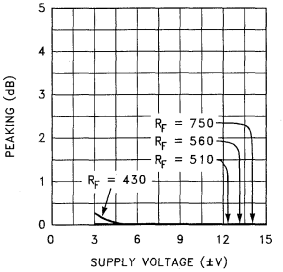
3 dB Bandwidth vs Temperature for A_V = +2



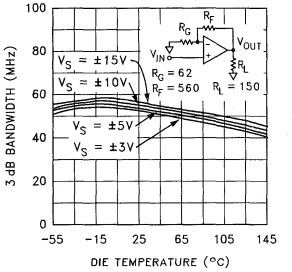
3 dB Bandwidth vs Supply Voltage for A_V = +10



Peaking vs Supply Voltage for A_V = +10



3 dB Bandwidth vs Temperature for A_V = +10



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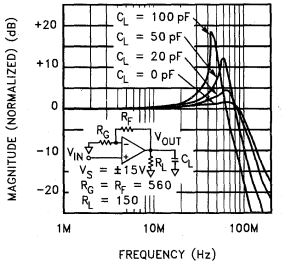
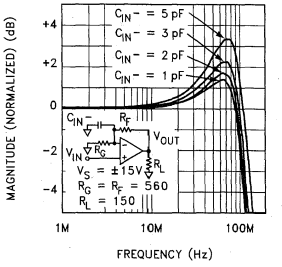
Typical Performance Curves — Contd.

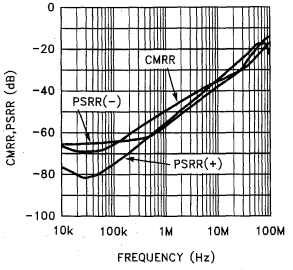
Frequency Response for Various C_L



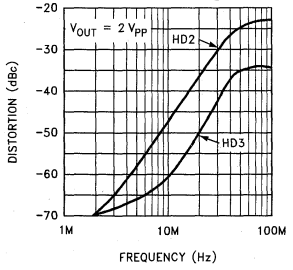
Frequency Response for Various C_{IN-}



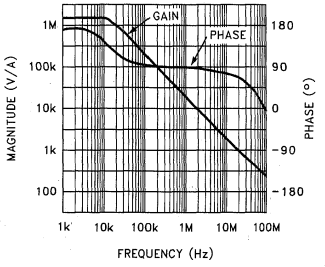
PSRR and CMRR vs Frequency



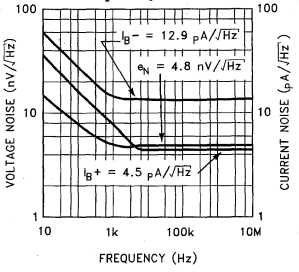
2nd and 3rd Harmonic Distortion vs Frequency



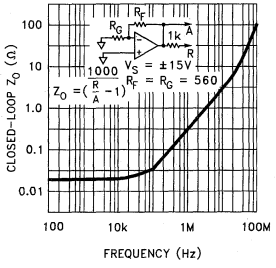
Transimpedance (R_{OL}) vs Frequency



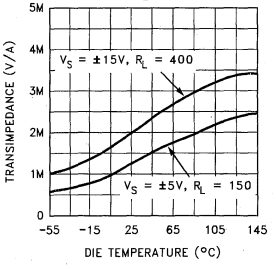
Voltage and Current Noise vs Frequency



Closed-Loop Output Impedance vs Frequency



Transimpedance (R_{OL}) vs Die Temperature



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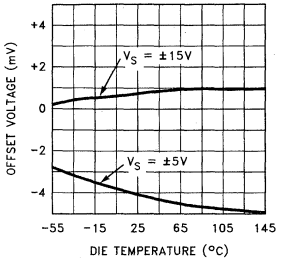
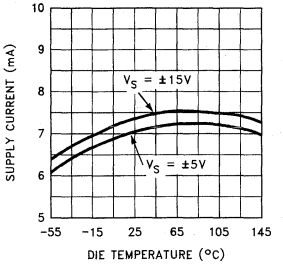
EL2166C
110 MHz Current Feedback Amplifier with Disable

Typical Performance Curves — Contd.

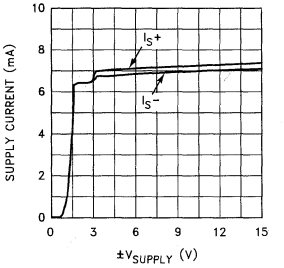
Offset Voltage vs Die Temperature



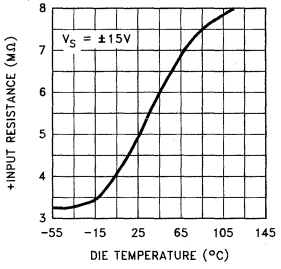
Supply Current vs Die Temperature



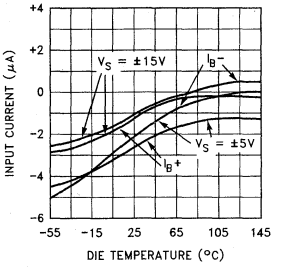
Supply Current vs Supply Voltage



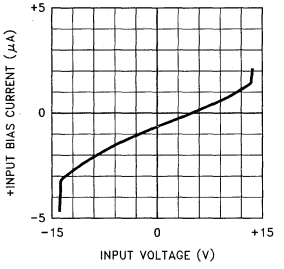
+Input Resistance vs Die Temperature



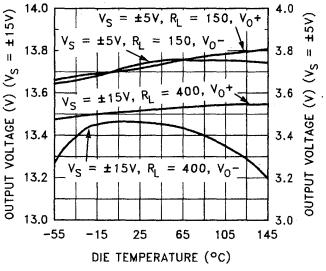
Input Current vs Die Temperature



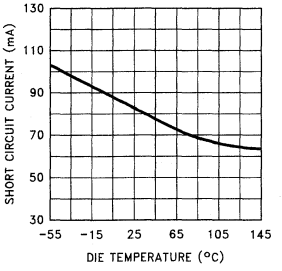
+Input Bias Current vs Input Voltage



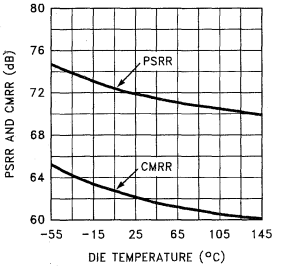
Output Voltage Swing vs Die Temperature



Short Circuit Current vs Die Temperature



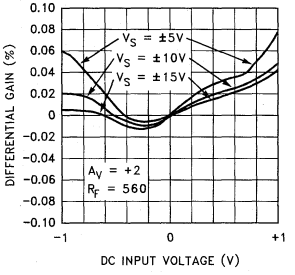
PSRR & CMRR vs Die Temperature



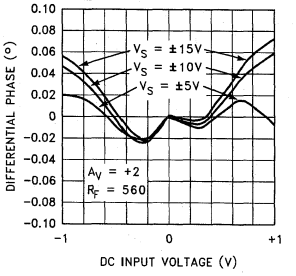
2166-5

Typical Performance Curves — Contd.

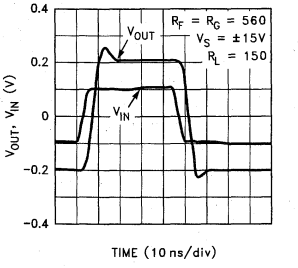
Differential Gain vs DC Input Voltage, R_L = 150



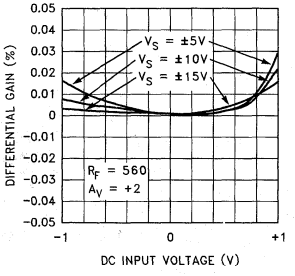
Differential Phase vs DC Input Voltage, R_L = 150



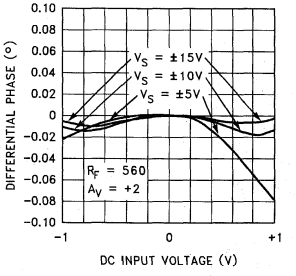
Small Signal Pulse Response



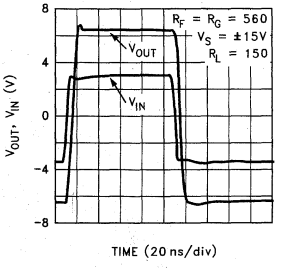
Differential Gain vs DC Input Voltage, R_L = 500



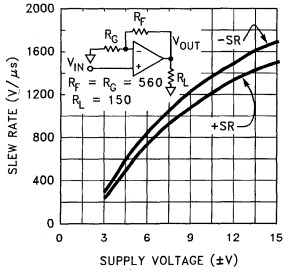
Differential Phase vs DC Input Voltage, R_L = 500



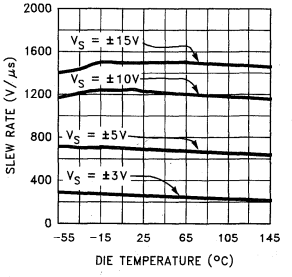
Large Signal Pulse Response



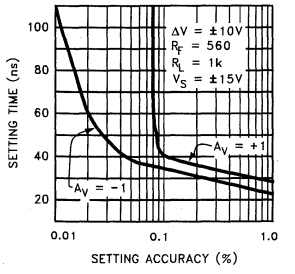
Slew Rate vs Supply Voltage



Slew Rate vs Temperature



Settling Time vs Settling Accuracy

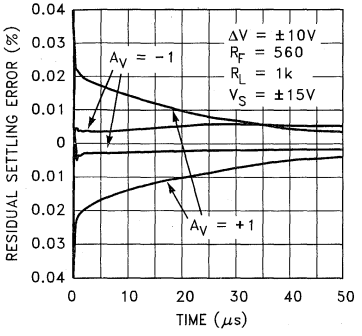


2166-6

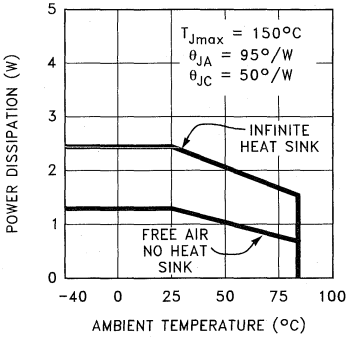
EL2166C
110 MHz Current Feedback Amplifier with Disable

Typical Performance Curves — Contd.

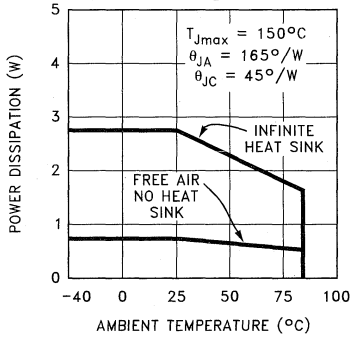
Long Term Settling Error



8-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature

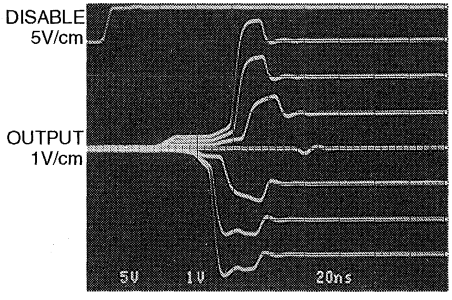


8-Lead Plastic SO
Maximum Power Dissipation
vs Ambient Temperature



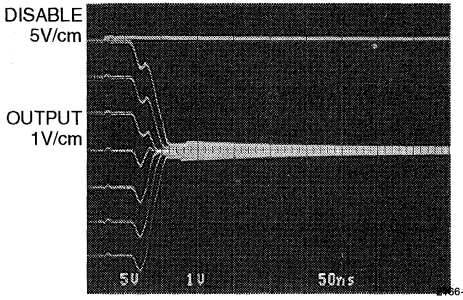
2166-7

ENABLE Response for a Family of D.C. Inputs



$A_V = +2, R_L = 150, V_S = \pm 15V$ 2166-8

DISABLE Response for a Family of D.C. Inputs

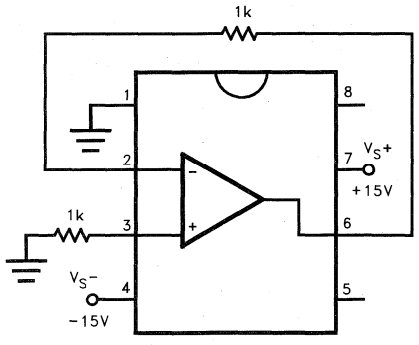


2166-9

$A_V = +2, R_L = 150, V_S = \pm 15V$

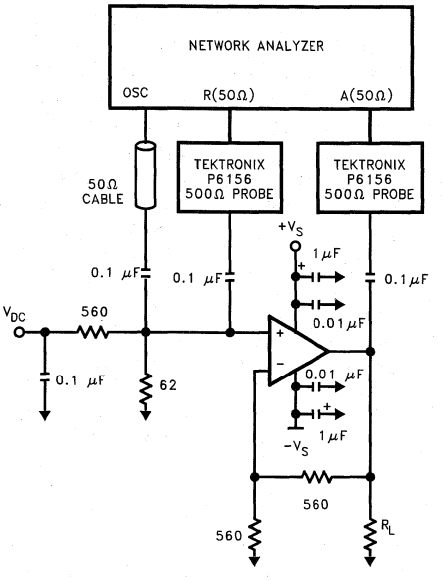
Burn-In Circuit

EL2166C



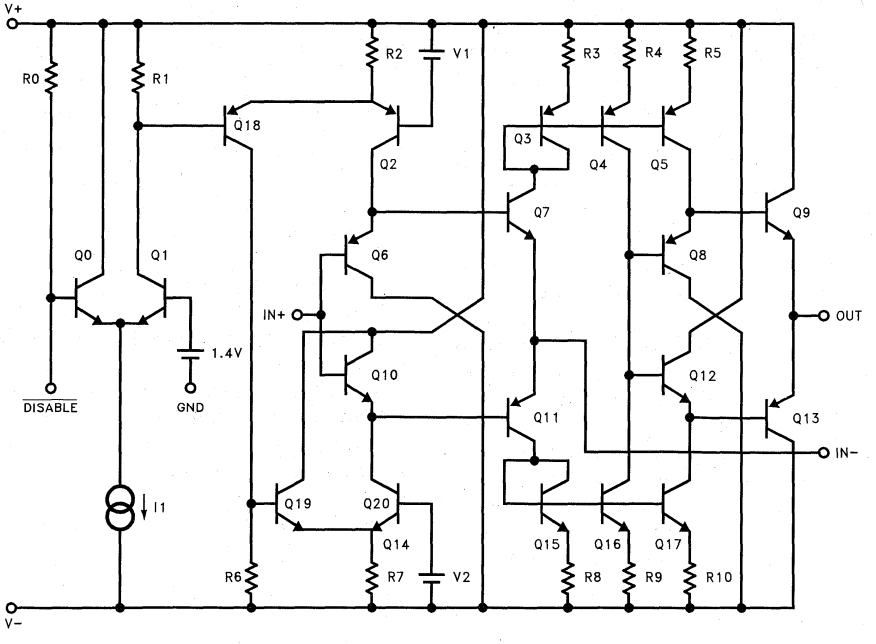
2166-10

Differential Gain and Phase Test Circuit



2166-11

Simplified Schematic



2166-12

EL2166C
110 MHz Current Feedback Amplifier with Disable

Applications Information

Product Description

The EL2166C is a current mode feedback amplifier that offers wide bandwidth and good video specifications at a moderately low supply current. It is built using Elantec's proprietary complimentary bipolar process and is offered in industry standard pin-outs. Due to the current feedback architecture, the EL2166C closed-loop 3 dB bandwidth is dependent on the value of the feedback resistor. First the desired bandwidth is selected by choosing the feedback resistor, R_F, and then the gain is set by picking the gain resistor, R_G. The curves at the beginning of the Typical Performance Curves section show the effect of varying both R_F and R_G. The 3 dB bandwidth is only slightly dependent on the power supply voltage. The bandwidth reduces from 110 MHz to 95 MHz as supplies are varied from $\pm 15V$ to $\pm 5V$. To compensate for this, smaller values of feedback resistor can be used at lower supply voltages.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible, below ¼". The power supply pins must be well bypassed to reduce the risk of oscillation. A 1.0 μF tantalum capacitor in parallel with a 0.01 μF ceramic capacitor is adequate for each supply pin.

For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input (see Capacitance at the Inverting Input section). This implies keeping the ground plane away from this pin. Carbon resistors are acceptable, while use of wire-wound resistors should not be used because of their parasitic inductance. Similarly, capacitors should be low inductance for best performance. Use of sockets, particularly for the SO package, should be avoided. Sockets add parasitic inductance and capacitance which will result in peaking and overshoot.

Capacitance at the Inverting Input

Due to the topology of the current feedback amplifier, stray capacitance at the inverting input will affect the AC and transient performance of the EL2166C when operating in the non-inverting configuration. The characteristic curve of gain vs. frequency with variations of $C_{IN}-$ emphasizes this effect. The curve illustrates how the bandwidth can be extended over 30 MHz with some additional peaking with an additional 5 pF of capacitance at the $V_{IN}-$ pin for the case of $A_V = +2$. Higher values of capacitance will be required to obtain similar effects at higher gains.

In the inverting gain mode, added capacitance at the inverting input has little effect since this point is at a virtual ground and stray capacitance is therefore not "seen" by the amplifier.

Feedback Resistor Values

The EL2166C has been designed and specified with $R_F = 560\Omega$ for $A_V = +2$. This value of feedback resistor yields relatively flat frequency response with <1.5 dB peaking out to 110 MHz. As is the case with all current feedback amplifiers, wider bandwidth, at the expense of slight peaking, can be obtained by reducing the value of the feedback resistor. Inversely, larger values of feedback resistor will cause rolloff to occur at a lower frequency. By reducing R_F to 430Ω, bandwidth can be extended to 120 MHz with 4.5 dB of peaking. See the curves in the Typical Performance Curves section which show 3 dB bandwidth and peaking vs. frequency for various feedback resistors and various supply voltages.

Bandwidth vs Temperature

Whereas many amplifier's supply current and consequently 3 dB bandwidth drop off at high temperature, the EL2166C was designed to have little supply current variations with temperature. An immediate benefit from this is that the 3 dB bandwidth does not drop off drastically with temperature. With $V_S = \pm 15V$ and $A_V = +2$, the bandwidth only varies from 115 MHz to 95 MHz over the entire die junction temperature range of $0°C < T < 150°C$.

Applications Information — Contd.

Supply Voltage Range

The EL2166C has been designed to operate with supply voltages from ±5V to ±15V. AC performance, including −3 dB bandwidth and differential gain and phase, shows little degradation as the supplies are lowered to ±5V. For example, as supplies are lowered from ±15V to ±5V, −3 dB bandwidth reduces only 15 MHz, and differential gain and phase remain less than 0.05%/0.02° respectively.

If a single supply is desired, values from +10V to +30V can be used as long as the input common mode range is not exceeded. When using a single supply, be sure to either 1) DC bias the inputs at an appropriate common mode voltage and AC couple the signal, or 2) ensure the driving signal is within the common mode range of the EL2166C.

Disable Function

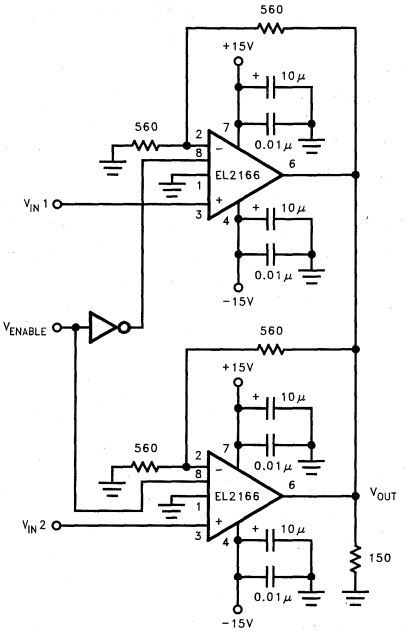
The EL2166C has a superior disable function that has been optimized for video performance. Time to disable/enable is around 75 ns.

During disable, the output of the EL2166C can withstand over 1500 V/μs slew rate signals at its output and the output does not draw excessive currents. The feed-through can be modeled as a 1.5 pF capacitor from $V_{IN}+$ to the output, and the output impedance can be modeled as 4.4 pF in parallel with 180 kΩ to ground when disabled. Consequently, multiplexing with the EL2166C is very easy. Simply tie the outputs of multiple EL2166Cs together and drive the /DISABLE pins with standard TTL or CMOS signals. The disable signal applied to the /DISABLE pin is referenced to the GND pin. The GND pin can be tied as low as the $V_{S}-$ pin. This allows the EL2166C to be operated on a single supply. For example, one could tie the $V_{S}-$ and GND pins to 0V and $V_{S}+$ to +10V, and then use standard TTL or CMOS to drive the /DISABLE pin. Remember to keep the inputs of the EL2166C within their common mode range.

Multiplexing with the EL2166C

An example of multiplexing with the EL2166C and its response curve is shown below. Always be sure that no more than ±5V is applied between $V_{IN}+$ and $V_{IN}-$, which is compatible with standard video signals. This usually becomes an issue only when using the disable feature and amplifying large voltages.

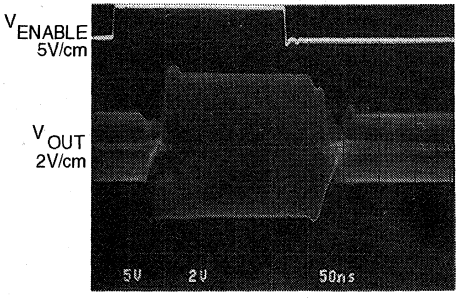
Dual EL2166C Multiplexer



2166-15

In the multiplexer above, suppose one amp is disabled and the other has amplified a signal to +10V at V_{OUT}. The voltage at pin 2 of the dis-

Dual EL2166C Multiplexer Switching 4 V_{PP} Uncorrelated Sinewaves to 2 V_{PP} Uncorrelated Sinewaves



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EL2166C
110 MHz Current Feedback Amplifier with Disable

Applications Information — Contd.

abled amplifier will now be +5V due to the resistor divider action. Therefore, any applied voltage at pin 3 of the disabled amplifier must remain above 0V if the voltage between pins 2 and 3 of the disabled amplifier is to remain less than 5V. Also keep in mind that each disabled amplifier adds more capacitance to the bus, as discussed above. See Disable Function, and Driving Cables and Capacitive Loads in this section, and the Frequency Response for Various C_L curves in the Typical Performance Curve section.

Settling Characteristics

The EL2166C offers superb settling characteristics to 0.1%, typically in the 35 ns to 40 ns range. There are no aberrations created from the input stage which often cause longer settling times in other current feedback amplifiers. The EL2166C is not slew rate limited, therefore any size step up to ±10V gives approximately the same settling time.

As can be seen from the Long Term Settling Error curve, for $A_V = +1$, there is approximately a 0.02% residual which tails away to 0.01% in about 20 µs. This is a thermal settling error caused by a power dissipation differential (before and after the voltage step). For $A_V = -1$, due to the inverting mode configuration, this tail does not appear since the input stage does not experience the large voltage change as in the non-inverting mode. With $A_V = -1$, 0.01% settling time is slightly greater than 100 ns.

Power Dissipation

The EL2166C amplifier combines both high speed and large output current drive capability at a moderate supply current in very small packages. It is possible to exceed the maximum junction temperature allowed under certain supply voltage, temperature, and loading conditions. To ensure that the EL2166C remains within its absolute maximum ratings, the following discussion will help to avoid exceeding the maximum junction temperature.

The maximum power dissipation allowed in a package is determined by its thermal resistance and the amount of temperature rise according to

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage plus the power in the IC due to the load, or

$$P_{DMAX} = 2 * V_S * I_S + (V_S - V_{OUT}) * \frac{V_{OUT}}{R_L}$$

where I_S is the supply current. (To be more accurate, the quiescent supply current flowing in the output driver transistor should be subtracted from the first term because, under loading and due to the class AB nature of the output stage, the output driver current is now included in the second term.)

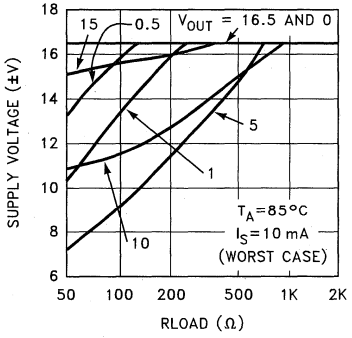
In general, an amplifier's AC performance degrades at higher operating temperature and lower supply current. Unlike some amplifiers, the EL2166C maintains almost constant supply current over temperature so that AC performance is not degraded as much over the entire operating temperature range. Of course, this increase in performance doesn't come for free. Since the current has increased, supply voltages must be limited so that maximum power ratings are not exceeded.

The EL2166C consumes typically 7.5 mA and maximum 10.0 mA. The worst case power in an IC occurs when the output voltage is at half supply, if it can go that far, or its maximum values if it cannot reach half supply. If we set the two P_{DMAX} equations equal to each other, and solve for V_S, we can get a family of curves for various loads and output voltages according to:

$$V_S = \frac{\frac{R_L * (T_{JMAX} - T_{AMAX})}{\theta_{JA}} + (V_{OUT})^2}{(2 * I_S * R_L) + V_{OUT}}$$

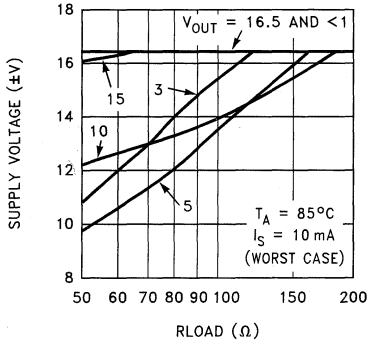
the 2 different packages. The curves assume worst case conditions of $T_A = +85°C$ and $I_S = 10$ mA.

Supply Voltage vs R_{LOAD} for Various V_{OUT} (SO Package)



2166-13

Supply Voltage vs R_{LOAD} for Various V_{OUT} (PDIP Package)



2166-14

can also provide some form of heat removal. Larger temperature and voltage ranges are possible with heat removal and forcing air past the part.

Current Limit

The EL2166C has an internal current limit that protects the circuit in the event of the output being shorted to ground. This limit is set at 80 mA nominally and reduces with junction temperature. At a junction temperature of 150°C, the current limits at about 50 mA. If the output is shorted to ground, the power dissipation could be well over 1W. Heat removal is required in order for the EL2166C to survive an indefinite short.

Driving Cables and Capacitive Loads

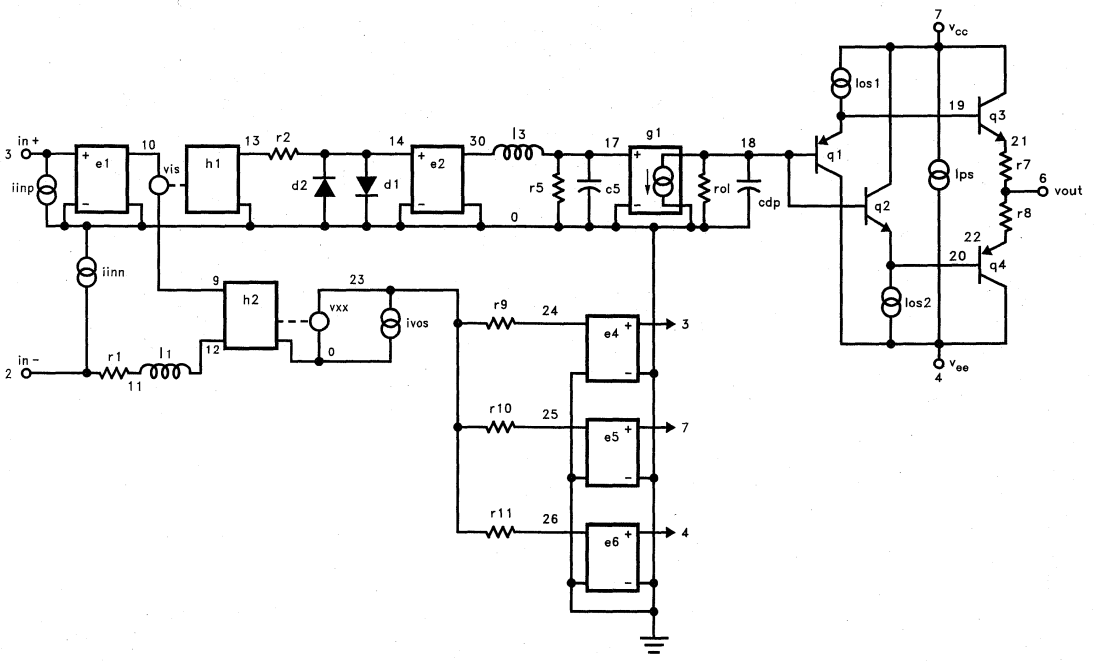
When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back termination series resistor will decouple the EL2166C from the capacitive cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without termination resistors. In these applications, an additional small value (5Ω–50Ω) resistor in series with the output will eliminate most peaking. The gain resistor, R_G, can be chosen to make up for the gain loss created by this additional series resistor at the output.

EL2166C
110 MHz Current Feedback Amplifier with Disable

EL2166C Macromodel

```
* Revision A, May 1994
* AC Characteristics used C_IN − (pin 2) = 1 pF; R_F = 560Ω
* Connections:          +input
*                       |    −input
*                       |    |    +Vsupply
*                       |    |    |    −Vsupply
*                       |    |    |    |    output
*                       |    |    |    |    |
.subckt EL2166C/EL  3    2    7    4    6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 130
l1 11 12 25nH
iinp 3 0 0.5µA
iinm 2 0 5µA
r12 3 0 2Meg
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
*e2 30 0 14 0 0.00166666666
l3 30 17 0.8µH
c5 17 0 1.25pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
ro1 18 0 2Meg
cdp 18 0 2.9pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 2mA
ios2 20 4 2mA
*
* Supply Current
*
ips 7 4 2mA
*
* Error Terms
*
ivos 0 23 2mA
vxx 23 0 0V
e4 24 0 3 0 1.35K
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 562
r10 25 23 1K
r11 26 23 1K
*
* Models
*
.model qn npn (is=5e−15 bf=200 tf=0.1ns)
.model qp pnp (is=5e−15 bf=200 tf=0.1ns)
.model dclamp d (is=1e−30 ibv=0.266 bv=2.8 n=4)
.ends
```

EL2166C Macromodel — Contd.



2166-17

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2170C/EL2270C/EL2470C

70 MHz/1 mA Current Mode Feedback Amplifiers

Features

- Single (EL2170C), dual (EL2270C) and quad (EL2470C) topologies
- 1 mA supply current (per amplifier)
- 70 MHz −3 dB bandwidth
- Low cost
- Single- and dual-supply operation down to ±1.5V
- 0.15%/0.15° diff. gain/diff. phase into 150Ω
- 800 V/μs slew rate
- Large output drive current:
  100 mA (EL2170C)
  55 mA (EL2270C)
  55 mA (EL2470C)
- Also available with disable in single (EL2176C) and dual (EL2276C)
- Higher speed EL2180C/EL2186C family also available (3 mA/250 MHz) in single, dual and quad

Applications

- Low power/battery applications
- HDSL amplifiers
- Video amplifiers
- Cable drivers
- RGB amplifiers
- Test equipment amplifiers
- Current to voltage converters

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2170CN	−40°C to +85°C	8-Pin PDIP	MDP0031
EL2170CS	−40°C to +85°C	8-Pin SOIC	MDP0027
EL2270CN	−40°C to +85°C	8-Pin PDIP	MDP0031
EL2270CS	−40°C to +85°C	8-Pin SOIC	MDP0027
EL2470CN	−40°C to +85°C	14-Pin PDIP	MDP0031
EL2470CS	−40°C to +85°C	14-Pin SOIC	MDP0027

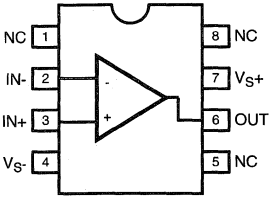
General Description

The EL2170C/EL2270C/EL2470C are single/dual/quad current-feedback operational amplifiers which achieve a −3 dB bandwidth of 70 MHz at a gain of +1 while consuming only 1 mA of supply current per amplifier. They will operate with dual supplies ranging from ±1.5V to ±6V, or from single supplies ranging from +3V to +12V. In spite of their low supply current, the EL2270C and the EL2470C can output 55 mA while swinging to ±4V on ±5V supplies. The EL2170C can output 100 mA with similar output swings. These attributes make the EL2170C/EL2270C/EL2470C excellent choices for low power and/or low voltage cable-driver, HDSL, or RGB applications.

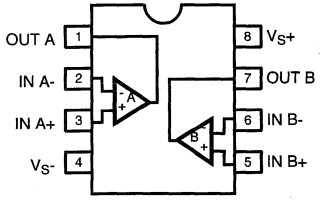
For Single and Dual applications with disable, consider the EL2176C (8-Pin Single) or EL2276C (14-Pin Dual). For higher speed applications where power is still a concern, consider the EL2180C/El2186C family which also comes in similar Single, Dual and Quad configurations. The EL2180C/EL2186C family provides a −3 dB bandwidth of 250 MHz while consuming 3 mA of supply current per amplifier.

Connection Diagrams

EL2170C SO, P-DIP

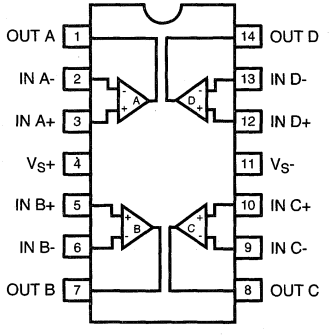


EL2270C SO, P-DIP



2170-1

EL2470C SO, P-DIP



2170-2

EL2170C/EL2270C/EL2470C
70 MHz/1 mA Current Mode Feedback Amplifiers

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_{S+} and V_{S-}	+12.6V	Operating Junction Temperature	
Common-Mode Input Voltage	V_{S-} to V_{S+}	Plastic Packages	150°C
Differential Input Voltage	±6V	Output Current (EL2170C)	±120 mA
Current into +IN or −IN	±7.5 mA	Output Current (EL2270C)	±60 mA
Internal Power Dissipation	See Curves	Output Current (EL2470C)	±60 mA
Operating Ambient Temperature Range	−40°C to +85°C	Storage Temperature Range	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

2

DC Electrical Characteristics V_S = ±5V, R_L = 150Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage			2.5	15	I	mV
TCV_{OS}	Average Input Offset Voltage Drift	Measured from T_{MIN} to T_{MAX}		5		V	µV/°C
dV_{OS}	V_{OS} Matching	EL2270C, EL2470C only		0.5		V	mV
$+I_{IN}$	+ Input Current			0.5	5	I	µA
$d+I_{IN}$	$+I_{IN}$ Matching	EL2270C, EL2470C only		20		V	nA
$-I_{IN}$	− Input Current			4	10	I	µA
$d-I_{IN}$	$-I_{IN}$ Matching	EL2270C, EL2470C only		1.5		V	µA
CMRR	Common Mode Rejection Ratio	V_{CM} = ±3.5V	45	50		I	dB
−ICMR	− Input Current Common Mode Rejection	V_{CM} = ±3.5V		4	10	I	µA/V
PSRR	Power Supply Rejection Ratio	V_S is moved from ±4V to ±6V	60	70		I	dB
−IPSR	− Input Current Power Supply Rejection	V_S is moved from ±4V to ±6V		0.5	5	I	µA/V
R_{OL}	Transimpedance	V_{OUT} = ±2.5V	200	400		I	kΩ
$+R_{IN}$	+ Input Resistance	V_{CM} = ±3.5V	1	4		I	MΩ
$+C_{IN}$	+ Input Capacitance			1.2		V	pF
CMIR	Common Mode Input Range		±3.5	±4.0		I	V

						Level	
V_O	Output Voltage Swing	$V_S = \pm 5$	±3.5	±4.0		I	V
		$V_S = +5$ Single-Supply, High		4.0		V	V
		$V_S = +5$ Single-Supply, Low		0.3		V	V
I_O	Output Current	EL2170C only	80	100		I	mA
		EL2270C only, per Amplifier	50	55		I	mA
		EL2470C only, per Amplifier	50	55		I	mA
I_S	Supply Current	Per Amplifier		1	2	I	mA

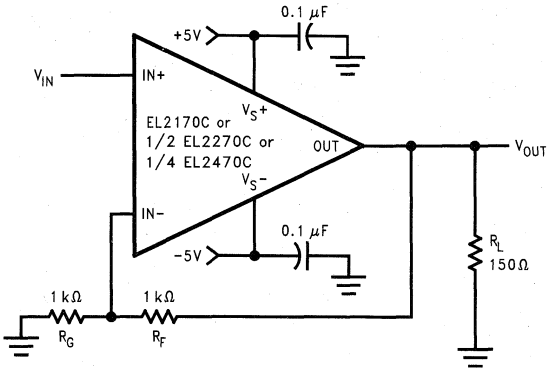
AC Electrical Characteristics

$V_S = \pm 5V$, $R_F = R_G = 1\ k\Omega$, $R_L = 150\Omega$, $T_A = 25°C$ unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
−3 dB BW	−3 dB Bandwidth	$A_V = +1$		70		V	MHz
−3 dB BW	−3 dB Bandwidth	$A_V = +2$		60		V	MHz
SR	Slew Rate	$V_{OUT} = \pm 2.5V$, $A_V = +2$	400	800		IV	V/µs
t_r, t_f	Rise and Fall Time	$V_{OUT} = \pm 500$ mV		4.5		V	ns
t_{pd}	Propagation Delay	$V_{OUT} = \pm 500$ mV		4.5		V	ns
OS	Overshoot	$V_{OUT} = \pm 500$ mV		3.0		V	%
t_s	0.1% Settling	$V_{OUT} = \pm 2.5V$, $A_V = -1$		40		V	ns
dG	Differential Gain	$A_V = +2$, $R_L = 150\Omega$ (Note 1)		0.15		V	%
dP	Differential Phase	$A_V = +2$, $R_L = 150\Omega$ (Note 1)		0.15		V	°
dG	Differential Gain	$A_V = +1$, $R_L = 500\Omega$ (Note 1)		0.02		V	%
dP	Differential Phase	$A_V = +1$, $R_L = 500\Omega$ (Note 1)		0.01		V	°
C_S	Channel Separation	EL2270C, EL2470C only, f = 5 MHz		85		V	dB

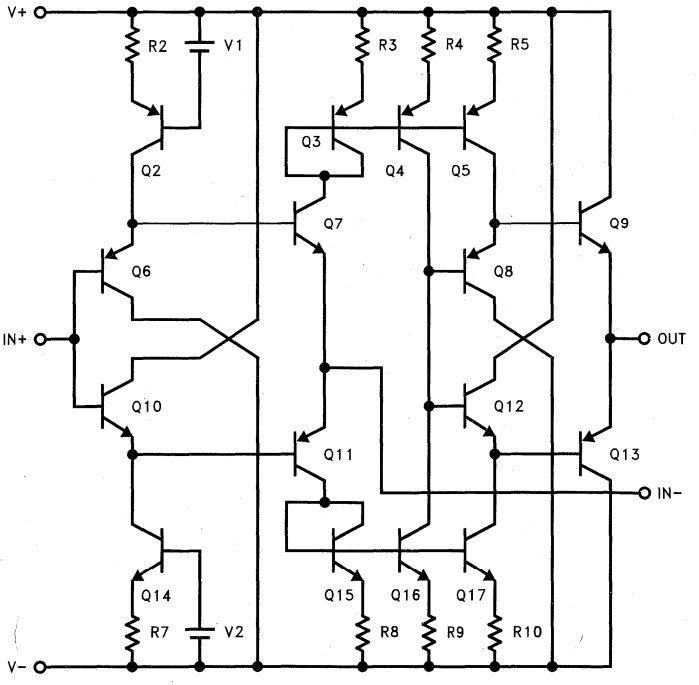
Note 1: DC offset from 0V to 0.714V, AC amplitude 286 mV_{P-P}, f = 3.58 MHz.

Test Circuit (per Amplifier)



2170-3

Simplified Schematic (per Amplifer)



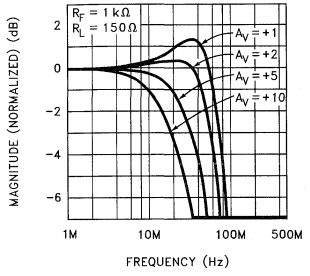
2170-4

EL2170C/EL2270C/EL2470C

70 MHz/1 mA Current Mode Feedback Amplifiers

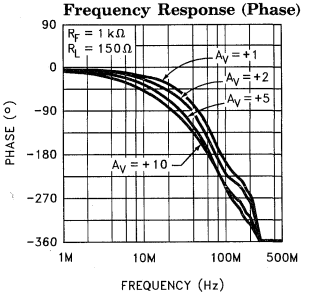
Typical Performance Curves

Non-Inverting Frequency Response (Gain)



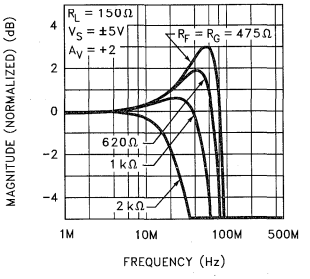
2170-5

Non-Inverting Frequency Response (Phase)



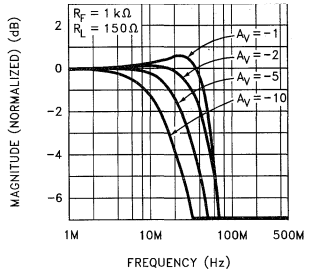
2170-6

Frequency Response for Various R_F and R_G



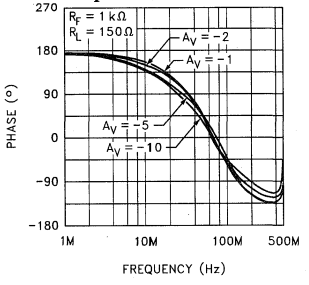
2170-7

Inverting Frequency Response (Gain)



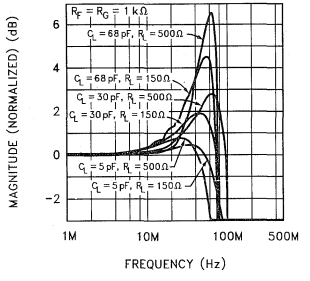
2170-8

Inverting Frequency Response (Phase)



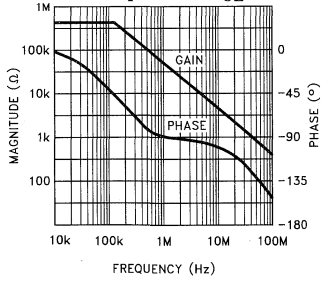
2170-9

Frequency Response for Various R_L and C_L



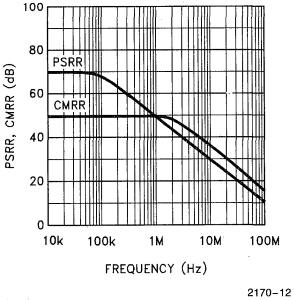
2170-10

Transimpedance (R_{OL})



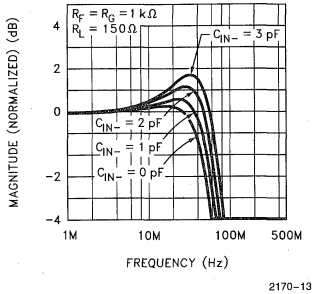
2170-11

PSRR and CMRR



2170-12

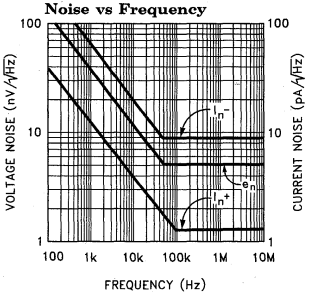
Frequency Response for Various C_{IN-}



2170-13

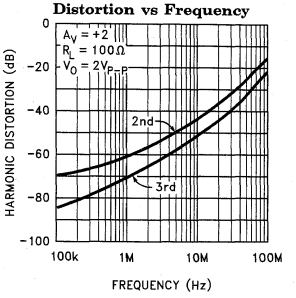
Typical Performance Curves — Contd.

Voltage and Current Noise vs Frequency



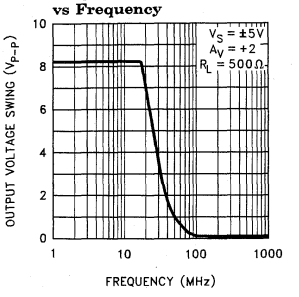
2170-14

2nd and 3rd Harmonic Distortion vs Frequency



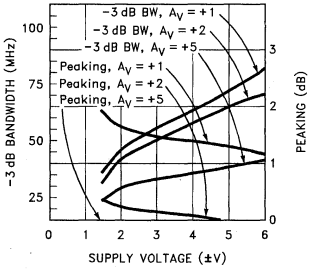
2170-15

Output Voltage vs Frequency



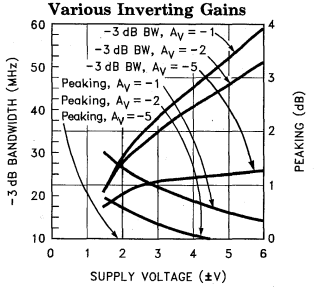
2170-16

−3 dB Bandwith and Peaking vs Supply Voltage for Various Non-Inverting Gains



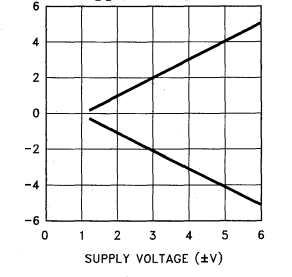
2170-17

−3 dB Bandwith and Peaking vs Supply Voltage for Various Inverting Gains



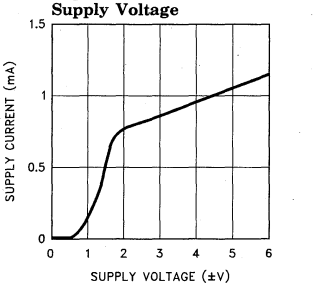
2170-18

Output Voltage Swing vs Supply Voltage



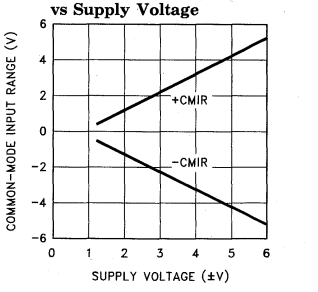
2170-19

Supply Current vs Supply Voltage



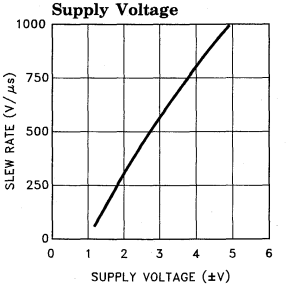
2170-20

Common-Mode Input Range vs Supply Voltage



2170-21

Slew Rate vs Supply Voltage

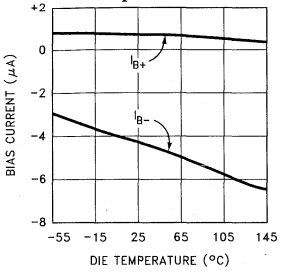


2170-22

EL2170C/EL2270C/EL2470C
70 MHz/1 mA Current Mode Feedback Amplifiers

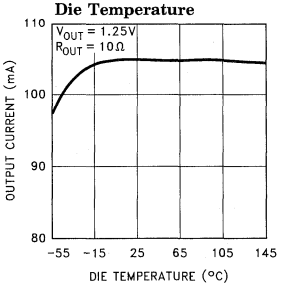
Typical Performance Curves — Contd.

Input Bias Current vs Die Temperature



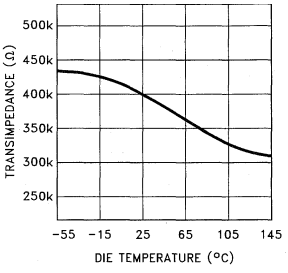
2170-23

Short-Circuit Current vs Die Temperature



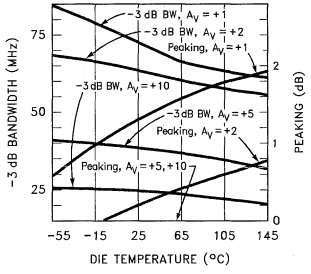
2170-24

Transimpedance (R_{OL}) vs Die Temperature



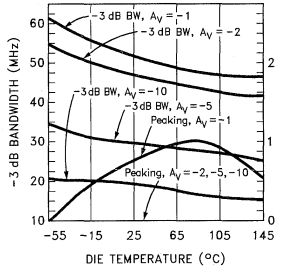
2170-25

−3 dB Bandwith and Peaking vs Die Temperature for Various Non-Inverting Gains



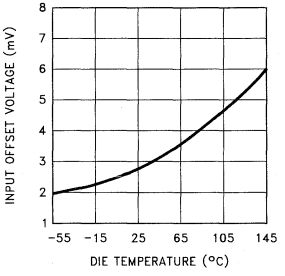
2170-26

−3 dB Bandwith and Peaking vs Die Temperature for Various Inverting Gains



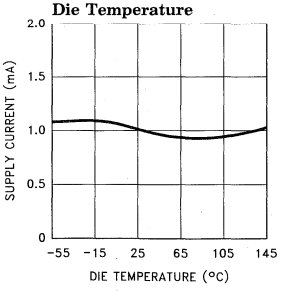
2170-27

Input Offset Voltage vs Die Temperature



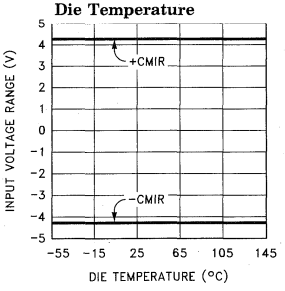
2170-28

Supply Current vs Die Temperature



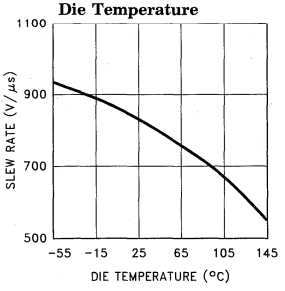
2170-29

Input Voltage Range vs Die Temperature



2170-30

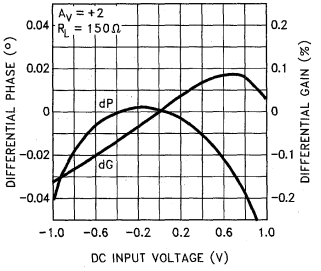
Slew Rate vs Die Temperature



2170-31

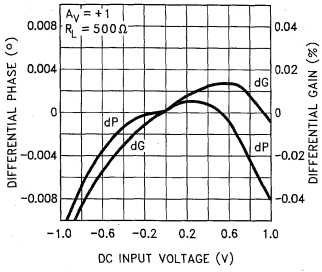
Typical Performance Curves — Contd.

Differential Gain and Phase vs DC Input Voltage at 3.58 MHz/A_V = +2



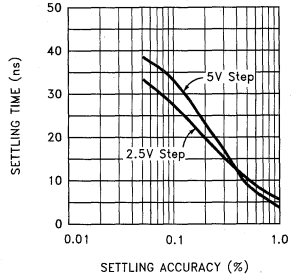
2170-32

Differential Gain and Phase vs DC Input Offset at 3.58 MHz/A_V = +1



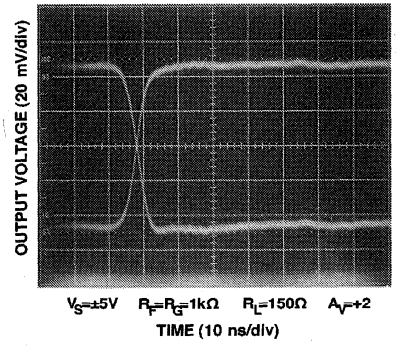
2170-33

Settling Time vs Settling Accuracy



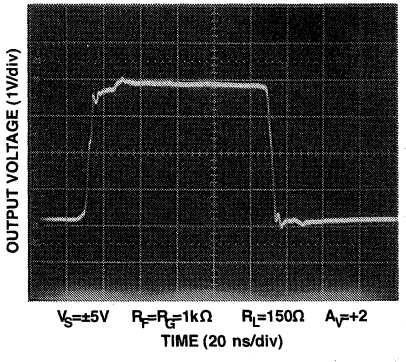
2170-34

Small-Signal Step Response



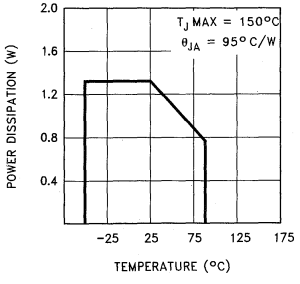
2170-35

Large-Signal Step Response



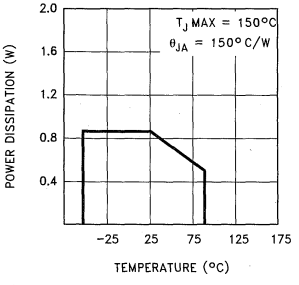
2170-36

8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



2170-37

8-Lead SO Maximum Power Dissipation vs Ambient Temperature

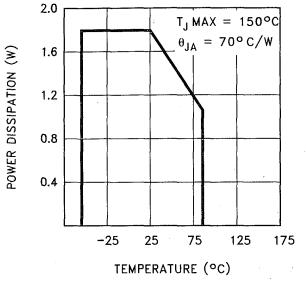


2170-38

EL2170C/EL2270C/EL2470C
70 MHz/1 mA Current Mode Feedback Amplifiers

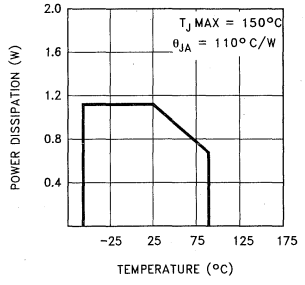
Typical Performance Curves — Contd.

14-Pin Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



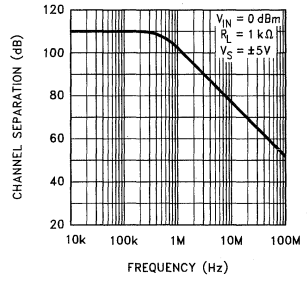
2170-39

14-Lead SO
Maximum Power Dissipation
vs Ambient Temperature



2170-40

Channel Separation
vs Frequency



2170-41

Applications Information

Product Description

The EL2170C/EL2270C/EL2470C are current-feedback operational amplifiers that offer a wide −3 dB bandwidth of 70 MHz and a low supply current of 1 mA per amplifier. All of these products also feature high output current drive. The EL2170C can output 100 mA, while the EL2270C and the EL2470C can output 55 mA per amplifier. The EL2170C/EL2270C/EL2470C work with supply voltages ranging from a single 3V to ±6V, and they are also capable of swinging to within 1V of either supply on the input and the output. Because of their current-feedback topology, the EL2170C/EL2270C/EL2470C do not have the normal gain-bandwidth product associated with voltage-feedback operational amplifiers. This allows their −3 dB bandwidth to remain relatively constant as closed-loop gain is increased. This combination of high bandwidth and low power, together with aggressive pricing make the EL2170C/EL2270C/EL2470C the ideal choice for many low-power/high-bandwidth applications such as portable computing, HDSL, and video processing.

For Single and Dual applications with disable, consider the EL2176C (8-Pin Single) and EL2276C (14-Pin Dual). If higher speed is required, refer to the EL2180C/EL2186C family which provides Singles, Duals, and Quads with 250 MHz of bandwidth while consuming 3 mA of supply current per amplifier.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7 μF tantalum capacitor in parallel with a 0.1 μF capacitor has been shown to work well when placed at each supply pin.

For good AC performance, parasitic capacitance should be kept to a minimum especially at the inverting input (see the Capacitance at the Inverting Input section). Ground plane construction should be used, but it should be removed from the area near the inverting input to minimize any stray capacitance at that node. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of their additional series inductance. Use of sockets, particularly for the SO package should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

Capacitance at the Inverting Input

Any manufacturer's high-speed voltage- or current-feedback amplifier can be affected by stray capacitance at the inverting input. For inverting gains this parasitic capacitance has little effect because the inverting input is a virtual ground, but for non-inverting gains this capacitance (in conjunction with the feedback and gain resistors) creates a pole in the feedback path of the amplifier. This pole, if low enough in frequency, has the same destabilizing effect as a zero in the forward open-loop response. The use of large value feedback and gain resistors further exacerbates the problem by further lowering the pole frequency.

The EL2170C/EL2270C/EL2470C have been specially designed to reduce power dissipation in the feedback network by using large 1 kΩ feedback and gain resistors. With the high bandwidths of these amplifiers, these large resistor values would normally cause stability problems when combined with parasitic capacitance, but by internally canceling the effects of a nominal amount of parasitic capacitance, the EL2170C/EL2270C/EL2470C remain very stable. For less experienced users, this feature makes the EL2170C/EL2270C/EL2470C much more forgiving, and therefore easier to use than other products not incorporating this proprietary circuitry.

EL2170C/EL2270C/EL2470C
70 MHz/1 mA Current Mode Feedback Amplifiers

Applications Information — Contd.

The experienced user with a large amount of PC board layout experience may find in rare cases that the EL2170C/EL2270C/EL2470C have less bandwidth than expected. In this case, the inverting input may have less parasitic capacitance than expected by the internal compensation circuitry of the EL2170C/EL2270C/EL2470C. The reduction of feedback resistor values (or the addition of a very small amount of external capacitance at the inverting input, e. g. 0.5 pF) will increase bandwidth as desired. Please see the curves for Frequency Response for Various R_F and R_G, and Frequency Response for Various $C_{IN}-$.

Feedback Resistor Values

The EL2170C/EL2270C/EL2470C have been designed and specified at gains of +1 and +2 with R_F = 1 kΩ. This value of feedback resistor gives 70 MHz of −3 dB bandwidth at A_V = +1 with about 1.5 dB of peaking, and 60 MHz of −3 dB bandwidth at A_V = +2 with about 0.5 dB of peaking. Since the EL2170C/EL2270C/EL2470C are current-feedback amplifiers, it is also possible to change the value of R_F to get more bandwidth. As seen in the curve of Frequency Response For Various R_F and R_G, bandwidth and peaking can be easily modified by varying the value of the feedback resistor.

Because the EL2170C/EL2270C/EL2470C are current-feedback amplifiers, their gain-bandwidth product is not a constant for different closed-loop gains. This feature actually allows the EL2170C/EL2270C/EL2470C to maintain about the same −3 dB bandwidth, regardless of closed-loop gain. However, as closed-loop gain is increased, bandwidth decreases slightly while stability increases. Since the loop stability is improving with higher closed-loop gains, it becomes possible to reduce the value of R_F below the specified 1 kΩ and still retain stability, resulting in only a slight loss of bandwidth with increased closed-loop gain.

Supply Voltage Range and Single-Supply Operation

The EL2170C/EL2270C/EL2470C have been designed to operate with supply voltages having a span of greater than 3V, and less than 12V. In practical terms, this means that the EL2170C/EL2270C/EL2470C will operate on dual supplies ranging from ±1.5V to ±6V. With a single-supply, the EL2170C/EL2270C/EL2470C will operate from +3V to +12V.

As supply voltages continue to decrease, it becomes necessary to provide input and output voltage ranges that can get as close as possible to the supply voltages. The EL2170C/EL2270C/EL2470C have an input voltage range that extends to within 1V of either supply. So, for example, on a single +5V supply, the EL2170C/EL2270C/EL2470C have an input range which spans from 1V to 4V. The output range of the EL2170C/EL2270C/EL2470C is also quite large, extending to within 1V of the supply rail. On a ±5V supply, the output is therefore capable of swinging from −4V to +4V. Single-supply output range is even larger because of the increased negative swing due to the external pull-down resistor to ground. On a single +5V supply, output voltage range is about 0.3V to 4V.

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This is especially difficult when driving a standard video load of 150Ω, because of the change in output current with DC level. Until the EL2170C/EL2270C/EL2470C, good Differential Gain could only be achieved by running high idle currents through the output transistors (to reduce variations in output impedance). These currents were typically more than the entire 1 mA supply current of each EL2170C/EL2270C/EL2470C amplifier! Special circuitry has been incorporated in the EL2170C/EL2270C/EL2470C to reduce the variation of output impedance with current output. This results in dG and dP specifications of 0.15% and 0.15° while driving 150Ω at a gain of +2.

Applications Information — Contd.

Video Performance has also been measured with a 500Ω load at a gain of +1. Under these conditions, the EL2170C/EL2270C/EL2470C have dG and dP specifications of 0.01% and 0.02° respectively while driving 500 Ω at A_V = +1.

Output Drive Capability

In spite of its low 1 mA of supply current, the EL2170C is capable of providing a minimum of ±80 mA of output current. Similarly, each amplifier of the EL2270C and the EL2470C is capable of providing a minimum of ±50 mA. These output drive levels are unprecedented in amplifiers running at these supply currents. With a minimum ±80 mA of output drive, the EL2170C is capable of driving 50Ω loads to ±4V, making it an excellent choice for driving isolation transformers in telecommunications applications. Similarly, the ±50 mA minimum output drive of each EL2270C and EL2470C amplifier allows swings of ±2.5V into 50Ω loads.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will decouple the EL2170C/EL2270C/EL2470C from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output to eliminate most peaking. The gain resistor (R_G) can then be chosen to make up for any gain loss which may be created by this additional resistor at the output. In many cases it is also possible to simply increase the value of the feedback resistor (R_F) to reduce the peaking.

Current Limiting

The EL2170C/EL2270C/EL2470C have no internal current-limiting circuitry. If any output is shorted, it is possible to exceed the Absolute Maximum Ratings for output current or power dissipation, potentially resulting in the destruction of the device.

Power Dissipation

With the high output drive capability of the EL2170C/EL2270C/EL2470C, it is possible to exceed the 150°C Absolute Maximum junction temperature under certain very high load current conditions. Generally speaking, when R_L falls below about 25Ω, it is important to calculate the maximum junction temperature (T_{JMAX}) for the application to determine if power-supply voltages, load conditions, or package type need to be modified for the EL2170C/EL2270C/EL2470C to remain in the safe operating area. These parameters are calculated as follows:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} * n * PD_{MAX}) \quad [1]$$

where:

T_{MAX} = Maximum Ambient Temperature
θ_{JA} = Thermal Resistance of the Package
n = Number of Amplifiers in the Package
PD_{MAX} = Maximum Power Dissipation of Each Amplifier in the Package.

PD_{MAX} for each amplifier can be calculated as follows:

$$PD_{MAX} = (2 * V_S * I_{SMAX}) + (V_S - V_{OUTMAX}) * (V_{OUTMAX}/R_L)) \quad [2]$$

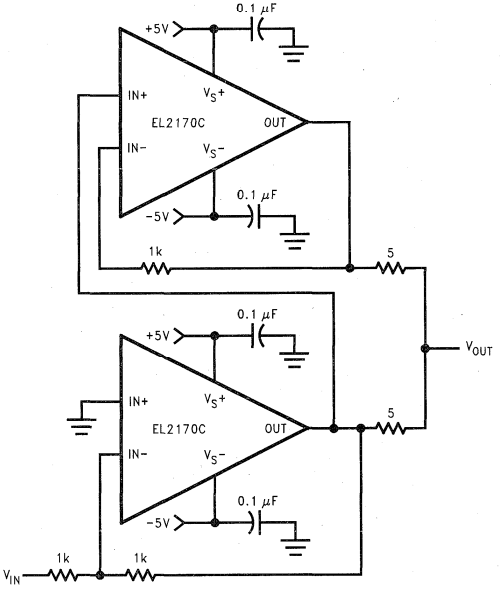
where:

V_S = Supply Voltage
I_{SMAX} = Maximum Supply Current of 1 Amplifier
V_{OUTMAX} = Max. Output Voltage of the Application
R_L = Load Resistance

EL2170C/EL2270C/EL2470C
70 MHz/1 mA Current Mode Feedback Amplifiers

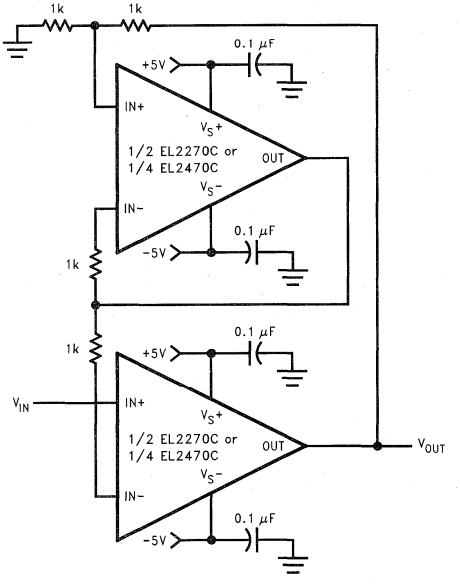
Typical Application Circuits

Inverting 200 mA Output Current Distribution Amplifier



2170-42

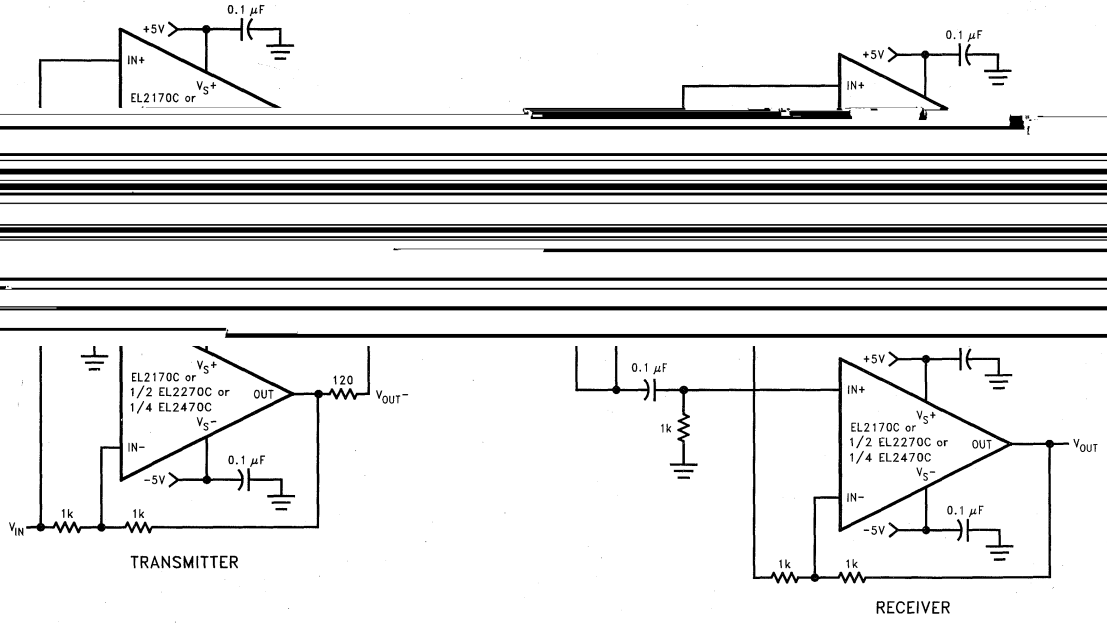
Fast-Settling Precision Amplifier



2170-43

Typical Application Circuits — Contd.

Differential Line-Driver/Receiver



```
* Connections:          +input
*                       |    -input
*                       |    |    +Vsupply
*                       |    |    |    -Vsupply
*                       |    |    |    |    output
*                       |    |    |    |    |
.subckt EL2170/el       3    2    7    4    6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 165
l1 11 12 25nH
iinp 3 0 0.5uA
iinm 2 0 4uA
r12 3 0 4Meg
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
e2 30 0 14 0 0.00166666666
l3 30 17 0.5uH
c5 17 0 0.69pF
r5 17 0 300
*
g1 0 18 17 0 1.0
rol 18 0 400K
cdp 18 0 1.9pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 0.4mA
ios2 20 4 0.4mA
*
* Supply Current
*
ips 7 4 1nA
*
* Error Terms
*
ivos 0 23 2mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 -1.0
r9 24 23 0.316K
r10 25 23 3.2K
r11 26 23 3.2K
*
* Models
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.model qn npn(is=5e-15 bf=200 tf=0.01nS)
.model qp pnp(is=5e-15 bf=200 tf=0.01nS)
.model dclamp d(is=1e-30 ibv=0.266
+ bv=1.3v n=4)
.ends
```

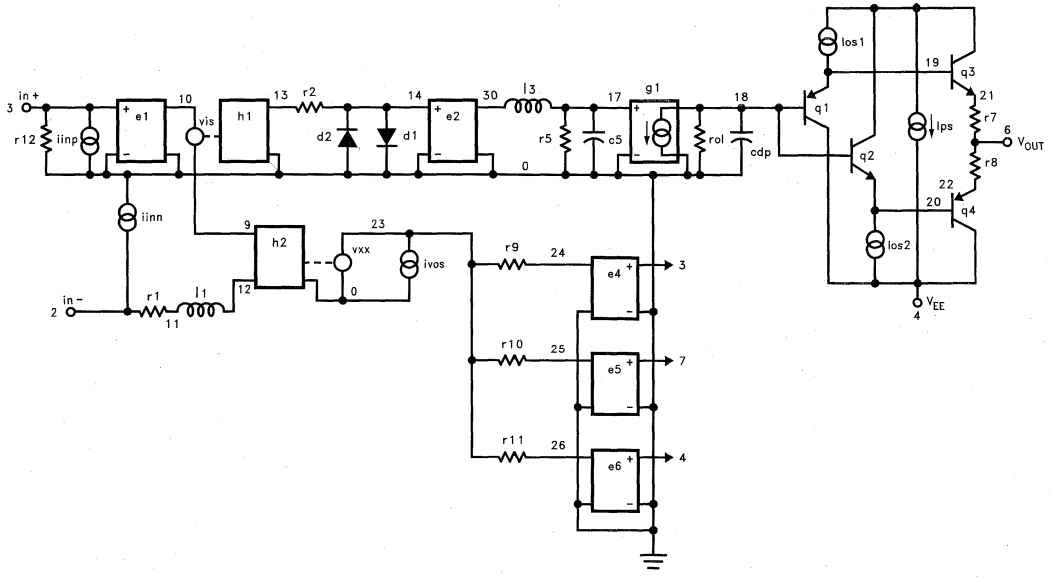
in+
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r12
iinp
e1
10
vis
h1
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r2
d2
d1
14
e2
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l3
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r5
17
c5
g1
18
rol
cdp
los1
19
q3
21
r7
6
V_{OUT}
r8
q1
q2
Ips
22
20
q4
los2
V_{EE}
4
iinn
9
h2
23
vxx
ivos
0
in−
2
r1
11
l1
12
r9
24
e4
3
r10
25
e5
7
r11
26
e6
4

2170-45

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2175C

120 MHz Precision Current Mode Feedback Amplifier

Features

- 30 MΩ transimpedance
- 142 MHz − 3 dB bandwidth ($A_V = +1$)
- 120 MHz − 3 dB bandwidth ($A_V = +2$)
- 1 mV input offset voltage
- 2 μA negative input bias current
- 86 dB common-mode rejection ratio
- 92 dB power supply rejection ratio
- Low supply current, 8.5 mA
- Wide supply range, ±4.5V to ±16.5V
- 80 mA peak output current
- High capacitive load toleration
- Input/output compliance to ±2V of supplies
- 1,000 V/μs slew rate
- 50 ns settling to 0.1%
- 90 ns settling to 0.01%
- −70 dB distortion @ 4 MHz
- Low cost

Applications

- Instrumentation circuitry
- Current to voltage convertors
- RGB amplifiers
- DAC/ADC output amplifier/ buffer
- Cable drivers
- Low distortion communications
- Medical imaging
- CCD imaging
- Infrared image enhancement

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2175CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2175CS	−40°C to +85°C	8-Lead SO	MDP0027

General Description

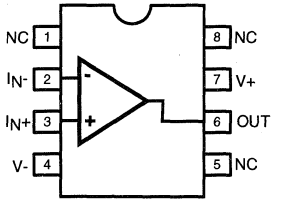
The EL2175C is a low offset, high transimpedance current mode feedback amplifier with a −3 dB bandwidth of 120 MHz at a gain of +2. Built on Elantec's proprietary monolithic complementary bipolar process, this amplifier uses current mode feedback to achieve more bandwidth at a give gain than conventional voltage feedback amplifiers.

The high 30 MΩ transimpedance gain and low input referred offset of the EL2175 will also bring the final settled output much closer to its ideal value than is possible with earlier CMF designs.

In addition, the common-mode and power supply rejection have been greatly improved over earlier current mode feedback amplifiers and the input offset voltage and current have been trimmed to rival that of good conventional voltage feedback amplifiers. The part has a typical slew rate of 1,000 V/μs and a 0.01% settling time of less than 90 ns in inverting mode. At a gain of +2 and an output signal level of 2 V_{P-P} the total harmonic distortion is only −70 dB at 4 MHz.

The amplifier can operate on any supply from 9V (±4.5V) to 33V (±16.5V), yet consumes only 8.5 mA at any supply voltage. Using the industry standard pinout, the EL2175C is available in both P-DIP and SO packages.

Connection Diagram



2175-1

EL2175C
120 MHz Precision Current Mode Feedback Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_S+ and V_S−	+33V	Operating Junction Temperature	
Voltage between I_N+ and I_N−	±6V	Plastic Package	150°C
Current into I_N+ and I_N−	4 mA	Storage Temperature Range	−65°C to +150°C
Operating Ambient Temperature Range	See Curves		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±15V, R_L = 500Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage		25°C		1	3	I	mV
TC V_{OS}	Average Offset Voltage Drift (Note 1)		Full		2		V	µV/°C
I_{IN}+	+ Input Current		25°C		−2.5	±6	I	µA
I_{IN}−	− Input Current		25°C		±2	±7	I	µA
CMRR	Common Mode Rejection Ratio (Note 2)		25°C	79	86		II	dB
ICMR−	−Input Current Common Mode Rejection (Note 2)		25°C		27	100	I	nA/V
PSRR	Power Supply Rejection Ratio (Note 3)		25°C	84	92		II	dB
IPSR−	−Input Current Power Supply Rejection (Note 3)		25°C		28	225	I	nA/V
R_{OL}	Transimpedance (Note 4)	V_S = ±15V, R_L = 500Ω	25°C		30		I	MΩ
		V_S = ±5V, R_L = 150Ω	25°C	5	25		I	MΩ
R_{IN} +	+ Input Resistance		25°C	18	25		II	MΩ
C_{IN} +	+ Input Capacitance		25°C		2.5		V	pF
CMIR	Common Mode Input Range (Note 2)	V_S = ±15V	25°C	±12	±12.5		I	V
		V_S = ±5V	25°C	±2.0	±2.5		I	V

EL2175C
120 MHz Precision Current Mode Feedback Amplifier

Open Loop DC Electrical Characteristics

V_S = ±15V, R_L = 500Ω, T_A = 25°C unless otherwise specified — Contd.

Parameter	Description	Conditions	Temp	Min	Typ	Max	Test Levels	Units
V_O	Output Voltage Swing	R_L = 500Ω V_S = ±15V	25°C	±12, 3	±13		I	I
		R_L = 150Ω V_S = ±15V	25°C		±11.7		V	V
		R_L = 150Ω V_S = ±5V	25°C	±2.7	±3.0		I	I
I_{SC}	Output Short Circuit Current (Note 4)	V_S = ±5V V_S = ±15V	25°C	55 80	90 135		I	mA
I_S	Supply Current	V_S = ±15V	25°C		8.5	10.25	I	mA

Closed Loop AC Electrical Characteristics

$V_S = \pm 15V$, $A_V = +2$, $R_F = 750\Omega$, $R_L = 500\Omega$, $T_A = 25°C$ unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
BW	−3 dB (Note 8) BDWH	$V_S = \pm 15V$, $A_V = +2$, $R_F = 750\Omega$		120		V	MHz
		$V_S = \pm 15V$, $A_V = +1$, $R_F = 1K\Omega$		142		V	MHz
		$V_S = \pm 5V$, $A_V = +2$, $R_F = 750\Omega$		98		V	MHz
		$V_S = \pm 5V$, $A_V = +1$, $R_F = 1K\Omega$		113		V	MHz
SR	Slew Rate (Notes 6, 8)	$R_L = 500\Omega$	500	1000		I	V/μs
		$R_F = 1\,K\Omega$, $R_G = 110\Omega$ $R_L = 500\Omega$		1000		V	V/μs
t_r, t_f	Rise Time, Fall Time (Note 8)	$V_{OUT} = \pm 500$ mV		3.7		V	ns
t_{pd}	Propagation Delay			7.7		V	ns
O_S	Overshoot (Note 8)	$V_{OUT} = \pm 500$ mV		6		V	%
t_s	0.1% Settling Time (Note 8)	$\Delta V_{OUT} = \pm 10V$, $A_V = 1$		70		V	ns
		$\Delta V_{OUT} = \pm 10V$, $A_V = -1$		50			
		$\Delta V_{OUT} = \pm 10V$, $A_V = 2$		60			
t_s	0.01% Settling Time	$\Delta V_{OUT} = \pm 10V$, $A_V = 1$		900		V	ns
		$\Delta V_{OUT} = \pm 10V$, $A_V = -1$		90			
		$\Delta V_{OUT} = \pm 10V$, $A_V = 2$		500			
dG	Differential Gain (Notes 7, 8)	$R_L = 150\Omega$		0.09		V	%
		$R_L = 500\Omega$		0.02		V	%
dP	Differential Phase (Notes 7, 8)	$R_L = 150\Omega$		0.5		V	deg (°)
		$R_L = 500\Omega$		0.16		V	deg (°)

Note 1: Measured from T_{MIN} to T_{MAX}

Note 2: $V_{CM} = \pm 12V$ for $V_S = \pm 15V$ and $T_A = 25°C$
$V_{CM} = \pm 2V$ for $V_S = \pm 5V$ and $T_A = 25°C$
CMIR is guaranteed by the part passing CMRR at the rated common-mode swing.

Note 3: The supplies are moved from $\pm 4.5V$ to $\pm 15V$.

Note 4: $V_{OUT} = \pm 10V$ for $V_S = \pm 15V$, and $V_{OUT} = \pm 2V$ for $V_S = \pm 5V$.

Note 5: A heat sink is required to keep junction temperature below absolute maximum when an output is shorted.

Note 6: Slew Rate is with V_{OUT} from $+10V$ to $-10V$ and measured at the 25% and 75% points.

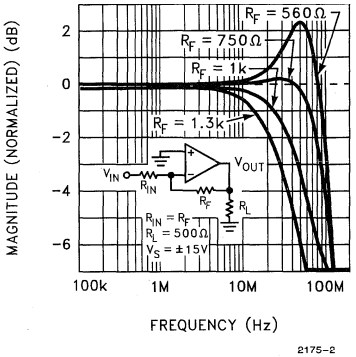
Note 7: DC offset from $-0.714V$ through $+0.714V$, AC amplitude 286 mV_{p-p}, f = 3.58 MHz.

Note 8: All AC tests are performed on a "warmed up" part, except for Slew Rate, which is pulse tested.

EL2175C
120 MHz Precision Current Mode Feedback Amplifier

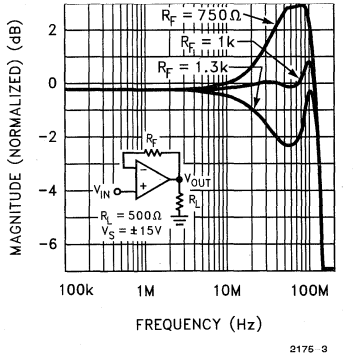
Typical Performance Curves

Frequency Response for $A_V = -1$ and for Various R_F Values



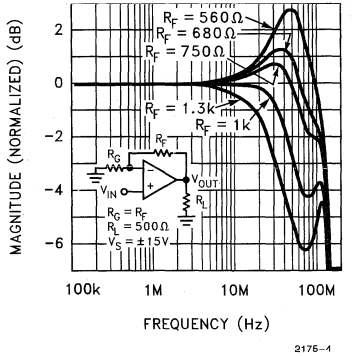
2175-2

Frequency Response for $A_V = +1$ and for Various R_F Values



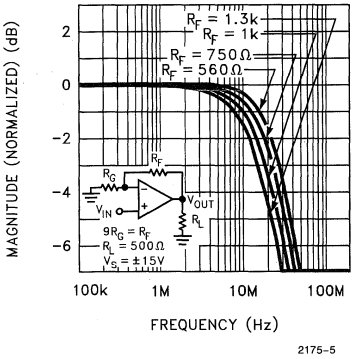
2175-3

Frequency Response for $A_V = +2$ and for Various R_F Values



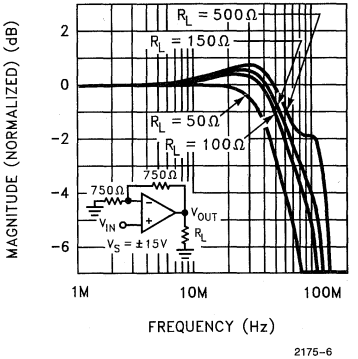
2175-4

Frequency Response for $A_V = +10$ and for Various R_F Values



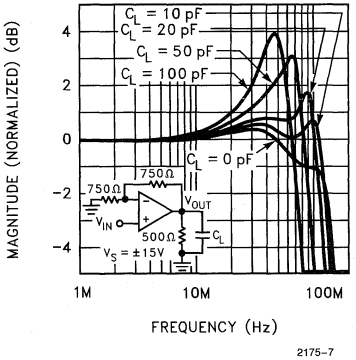
2175-5

Frequency Response for Various Values of R_L



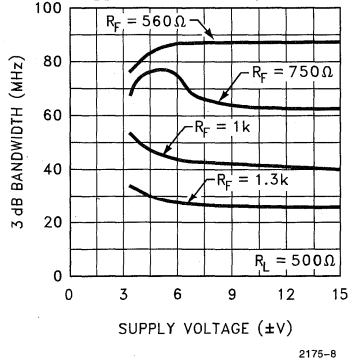
2175-6

Frequency Response for Various Values of C_L



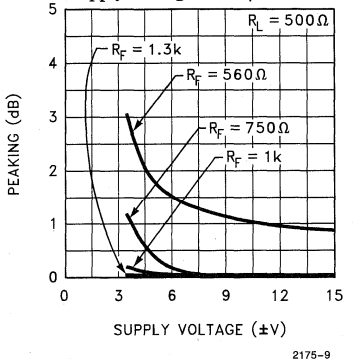
2175-7

3 dB Bandwidth vs Supply Voltage for $A_V = -1$



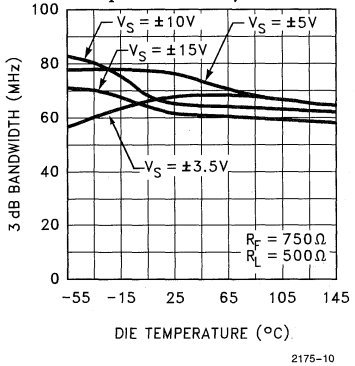
2175-8

Peaking vs Supply Voltage for $A_V = -1$



2175-9

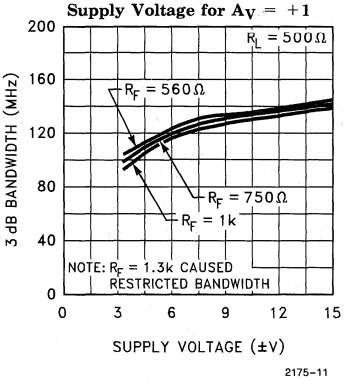
3 dB Bandwidth vs Temperature for $A_V = -1$



2175-10

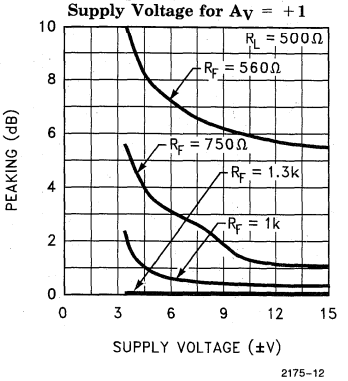
Typical Performance Curves — Contd.

3 dB Bandwidth vs Supply Voltage for A_V = +1



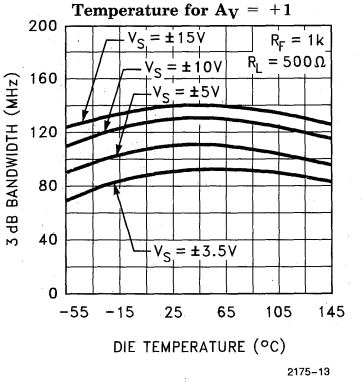
2175-11

Peaking vs Supply Voltage for A_V = +1



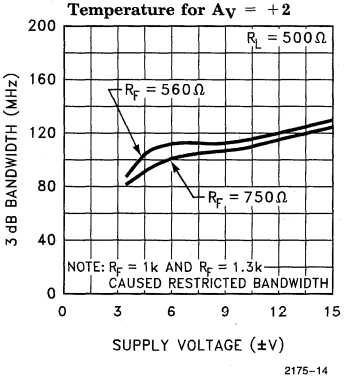
2175-12

3 dB Bandwidth vs Temperature for A_V = +1



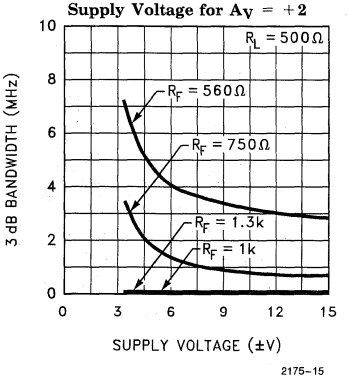
2175-13

3 dB Bandwidth vs Temperature for A_V = +2



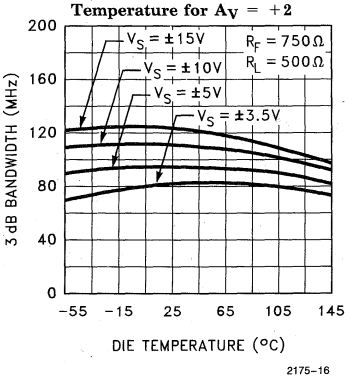
2175-14

Peaking vs Supply Voltage for A_V = +2



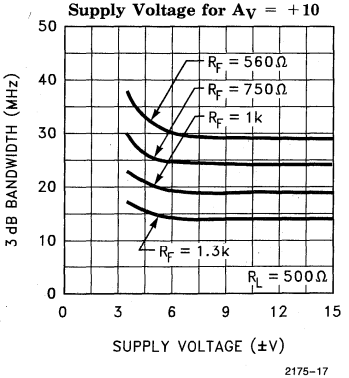
2175-15

3 dB Bandwidth vs Temperature for A_V = +2



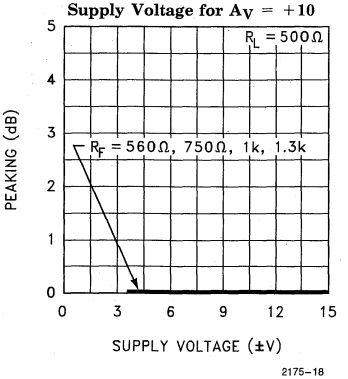
2175-16

3 dB Bandwidth vs Supply Voltage for A_V = +10



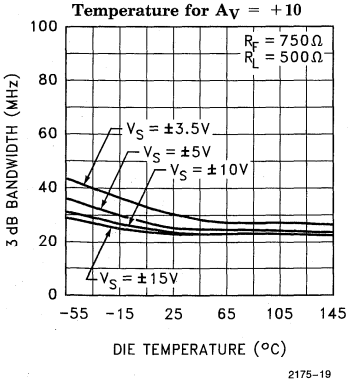
2175-17

Peaking vs Supply Voltage for A_V = +10



2175-18

3 dB Bandwidth vs Temperature for A_V = +10

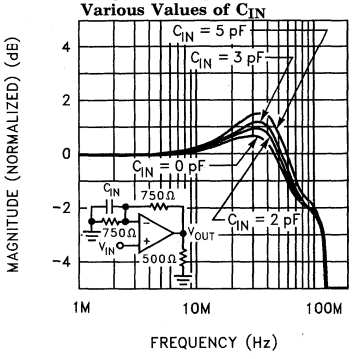


2175-19

EL2175C
120 MHz Precision Current Mode Feedback Amplifier

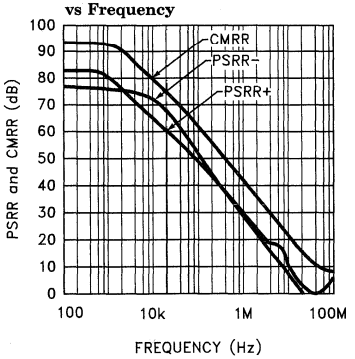
Typical Performance Curves — Contd.

Frequency Response for Various Values of C_{IN}



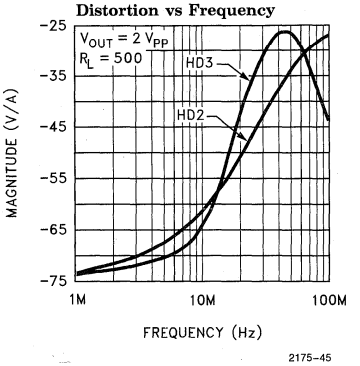
2175-20

PSRR and CMRR vs Frequency



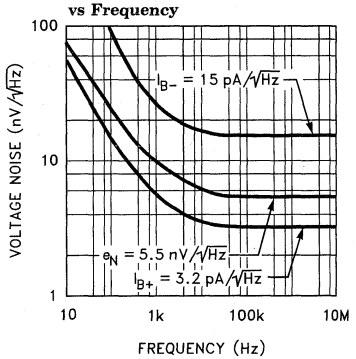
2175-21

Second and Third Harmonic Distortion vs Frequency



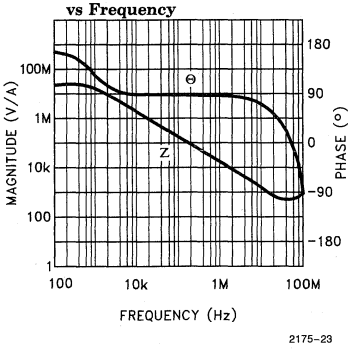
2175-45

Voltage and Current Noise vs Frequency



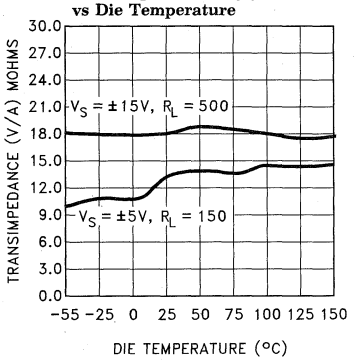
2175-22

Transimpedance (R_{OL}) vs Frequency



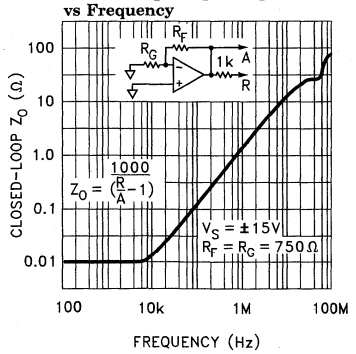
2175-23

Transimpedance (R_{OL}) vs Die Temperature



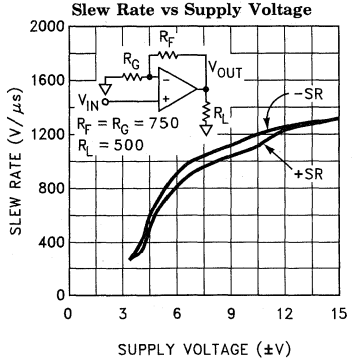
2175-24

Closed-Loop Output Impedance vs Frequency



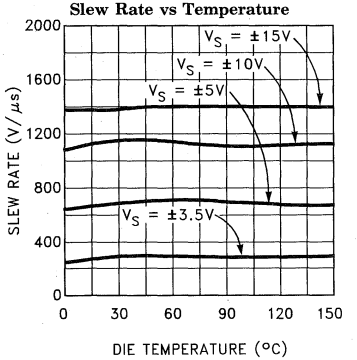
2175-25

Slew Rate vs Supply Voltage



2175-26

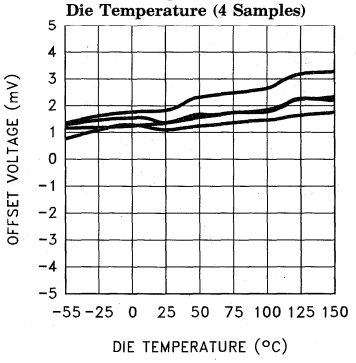
Slew Rate vs Temperature



2175-27

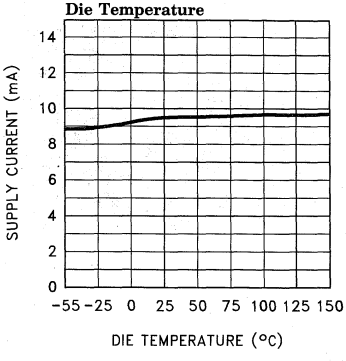
Typical Performance Curves — Contd.

Offset Voltage vs Die Temperature (4 Samples)



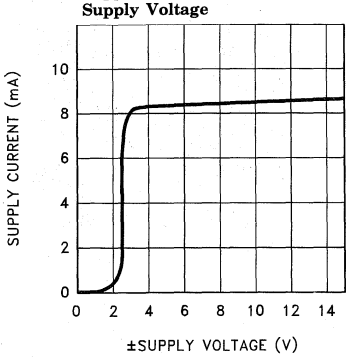
2175-28

Supply Current vs Die Temperature



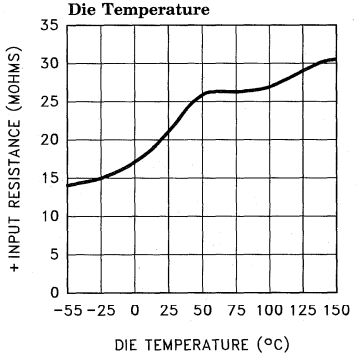
2175-29

Supply Current vs Supply Voltage



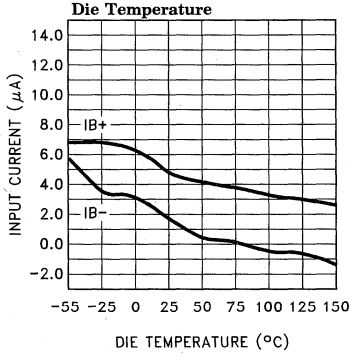
2175-30

+Input Resistance vs Die Temperature



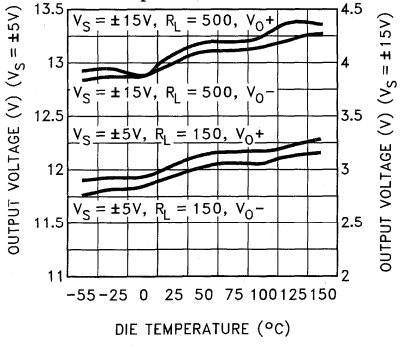
2175-31

Input Current vs Die Temperature



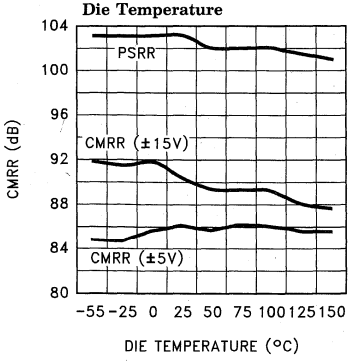
2175-32

Output Voltage Swing vs Die Temperature



2175-33

PSRR and CMRR vs Die Temperature

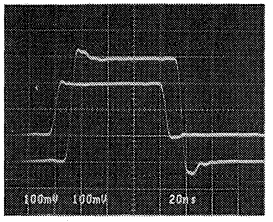


2175-34

EL2175C
120 MHz Precision Current Mode Feedback Amplifier

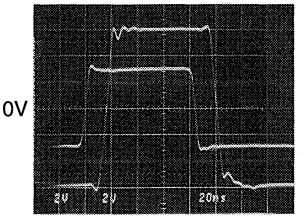
Typical Performance Curves — Contd.

Small Signal Pulse Response



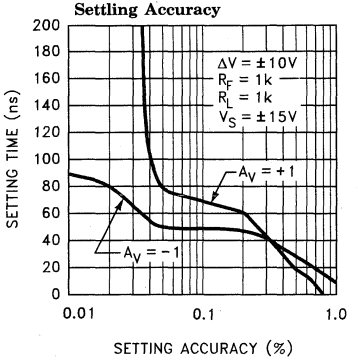
2175-35

Large Signal Pulse Response



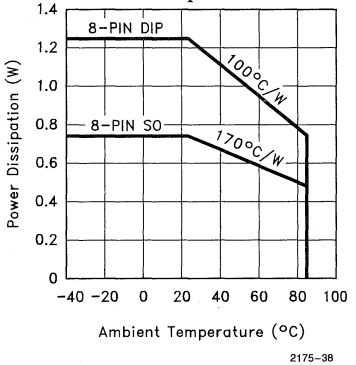
2175-36

Settling Time vs Settling Accuracy



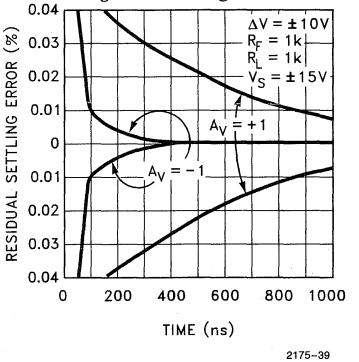
2175-37

8-Pin Package Power Dissipation vs Ambient Termperature



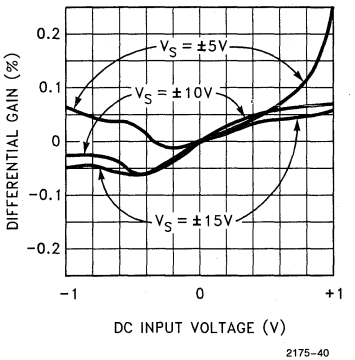
2175-38

Long Term Settling Error



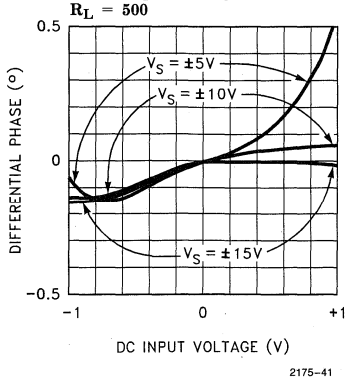
2175-39

Differential Gain vs DC Input Voltage R_L = 150



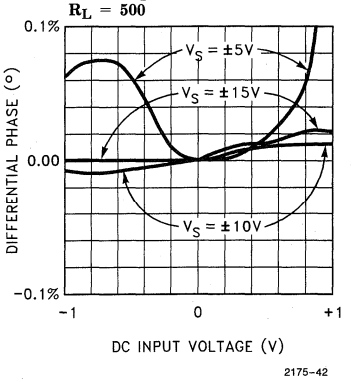
2175-40

Differential Phase vs DC Input Voltage R_L = 500



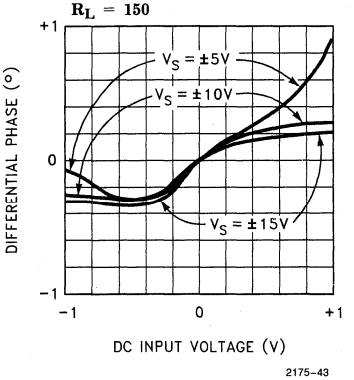
2175-41

Differential Gain vs DC Input Voltage R_L = 500



2175-42

Differential Phase vs DC Input Voltage R_L = 150



2175-43

Applications Information

Product Description

The EL2175 is a single current mode feedback amplifier that offers wide bandwidth, high gain, low distortion and exceptional DC specifications for a CMF type amplifier at moderate supply current. Due to the current feedback architecture, the closed loop 3 dB bandwidth is dependent on the feedback resistor, R_F, and then the gain is set by picking the gain set resistor, R_G. The curves at the beginning of the "Typical Performance Curves" section show the effect of varying both R_F and R_G. The 3 dB bandwidth is significantly less dependent on supply voltage than earlier CMF amplifiers where increasing junction capacitance's with decreasing supply voltage caused a much larger reduction in bandwidth. To compensate for the remaining effect, smaller values of feedback resistor can be used at lower supply voltages.

Power Supply Bypassing And Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible, below $\frac{1}{4}$". The power supply pins must be well bypassed to ensure stability. A 1.0 μF tantalum capacitor in parallel with a 0.01 μF ceramic capacitor is adequate for each supply pin.

For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input (see Capacitance at the Inverting Input section). This implies keeping the ground plane away from this pin. Carbon resistors are acceptable, while wire-wound resistors should not be used because of their parasitic inductance. Similarly, capacitors should have low inductance for best performance. Use of sockets, particularly for SO packages, should be avoided. Sockets have parasitic inductance and capacitance which will cause peaking and overshoot.

Capacitance at the Inverting Input

Due to the topology of the conventional current feedback amplifiers, stray capacitance at the inverting input will affect their AC and transient performance when operating in the non-inverting configuration. This may cause design, development and production difficulties. The EL2175 has been designed in such a way as to largely ignore such strays. The characteristic curves of gain vs. frequency with varying values of $C_{IN}-$ illustrate this effect which produces only a slight increase in peaking with $C_{IN}-$ values up to 5 pF with almost no change in 3 dB bandwidth.

In the inverting gain mode, added capacitance at the inverting input has almost no effect at all. This is because the inverting input is now a virtual ground and the stray capacitance is not therefore "seen" by the amplifier.

Feedback Resistor Values

The EL2175 has been designed and specified with $R_F = 750\Omega$ for $A_V = +2$. This value of feedback resistor yields an extremely flat frequency response with little or no peaking out to 120 MHz. As is the case with all CMF amplifiers, wider bandwidth, at the expense of peaking, can be obtained by reducing the value of the feedback resistor. Inversely, larger values of feedback resistor will cause roll-off to occur at lower frequency. This dependence of bandwidth on feedback resistance value is not as pronounced with the EL2175 at low non-inverting gains as with other CMF amplifiers. However, it is at all other gain conditions. For example, the 3 dB bandwidth of the EL2175 connected for $A_V = -1$ and $R_F = 750\Omega$ is about 65 MHz. If R_F is reduced to 560Ω, the bandwidth increases to about 88 MHz. See "Typical Performance Curves" section which show 3 dB bandwidth and peaking vs. frequency for various feedback resistor, supply voltages and temperatures.

Bandwidth vs Temperature

The supply currents of many amplifiers and consequently their 3 dB bandwidths drop off significantly with increasing temperature. The EL2175 was designed to have nearly constant supply current over temperature resulting in a device with much less bandwidth vs. temperature sensitivity. With $V_S = +15V$ and $A_V = +2$, the bandwidth only varies from 123 MHz to 96 MHz over the entire die temperature range of $0°C < T < 150°C$.

EL2175C
120 MHz Precision Current Mode Feedback Amplifier

Applications Information — Contd.

Supply Voltage Range

The EL2175 has been designed to operate comfortably with supply voltages from ±5V to ±15V. AC characterization has been conducted down to supply voltages of ±3.5V. However, this low value will not allow the part to power up and function properly at the lowest portion of the part's operating temperature range (−40°C to +85°C). In general, bandwidth, slew rate and video characteristics will tend to improve with increasing supply voltages.

If a single supply is desired, values from +9V to +30V can be used as long as the input common mode range is not exceeded. When using a single supply, be sure to either 1) DC bias the inputs at an appropriate common mode voltage and AC couple the signal, or 2) ensure the driving signal is within the input common mode range of the EL2175.

Settling Characteristics

The EL2175 offers superb settling characteristics to 0.1%, typically 50 ns operating in inverting mode. The inverting 0.01% settling time is about 90 ns. The EL2175 is not slew rate limited, therefore step size up to ±10V gives approximately the same settling time. The high 30 MΩ transimpedance gain and low input referred offsets of the EL2175 will also bring the final settled output much closer to its ideal value than is possible with earlier CMF designs.

The non-inverting (A_V = +1) 0.1% settling time is about 70 ns. As can be seen from the Long Term Settling Error graph, for A_V = +1, there is approximately a 0.04% residual which tails away to 0.01% in about 900 ns. This is a thermal settling error caused by a power dissipation change in the input stage devices (before and after the voltage step). All other CMF amplifiers exhibit 0.01% thermal settling tails of several tens of microseconds under the same conditions. The input stage of the EL2175 has been designed to greatly reduce this effect. For A_V = −1, because the inverting input is then a virtual ground, this tail does not appear even in conventional CMF amplifiers since the input stage does not experience the large voltage change that it does in non-inverting mode.

Distortion Performance

The distortion performance of all high frequency amplifiers degrade with increasing frequency. The EL2175 is no exception. However, due to it's high transimpedance, it's distortion performance at a given frequency can be 10–14 dB better than other high speed amplifiers available.

Power Dissipation

The EL2175 combines both high speed and large output drive capability at a moderate supply current in very small packages. It is possible to exceed the maximum junction temperature allowed under certain supply voltage, temperature and loading conditions. To ensure that the EL2175 remains within it's absolute maximum ratings, the following discussion will help to avoid exceeding the maximum junction temperature.

The maximum power dissipation allowed in a package is determined by it's thermal resistance and the amount of temperature rise according to:

$$P_{DMAX} = (T_{JMAX} - T_{AMAX}) / \theta_{JA}$$

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage plus the power dissipated in the IC due to the load, or:

$$P_{DMAX} = N \times (2 \times V_S \times I_S + (V_S - V_{OUT}) \times V_{OUT} / R_L)$$

where N is the number of amplifiers per package, and I_S is the current per amplifier. (To be more accurate, the quiescent supply current flowing in the output driver transistor should be subtracted from the first term when the output is driving a load. That is to say, due to the class AB nature of the output stage, the output driver current is now included in the second term.) In general, an amplifier's AC performance degrades at higher temperatures and lower supply current. Unlike some amplifiers, the EL2175 and many other Elantec amplifiers maintain almost constant supply current over temperature so that the AC performance is not degraded as much at the upper end of the operating temperature range.

The EL2175 consumes typically 8.5 mA and a maximum of 10 mA. The worst case power in an amplifier operating from split supplies with a grounded load occurs when the output is between ground and half of one of it's supplies or, if it can't go that far due to drive limitations, at it's

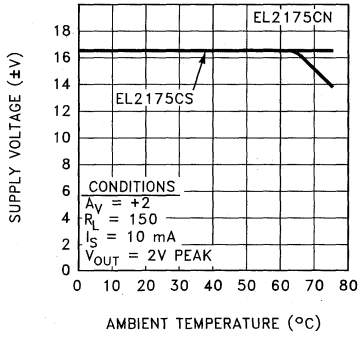
Applications Information — Contd.

maximum value. If we assume that the EL2175 is used for double terminate video cable driving applications (R_L = 150Ω), and A_V = +2, then the maximum output voltage is 2V, and the average output voltage is 1.4V. If we set the two P_{DMAX} equations equal to each other, and solve for V_S, we get a family of curves for various package options according to:

$$V_S = \frac{R_L \times (T_{JMAX} - T_{AMAX}) / N \times \theta_{JA} + (V_{OUT}) \times (V_{OUT})}{(2 \times I_S \times R_L) + (V_{OUT})}$$

The following curve shows supply voltage ($\pm V_S$) vs. temperature for the EL2175's two packages, assuming A_V = +2, R_L = 150Ω, and V_{OUT} (peak) = 2V. the curves include the worst case supply specification (I_S = 10 mA)

Supply Voltage vs Ambient Temperature



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The curves do not include heat removal or forcing air, or the simple fact that the package will probably be attached to a circuit board, which can also provide some form of heat removal. Larger temperature and voltage ranges are possible with heat removal and forcing air past the device.

Output Current Drive

The EL2175 does not have output short circuit protection. If the output is shorted to ground, the power dissipation could be well over 1W. Heat removal is required in order for the EL2175 to survive a continuous short.

Driving Cables And Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For these applications, the back termination series resistor will decouple the EL2175 from the capacitive cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without termination resistors. The EL2175 has particularly high capacitive load toleration and can drive a 50 pF load with only 3 dB of peaking and a 100 pF load with only 4 dB of peaking and without any instability. If higher capacitive loads must be driven or if little or no peaking is required, an additional small value (5Ω–50Ω) resistor can be placed in series with the output. The gain resistor, R_G, can be chosen to make up for the gain loss created by this additional series resistance at the output.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2176C/EL2276C

70 MHz/1 mA Current Mode Feedback Amp w/Disable

Features

- Single (EL2176C) and dual (EL2276C) topologies
- 1 mA supply current (per amplifier)
- 70 MHz −3 dB bandwidth
- Low cost
- Fast disable
- Powers down to 0 mA
- Single- and dual-supply operation down to ±1.5V
- 0.15%/0.15° diff. gain/diff. phase into 150Ω
- 800V/μs slew rate
- Large output drive current:
  100 mA (EL2176C)
  55 mA (EL2276C)
- Also available without disable in single (EL2170C), dual (EL2270C) and quad (EL2470C)
- Higher speed EL2180C/EL2186C family also available (3 mA/250 MHz) in single, dual and quad

Applications

- Low power/battery applications
- HDSL amplifiers
- Video amplifiers
- Cable drivers
- RGB amplifiers
- Test equipment amplifiers
- Current to voltage converters

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2176CN	−40°C to +85°C	8-Pin PDIP	MDP0031
EL2176CS	−40°C to +85°C	8-Pin SOIC	MDP0027
EL2276CN	−40°C to +85°C	14-Pin PDIP	MDP0031
EL2276CS	−40°C to +85°C	14-Pin SOIC	MDP0027

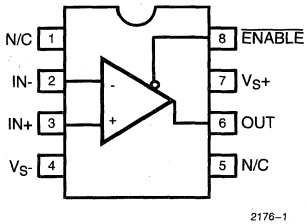
General Description

The EL2176C/EL2276C are single/dual current-feedback operational amplifiers which achieve a −3 dB bandwidth of 70 MHz at a gain of +1 while consuming only 1 mA of supply current per amplifier. They will operate with dual supplies ranging from ±1.5V to ±6V, or from single supplies ranging from +3V to +12V. The EL2176C/EL2276C also include a disable/power-down feature which reduces current consumption to 0 mA while placing the amplifier output in a high impedance state. In spite of its low supply current, the EL2276C can output 55 mA while swinging to ±4V on ±5V supplies. The EL2176C can output 100 mA with similar output swings. These attributes make the EL2176C/EL2276C excellent choices for low power and/or low voltage cable-driver, HDSL, or RGB applications.

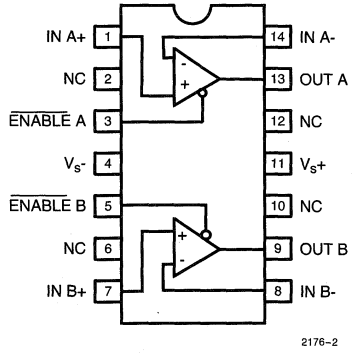
For Single, Dual and Quad applications without disable, consider the EL2170C (8-Pin Single), EL2270C (8-Pin Dual) or EL2470C (14-Pin Quad). For higher bandwidth applications where low power is still a concern, consider the EL2180C/El2186C family which also comes in similar Single, Dual and Quad configurations. The EL2180C/EL2186C family provides a −3 dB bandwidth of 250 MHz while consuming 3 mA of supply current per amplifier.

Connection Diagrams

EL2176C SO, P-DIP



EL2276C SO, P-DIP



EL2176C/EL2276C
70 MHz/1 mA Current Mode Feedback Amp w/Disable

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_{S+} and V_{S-}	+12.6V	Operating Junction Temperature	
Common-Mode Input Voltage	V_{S-} to V_{S+}	Plastic Packages	150°C
Differential Input Voltage	±6V	Output Current (EL2176C)	±120 mA
Current into +IN or −IN	±7.5 mA	Output Current (EL2276C)	±60 mA
Internal Power Dissipation	See Curves	Storage Temperature Range	−65°C to +150°C
Operating Ambient Temperature Range	−40°C to +85°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

V_S = ±5V, R_L = 150Ω, $\overline{ENABLE}$ = 0V, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage			2.5	15	I	mV
TCV_{OS}	Average Input Offset Voltage Drift	Measured from T_{MIN} to T_{MAX}		5		V	µV/°C
dV_{OS}	V_{OS} Matching	EL2276C only		0.5		V	mV
$+I_{IN}$	+ Input Current			0.5	5	I	µA
$d+I_{IN}$	$+I_{IN}$ Matching	EL2276C only		20		V	nA
$-I_{IN}$	− Input Current			4	10	I	µA
$d-I_{IN}$	$-I_{IN}$ Matching	EL2276C only		1.5		V	µA
CMRR	Common Mode Rejection Ratio	V_{CM} = ±3.5 V	45	50		I	dB
−ICMR	− Input Current Common Mode Rejection	V_{CM} = ±3.5V		4	10	I	µA/V
PSRR	Power Supply Rejection Ratio	V_S is moved from ±4V to ±6V	60	70		I	dB
−IPSR	− Input Current Power Supply Rejection	V_S is moved from ±4V to ±6V		0.5	5	I	µA/V
R_{OL}	Transimpedance	V_{OUT} = ±2.5V	200	400		I	kΩ
$+R_{IN}$	+ Input Resistance	V_{CM} = ±3.5V	1	4		I	MΩ
$+C_{IN}$	+ Input Capacitance			1.2		V	pF
CMIR	Common Mode Input Range		±3.5	±4.0		I	V

EL2176C/EL2276C
70 MHz/1 mA Current Mode Feedback Amp w/Disable

DC Electrical Characteristics — Contd.

V_S = ±5V, R_L = 150Ω, $\overline{ENABLE}$ = 0V, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_O	Output Voltage Swing	V_S = ±5	±3.5	±4.0		I	V
		V_S = +5 Single-Supply, High		4.0		V	V
		V_S = +5 Single-Supply, Low		0.3		V	V
I_O	Output Current	EL2176C only	80	100		I	mA
		EL2276C only, per Amplifier	50	55		I	mA
I_S	Supply Current	$\overline{ENABLE}$ = 2.0V, per Amplifier		1	2	I	mA
$I_{S(DIS)}$	Supply Current (Disabled)	$\overline{ENABLE}$ = 4.5V		0	20	I	µA
$C_{OUT(DIS)}$	Output Capacitance (Disabled)	$\overline{ENABLE}$ = 4.5V		4.4		V	pF
R_{EN}	Enable Pin Input Resistance	Measured at $\overline{ENABLE}$ = 2.0V, 4.5V	45	85		I	kΩ
I_{IH}	Logic "1" Input Current	Measured at $\overline{ENABLE}$, $\overline{ENABLE}$ = 4.5V		−0.04		V	µA
I_{IL}	Logic "0" Input Current	Measured at $\overline{ENABLE}$, $\overline{ENABLE}$ = 0V		−53		V	µA
V_{DIS}	Minimum Voltage at $\overline{ENABLE}$ to Disable		4.5			I	V
V_{EN}	Maximum Voltage at $\overline{ENABLE}$ to Enable				2.0	I	V

AC Electrical Characteristics

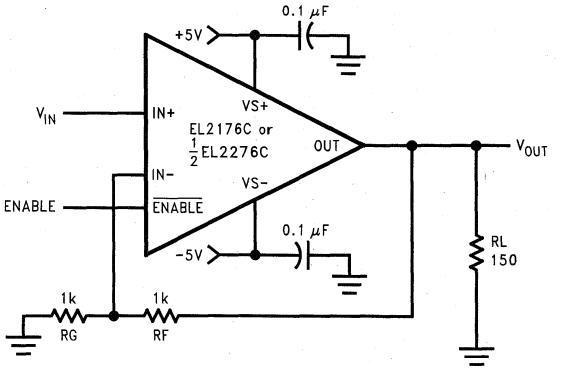
V_S = ±5V, R_F = R_G = 1.0 kΩ, R_L = 150Ω, $\overline{ENABLE}$ = 0V, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
−3 dB BW	−3 dB Bandwidth	A_V = +1		70		V	MHz
−3 dB BW	−3 dB Bandwidth	A_V = +2		60		V	MHz
SR	Slew Rate	V_{OUT} = ±2.5V, A_V = +2	400	800		IV	V/µs
t_r, t_f	Rise and Fall Time	V_{OUT} = ±500 mV		4.5		V	ns
t_{pd}	Propagation Delay	V_{OUT} = ±500 mV		4.5		V	ns
OS	Overshoot	V_{OUT} = ±500 mV		3.0		V	%
ts	0.1% Settling	V_{OUT} = ±2.5V, A_V = −1		40		V	ns
dG	Differential Gain	A_V = +2, R_L = 150Ω (Note 1)		0.15		V	%
dP	Differential Phase	A_V = +2, R_L = 150Ω (Note 1)		0.15		V	°
dG	Differential Gain	A_V = +1, R_L = 500Ω (Note 1)		0.02		V	%
dP	Differential Phase	A_V = +1, R_L = 500Ω (Note 1)		0.01		V	°
t_{ON}	Turn-On Time	A_V = +2, V_{IN} = +1V, R_L = 150Ω (Note 2)		40	100	I	ns
t_{OFF}	Turn-Off Time	A_V = +2, V_{IN} = +1V, R_L = 150Ω (Note 2)		500	1000	I	ns
CS	Channel Separation	EL2276C only, f = 5 MHz		85		V	dB

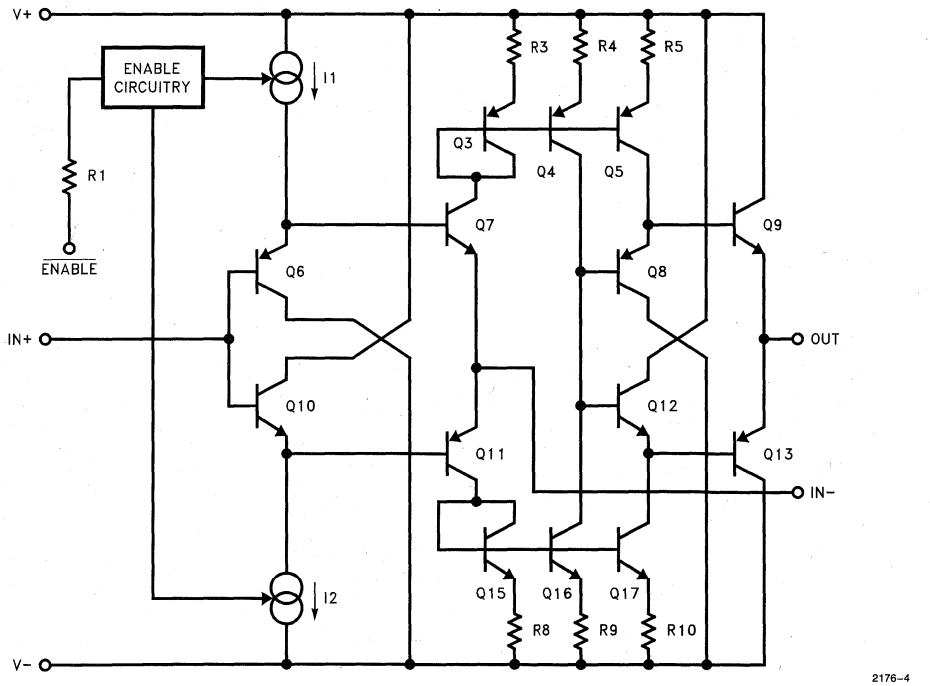
Note 1: DC offset from 0V to 0.714V, AC amplitude 286 mV_{P-P}, f = 3.58 MHz.

Note 2: Measured from the application of the logic signal until the output voltage is at the 50% point between initial and final values.

Test Circuit (per Amplifier)



Simplified Schematic (per Amplifer)

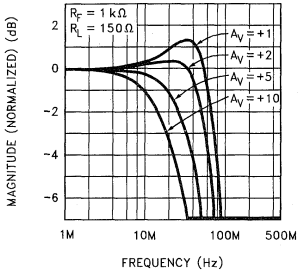


EL2176C/EL2276C

70 MHz/1 mA Current Mode Feedback Amp w/Disable

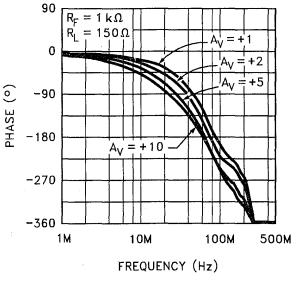
Typical Performance Curves

Non-Inverting Frequency Response (Gain)



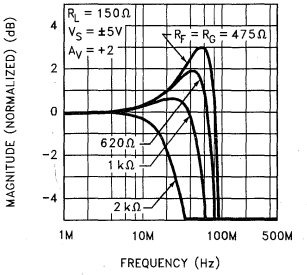
2176-5

Non-Inverting Frequency Response (Phase)



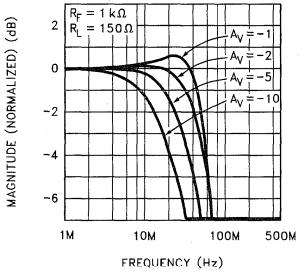
2176-6

Frequency Response for Various R_F and R_G



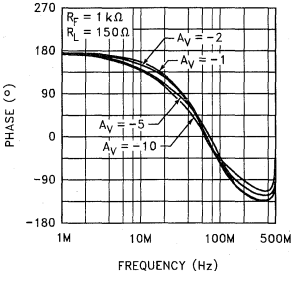
2176-7

Inverting Frequency Response (Gain)



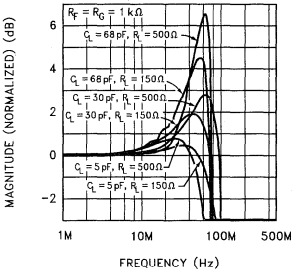
2176-8

Inverting Frequency Response (Phase)



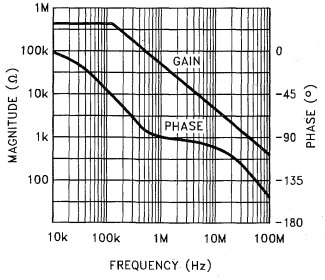
2176-9

Frequency Response for Various R_L and C_L



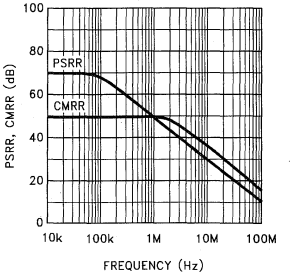
2176-10

Transimpedance (R_{OL})



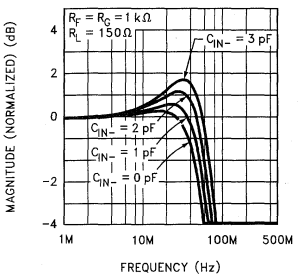
2176-11

PSRR and CMRR



2176-12

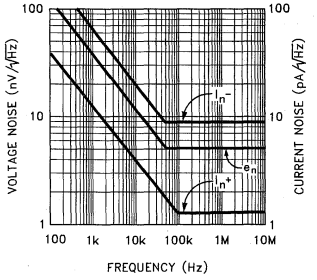
Frequency Response for Various C_{IN-}



2176-13

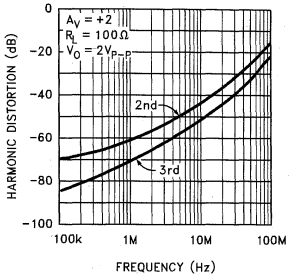
Typical Performance Curves — Contd.

Voltage and Current Noise vs Frequency



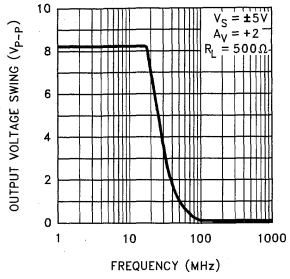
2176-14

2nd and 3rd Harmonic Distortion vs Frequency



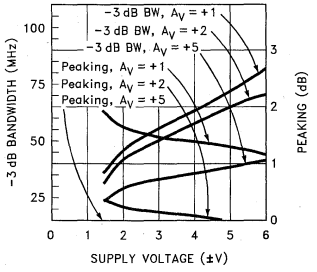
2176-15

Output Voltage vs Frequency



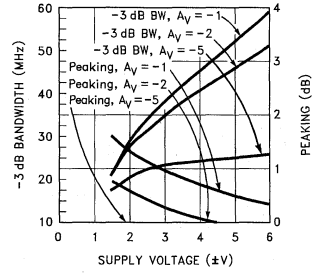
2176-16

−3 dB Bandwith and Peaking vs Supply Voltage for Various Non-Inverting Gains



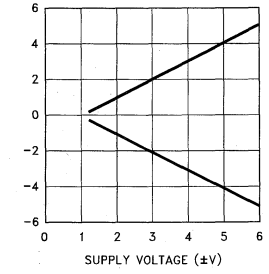
2176-17

−3 dB Bandwith and Peaking vs Supply Voltage for Various Inverting Gains



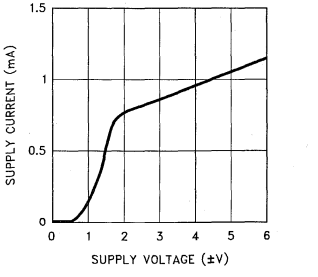
2176-18

Output Voltage Swing vs Supply Voltage



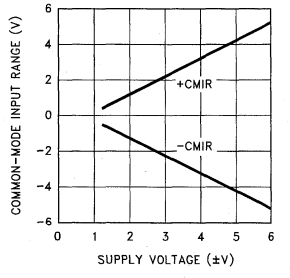
2176-19

Supply Current vs Supply Voltage



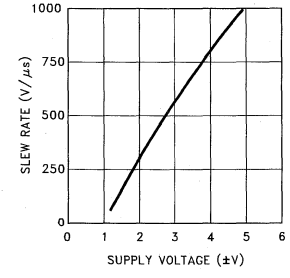
2176-20

Common-Mode Input Range vs Supply Voltage



2176-21

Slew Rate vs Supply Voltage

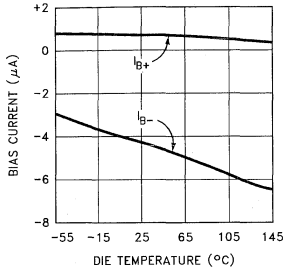


2176-22

EL2176C/EL2276C
70 MHz/1 mA Current Mode Feedback Amp w/Disable

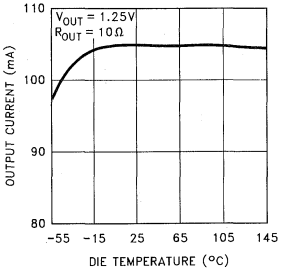
Typical Performance Curves — Contd.

Input Bias Current vs Die Temperature



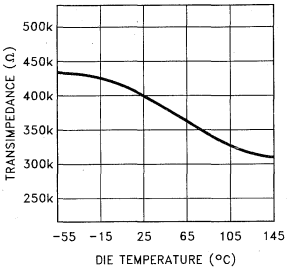
2176-23

Short-Circuit Current vs Die Temperature



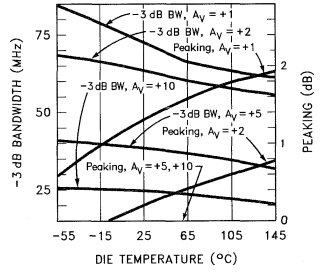
2176-24

Transimpedance (R_{OL}) vs Die Temperature



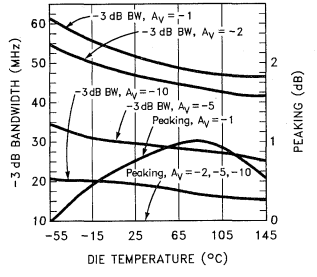
2176-25

−3 dB Bandwith and Peaking vs Die Temperature for Various Non-Inverting Gains



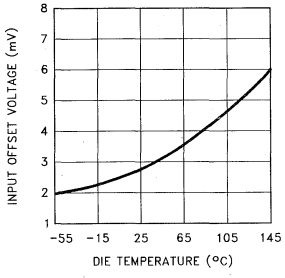
2176-26

−3 dB Bandwith and Peaking vs Die Temperature for Various Inverting Gains



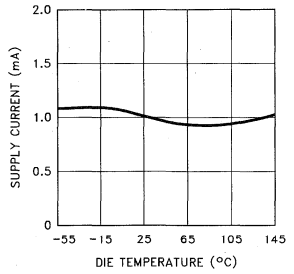
2176-27

Input Offset Voltage vs Die Temperature



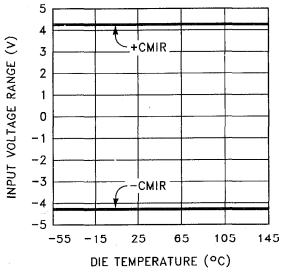
2176-28

Supply Current vs Die Temperature



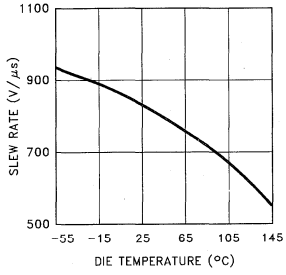
2176-29

Input Voltage Range vs Die Temperature



2176-30

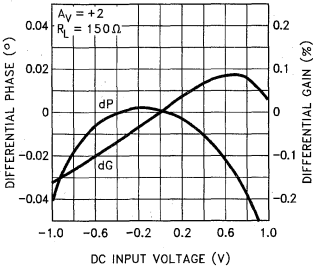
Slew Rate vs Die Temperature



2176-31

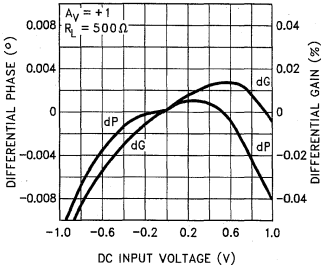
Typical Performance Curves — Contd.

Differential Gain and Phase vs DC Input Voltage at 3.58 MHz/A_V = +2



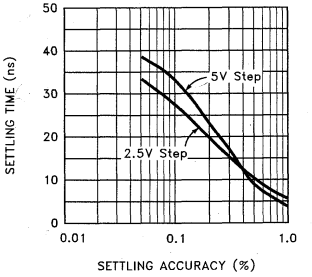
2176-32

Differential Gain and Phase vs DC Input Offset at 3.58 MHz/A_V = +1



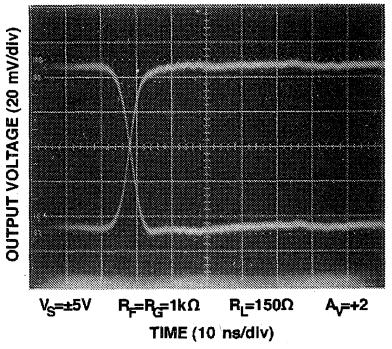
2176-33

Settling Time vs Settling Accuracy



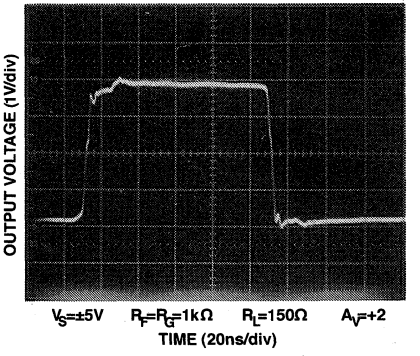
2176-34

Small-Signal Step Response



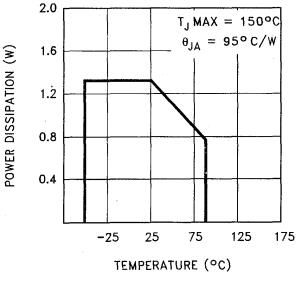
2176-35

Large-Signal Step Response



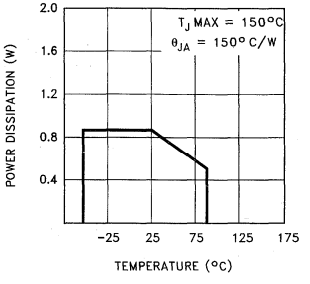
2176-36

8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



2176-37

8-Lead SO Maximum Power Dissipation vs Ambient Temperature

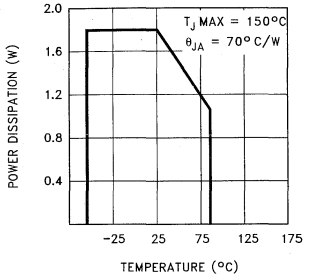


2176-38

EL2176C/EL2276C
70 MHz/1 mA Current Mode Feedback Amp w/Disable

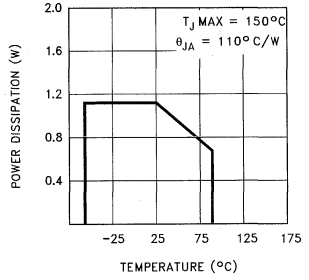
Typical Performance Curves — Contd.

14-Pin Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



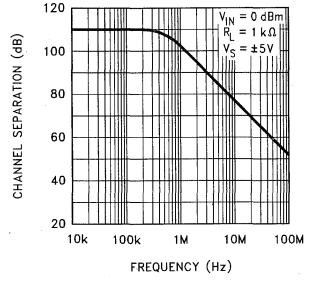
2176-39

14-Lead SO
Maximum Power Dissipation
vs Ambient Temperature



2176-40

Channel Separation
vs Frequency



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Applications Information

Product Description

The EL2176C/EL2276C are current-feedback operational amplifiers that offer a wide −3 dB bandwidth of 70 MHz, a low supply current of 1 mA per amplifier and the ability to disable to 0 mA. Both products also feature high output current drive. The EL2176C can output 100 mA, while the EL2276C can output 55 mA per amplifier. The EL2176C/EL2276C work with supply voltages ranging from a single 3V to ±6V, and they are also capable of swinging to with in 1V of either supply on the input and the output. Because of their current-feedback topology, the EL2176C/EL2276C do not have the normal gain-bandwidth product associated with voltage-feedback operational amplifiers. This allows their −3 dB bandwidth to remain relatively constant as closed-loop gain is increased. This combination of high bandwidth and low power, together with aggressive pricing make the EL2176C/EL2276C the ideal choice for many low-power/high-bandwidth applications such as portable computing, HDSL, and video processing.

For Single, Dual and Quad applications without disable, consider the EL2170C (8-Pin Single), EL2270C (8-Pin Dual) and EL2470C (14-Pin Quad). If more AC performance is required, refer to the EL2180C/EL2186C family which provides Singles, Duals, and Quads with 250 MHz of bandwidth while consuming 3 mA of supply current per amplifier.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7 μF tantalum capacitor in parallel with a 0.1 μF capacitor has been shown to work well when placed at each supply pin.

For good AC performance, parasitic capacitance should be kept to a minimum especially at the inverting input (see the Capacitance at the Inverting Input section). Ground plane construction should be used, but it should be removed from the area near the inverting input to minimize any stray capacitance at that node. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of their additional series inductance. Use of sockets, particularly for the SO package should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

Disable/Power-Down

The EL2176C/EL2276C amplifiers can be disabled, placing their output in a high-impedance state. When disabled, each amplifier's supply current is reduced to 0 mA. Each EL2176C/EL2276C amplifier is disabled when its $\overline{\text{ENABLE}}$ pin is floating or pulled up to within 0.5V of the positive supply. Similarly, each amplifier is enabled by pulling its $\overline{\text{ENABLE}}$ pin at least 3V below the positive supply. For ±5V supplies, this means that an EL2176C/EL2276C amplifier will be enabled when $\overline{\text{ENABLE}}$ is at 2V or less, and disabled when $\overline{\text{ENABLE}}$ is above 4.5V. Although the logic levels are not standard TTL, this choice of logic voltages allows the EL2176C/EL2276C to be enabled by tying $\overline{\text{ENABLE}}$ to ground, even in +3V single-supply applications. The $\overline{\text{ENABLE}}$ pin can be driven from CMOS outputs or open-collector TTL.

When enabled, supply current does vary somewhat with the voltage applied at $\overline{\text{ENABLE}}$. For example, with the supply voltages of the EL2176C at ±5V, if $\overline{\text{ENABLE}}$ is tied to −5V (rather than ground) the supply current will increase about 15% to 1.15 mA.

Capacitance at the Inverting Input

Any manufacturer's high-speed voltage- or current-feedback amplifier can be affected by stray capacitance at the inverting input. For inverting gains this parasitic capacitance has little effect because the inverting input is a virtual ground, but for non-inverting gains this capacitance (in conjunction with the feedback and gain resistors) creates a pole in the feedback path of the amplifier. This pole, if low enough in frequency, has the same destabilizing effect as a zero in the forward open-loop response. The use of large value feed-

EL2176C/EL2276C
70 MHz/1 mA Current Mode Feedback Amp w/Disable

Applications Information — Contd.

back and gain resistors further exacerbates the problem by further lowering the pole frequency.

The EL2176C/EL2276C have been specially designed to reduce power dissipation in the feedback network by using large 1.0 kΩ feedback and gain resistors. With the high bandwidths of these amplifiers, these large resistor values would normally cause stability problems when combined with parasitic capacitance, but by internally canceling the effects of a nominal amount of parasitic capacitance, the EL2176C/EL2276C remain very stable. For less experienced users, this feature makes the EL2176C/EL2276C much more forgiving, and therefore easier to use than other products not incorporating this proprietary circuitry.

The experienced user with a large amount of PC board layout experience may find in rare cases that the EL2176C/EL2276 C have less bandwidth than expected. In this case, the inverting input may have less parasitic capacitance than expected by the internal compensation circuitry of the EL2176C/EL2276C. The reduction of feedback resistor values (or the addition of a very small amount of external capacitance at the inverting input, e.g., 0.5 pF) will increase bandwidth as desired. Please see the curves for Frequency Response for Various R_F and R_G, and Frequency Response for Various $C_{IN}-$.

Feedback Resistor Values

The EL2176C/EL2276C have been designed and specified at gains of +1 and +2 with R_F = 1.0 kΩ. This value of feedback resistor gives 70 MHz of −3 dB bandwidth at A_V = +1 with about 1.5 dB of peaking, and 60 MHz of −3 dB bandwidth at A_V = +2 with about 0.5 dB of peaking. Since the EL2176C/EL2276C are current-feedback amplifiers, it is also possible to change the value of R_F to get more bandwidth. As seen in the curve of Frequency Response For Various R_F and R_G, bandwidth and peaking can be easily modified by varying the value of the feedback resistor.

Because the EL2176C is a current-feedback amplifier, the gain-bandwidth product is not a constant for different closed-loop gains. This feature actually allows the EL2176C/EL2276C to maintain about the same −3 dB bandwidth, regardless of closed-loop gain. However, as closed-loop gain is increased, bandwidth decreases slightly while stability increases.

Since the loop stability is improving with higher closed-loop gains, it becomes possible to reduce the value of R_F below the specified 1.0 kΩ and still retain stability, resulting in only a slight loss of bandwidth with increased closed-loop gain.

Supply Voltage Range and Single-Supply Operation

The EL2176C/EL2276C have been designed to operate with supply voltages having a span of greater than 3V, and less than 12V. In practical terms, this means that the EL2176C/EL2276C will operate on dual supplies ranging from ±1.5V to ±6V. With a single-supply, the EL2176C will operate from +3V to +12V.

As supply voltages continue to decrease, it becomes necessary to provide input and output voltage ranges that can get as close as possible to the supply voltages. The EL2176C/EL2276C have an input voltage range that extends to within 1V of either supply. So, for example, on a single +5V supply, the EL2176C/EL2276C have an input range which spans from 1V to 4V. The output range of the EL2176C /EL2276C is also quite large, extending to within 1V of the supply rail. On a ±5V supply, the output is therefore capable of swinging from −4V to +4V. Single-supply output range is even larger because of the increased negative swing due to the external pull-down resistor to ground. On a single +5V supply, output voltage range is about 0.3V to 4V.

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This is especially difficult when driving a standard video load of 150Ω, because of the change in output current with DC level. Until the EL2176C/EL2276C, good Differential Gain could only be achieved by running high idle currents through the output transistors (to reduce variations in output impedance). These currents were typically in excess of the

Applications Information — Contd.

entire 1 mA supply current of each EL2176C/EL2276C amplifier! Special circuitry has been incorporated in the EL2176C/EL2276C to reduce the variation of output impedance with current output. This results in dG and dP specifications of 0.15% and 0.15° while driving 150Ω at a gain of +2.

Video Performance has also been measured with a 500Ω load at a gain of +1. Under these conditions, the EL2176C/EL2276C have dG and dP specifications of 0.01% and 0.02° respectively while driving 500Ω at $A_V = +1$.

Output Drive Capability

In spite of its low 1 mA of supply current, the EL2176C is capable of providing a minimum of ±80 mA of output current. Similarly, each amplifier of the EL2276C is capable of providing a minimum of ±50 mA. These output drive levels are unprecedented in amplifiers running at these supply currents. With a minimum ±80 mA of output drive, the EL2176C is capable of driving 50Ω loads to ±4V, making it an excellent choice for driving isolation transformers in telecommunications applications. Similarly, the ±50 mA minimum output drive of each EL2276C amplifier allows swings of ±2.5V into 50Ω loads.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will decouple the EL2176C/EL2276C from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output to eliminate most peaking. The gain resistor (R_G) can then be chosen to make up for any gain loss which may be created by this additional resistor at the output. In many cases it is also possible to simply increase the value of the feedback resistor (R_F) to reduce the peaking.

Current Limiting

The EL2176C/EL2276C have no internal current-limiting circuitry. If any output is shorted, it is possible to exceed the Absolute Maximum Ratings for output current or power dissipation, potentially resulting in the destruction of the device.

Power Dissipation

With the high output drive capability of the EL2176C/EL2276C, it is possible to exceed the 150°C Absolute Maximum junction temperature under certain very high load current conditions. Generally speaking, when R_L falls below about 25Ω, it is important to calculate the maximum junction temperatu re (T_{Jmax}) for the application to determine if power-supply voltages, load conditions, or package type need to be modified for the EL2176C/EL2276C to remain in the safe operating area. These parameters are calculated as follows:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} * n * PD_{MAX}) \quad [1]$$

where:

T_{MAX} = Maximum Ambient Temperature
θ_{JA} = Thermal Resistance of the Package
n = Number of Amplifiers in the Package
PD_{MAX} = Maximum Power Dissipation of Each Amplifier in the Package.

PD_{MAX} for each amplifier can be calculated as follows:

$$PD_{MAX} = (2 * V_S * I_{SMAX}) + (V_S - V_{OUTMAX}) * (V_{OUTMAX}/R_L)) \quad [2]$$

where:

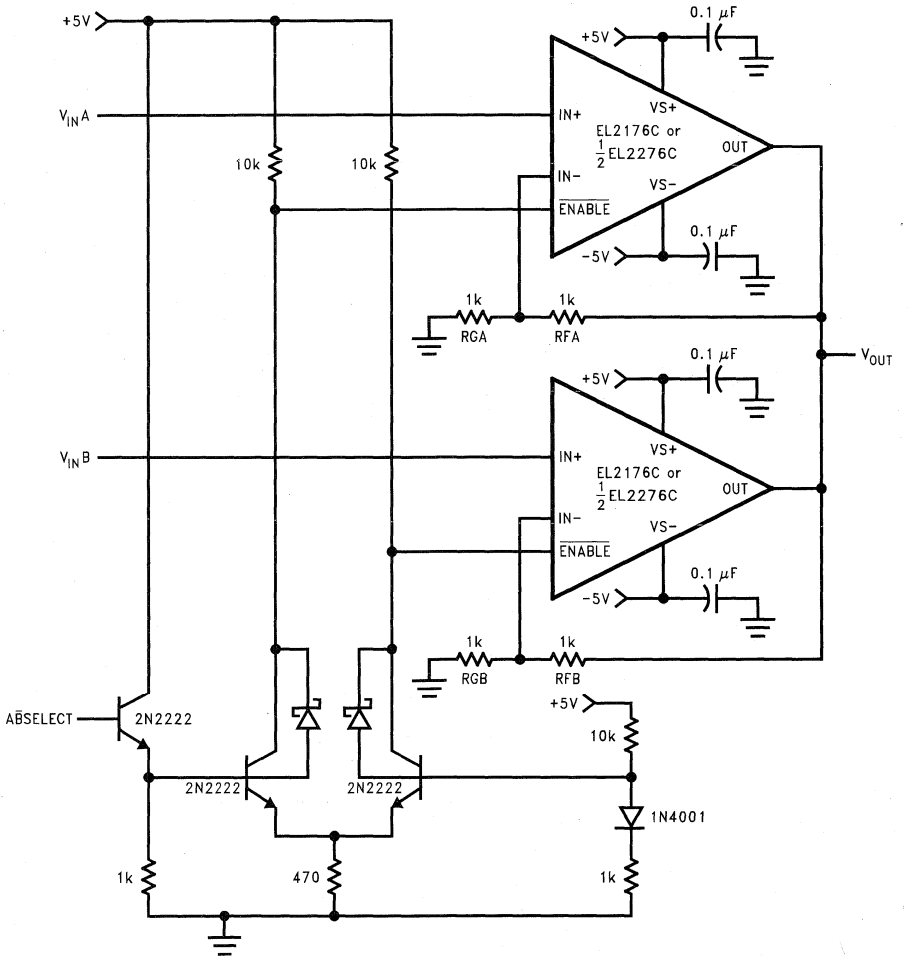
V_S = Supply Voltage
I_{SMAX} = Maximum Supply Current of 1 Amplifier
V_{OUTMAX} = Max. Output Voltage of the Application
R_L = Load Resistance

EL2176C/EL2276C

70 MHz/1 mA Current Mode Feedback Amp w/Disable

Typical Application Circuits

Low Power Multiplexer with Single-Ended TTL Input



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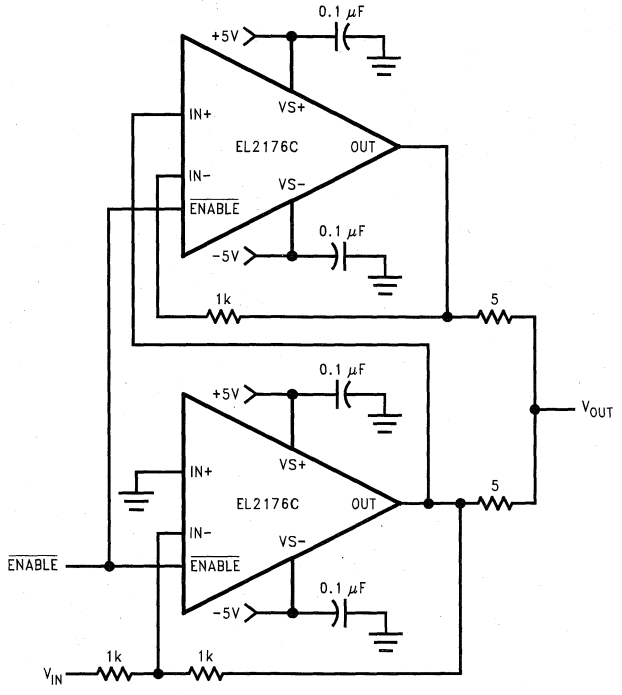
Typical Application Circuits — Contd.

Inverting 200 mA Output Current Distribution Amplifier



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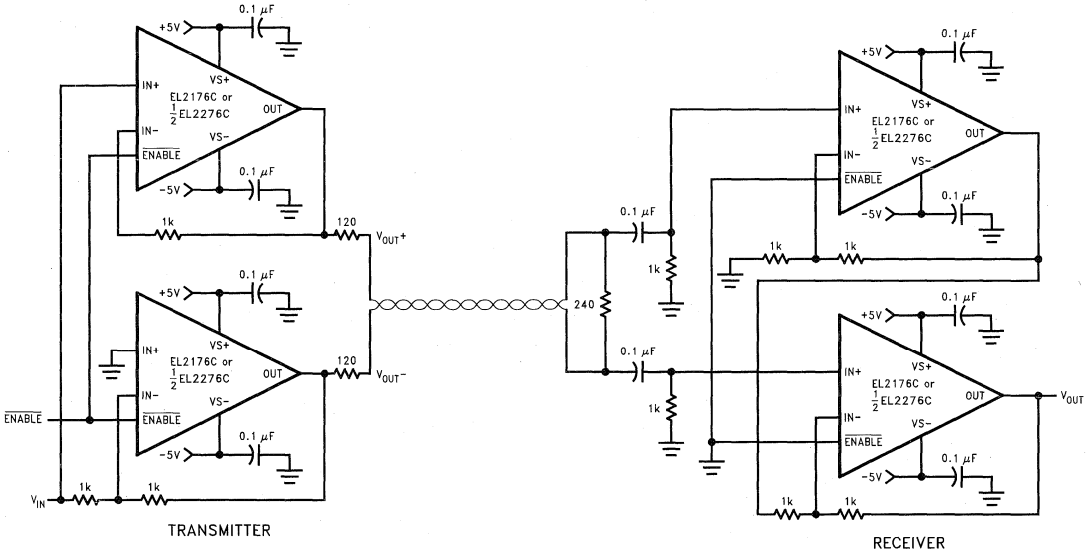
EL2176C/EL2276C
70 MHz/1 mA Current Mode Feedback Amp w/Disable

Typical Application Circuits — Contd.

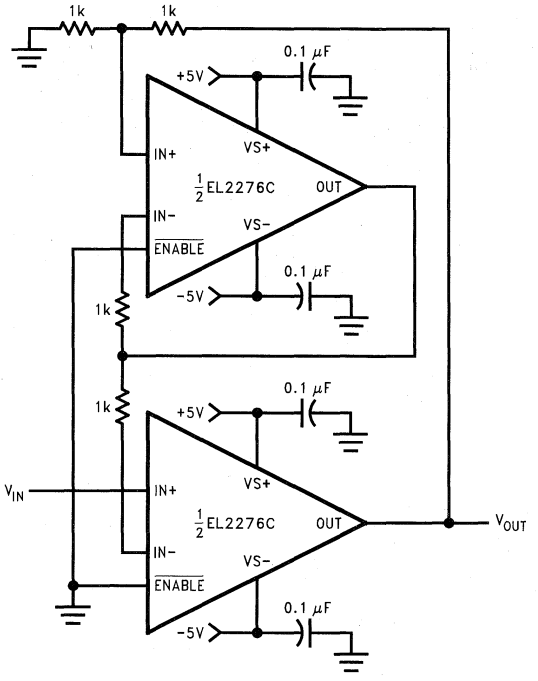
Differential Line-Driver/Receiver



2176-44

Typical Application Circuits — Contd.

Fast-Settling Precision Amplifier



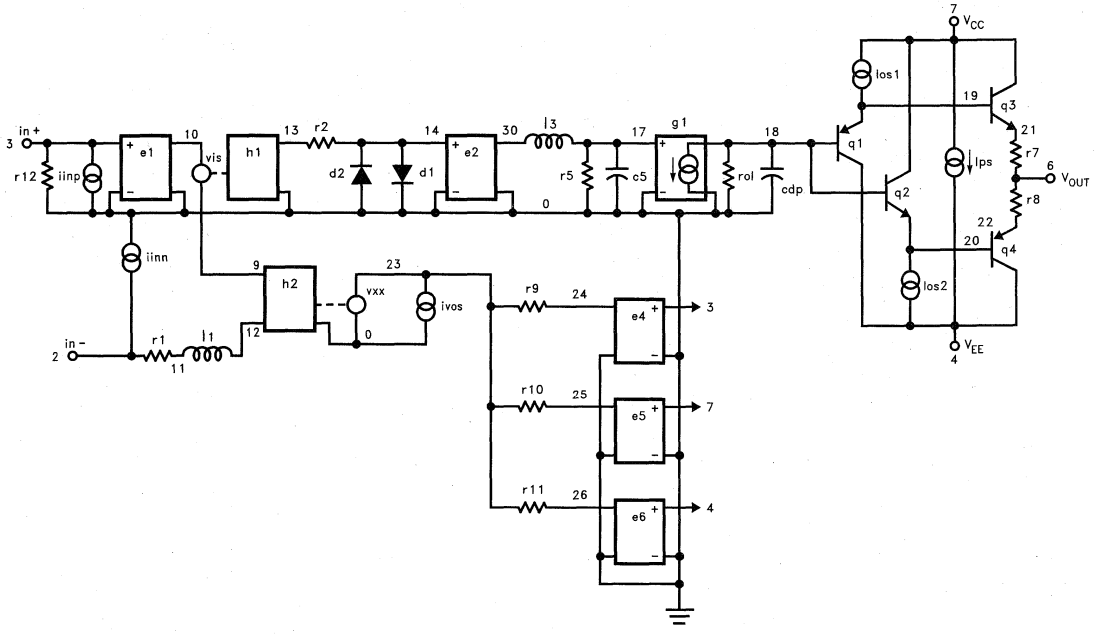
2176-45

EL2176C/EL2276C
70 MHz/1 mA Current Mode Feedback Amp w/Disable

EL2176C/EL2276C Macromodel

```
* Revision A, March 1995
* AC characteristics used Rf = Rg = 1KΩ, RL = 150Ω
* Connections:      +input
*                   |    -input
*                   |    |    +Vsupply
*                   |    |    |    -Vsupply
*                   |    |    |    |    output
*                   |    |    |    |    |
.subckt EL2176/el    3    2    7    4    6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 165
l1 11 12 25nH
iinp 3 0 0.5uA
iinm 2 0 4uA
r12 3 0 4Meg
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
e2 30 0 14 0 0.00166666666
l3 30 17 0.5uH
c5 17 0 0.69pF
r5 17 0 300
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 400K
cdp 18 0 1.9pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 0.4mA
ios2 20 4 0.4mA
*
* Supply Current
*
ips 7 4 1nA
*
* Error Terms
*
ivos 0 23 2mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 -1. 0
r9 24 23 0.316K
r10 25 23 3.2K
r11 26 23 3.2K
*
* Models
*
.model qn npn(is = 5e-15 bf = 200 tf = 0.01nS)
.model qp pnp(is = 5e-15 bf = 200 tf = 0.01nS)
.model dclamp d(is = 1e-30 ibv = 0.266
+ bv = 1.3v n = 4)
.ends
```

EL2176C/EL2276C Macromodel — Contd.



2176-46

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2180C/EL2280C/EL2480C

250 MHz/3 mA Current Mode Feedback Amplifiers

Features

- Single (EL2180C), dual (EL2280C) and quad (EL2480C) topologies
- 3 mA supply current (per amplifier)
- 250 MHz −3 dB bandwidth
- Low cost
- Single- and dual-supply operation down to ±1.5V
- 0.05%/0.05° diff. gain/diff. phase into 150Ω
- 1200 V/μs slew rate
- Large output drive current:
  100 mA (EL2180C)
  55 mA (EL2280C)
  55 mA (EL2480C)
- Also available with disable in single (EL2186C) and dual (EL2286C)
- Lower power EL2170C/EL2176C family also available (1 mA/ 70 MHz) in single, dual and quad

Applications

- Low power/battery applications
- HDSL amplifiers
- Video amplifiers
- Cable drivers
- RGB amplifiers
- Test equipment amplifiers
- Current to voltage converters

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2180CN	−40°C to +85°C	8-Pin PDIP	MDP0031
EL2180CS	−40°C to +85°C	8-Pin SOIC	MDP0027
EL2280CN	−40°C to +85°C	8-Pin PDIP	MDP0031
EL2280CS	−40°C to +85°C	8-Pin SOIC	MDP0027
EL2480CN	−40°C to +85°C	14-Pin PDIP	MDP0031
EL2480CS	−40°C to +85°C	14-Pin SOIC	MDP0027

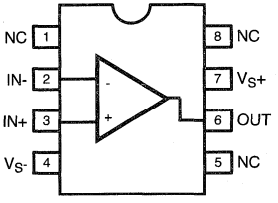
General Description

The EL2180C/EL2280C/EL2480C are single/dual/quad current-feedback operational amplifiers which achieve a −3 dB bandwidth of 250 MHz at a gain of +1 while consuming only 3 mA of supply current per amplifier. They will operate with dual supplies ranging from ±1.5V to ±6V, or from single supplies ranging from +3V to +12V. In spite of their low supply current, the EL2480C and the EL2280C can output 55 mA while swinging to ±4V on ±5V supplies. The EL2180C can output 100 mA with similar output swings. These attributes make the EL2180C/EL2280C/EL2480C excellent choices for low power and/or low voltage cable-driver, HDSL, or RGB applications.

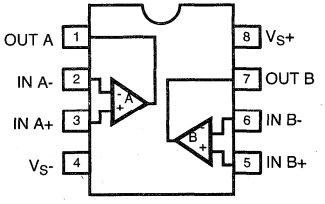
For Single and Dual applications with disable, consider the EL2186C (8-Pin Single) or EL2286C (14-Pin Dual). For lower power applications where speed is still a concern, consider the EL2170C/El2176C family which also comes in similar Single, Dual and Quad configurations. The EL2170C/EL2176C family provides a −3 dB bandwidth of 70 MHz while consuming 1 mA of supply current per amplifier.

Connection Diagrams

EL2180C SO, P-DIP

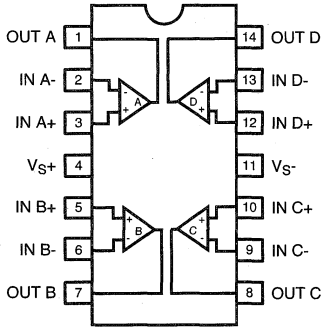


EL2280C SO, P-DIP



2180-1

EL2480C SO, P-DIP



2180-2

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_S+ and V_S-	+12.6V	Operating Junction Temperature	
Common-Mode Input Voltage	V_S- to V_S+	Plastic Packages	150°C
Differential Input Voltage	±6V	Output Current (EL2180C)	±120 mA
Current into +IN or −IN	±7.5 mA	Output Current (EL2280C)	±60 mA
Internal Power Dissipation	See Curves	Output Current (EL2480C)	±60 mA
Operating Ambient Temperature Range	−40°C to +85°C	Storage Temperature Range	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±5V, R_L = 150Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage			2.5	15	I	mV
TCV_{OS}	Average Input Offset Voltage Drift	Measured from T_{MIN} to T_{MAX}		5		V	µV/°C
dV_{OS}	V_{OS} Matching	EL2280C, EL2480C only		0.5		V	mV
$+I_{IN}$	+ Input Current			1.5	15	I	µA
$d+I_{IN}$	$+I_{IN}$ Matching	EL2280C, EL2480C only		20		V	nA
$-I_{IN}$	− Input Current			16	30	I	µA
$d-I_{IN}$	$-I_{IN}$ Matching	EL2280C, EL2480C only		2		V	µA
CMRR	Common Mode Rejection Ratio	V_{CM} = ±3.5V	45	50		I	dB
−ICMR	− Input Current Common Mode Rejection	V_{CM} = ±3.5V		5	30	I	µA/V
PSRR	Power Supply Rejection Ratio	V_S is moved from ±4V to ±6V	60	70		I	dB
−IPSR	− Input Current Power Supply Rejection	V_S is moved from ±4V to ±6V		1	15	I	µA/V
R_{OL}	Transimpedance	V_{OUT} = ±2.5V	150	300		I	kΩ
$+R_{IN}$	+ Input Resistance	V_{CM} = ±3.5V	0.5	2		I	MΩ
$+C_{IN}$	+ Input Capacitance			1.2		V	pF
CMIR	Common Mode Input Range		±3.5	±4.0		I	V

EL2180C/EL2280C/EL2480C
250 MHz/3 mA Current Mode Feedback Amplifiers

DC Electrical Characteristics — Contd.

$V_S = \pm 5V$, $R_L = 150\Omega$, $T_A = 25°C$ unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_O	Output Voltage Swing	$V_S = \pm 5$	± 3.5	± 4.0		I	V
		$V_S = +5$ Single-Supply, High		4.0		V	V
		$V_S = +5$ Single-Supply, Low		0.3		V	V
I_O	Output Current	EL2180C only	80	100		I	mA
		EL2280C only, per Amplifier	50	55		I	mA
		EL2480C only, per Amplifier	50	55		I	mA
I_S	Supply Current	Per Amplifier		3	6	I	mA

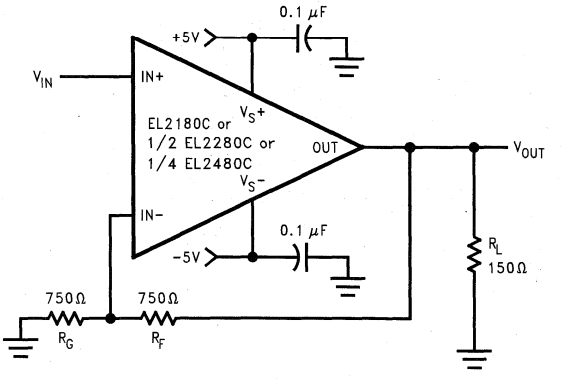
AC Electrical Characteristics

$V_S = \pm 5V$, $R_F = R_G = 750\Omega$, $R_L = 150\Omega$, $T_A = 25°C$ unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
−3 dB BW	−3 dB Bandwidth	$A_V = +1$		250		V	MHz
−3 dB BW	−3 dB Bandwidth	$A_V = +2$		180		V	MHz
0.1 dB BW	0.1 dB Bandwidth	$A_V = +2$		50		V	MHz
SR	Slew Rate	$V_{OUT} = \pm 2.5V$, $A_V = +2$	600	1200		IV	V/μs
t_r, t_f	Rise and Fall Time	$V_{OUT} = \pm 500$ mV		1.5		V	ns
t_{pd}	Propagation Delay	$V_{OUT} = \pm 500$ mV		1.5		V	ns
OS	Overshoot	$V_{OUT} = \pm 500$ mV		3.0		V	%
t_s	0.1% Settling	$V_{OUT} = \pm 2.5V$, $A_V = -1$		15		V	ns
dG	Differential Gain	$A_V = +2$, $R_L = 150\Omega$ (Note 1)		0.05		V	%
dP	Differential Phase	$A_V = +2$, $R_L = 150\Omega$ (Note 1)		0.05		V	°
dG	Differential Gain	$A_V = +1$, $R_L = 500\Omega$ (Note 1)		0.01		V	%
dP	Differential Phase	$A_V = +1$, $R_L = 500\Omega$ (Note 1)		0.01		V	°
C_S	Channel Separation	EL2280C, EL2480C only, f = 5 MHz		85		V	dB

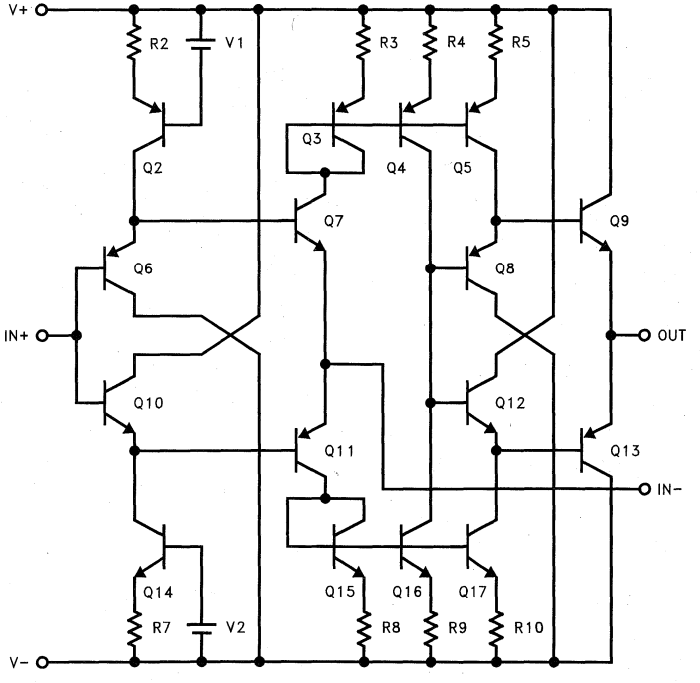
Note 1: DC offset from 0V to 0.714V, AC amplitude 286 mV_{P-P}, f = 3.58 MHz.

Test Circuit (per Amplifier)



2180-3

Simplified Schematic (per Amplifer)



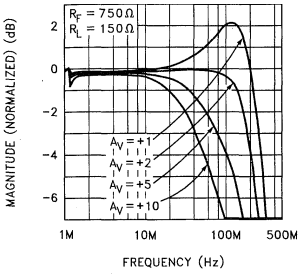
2180-4

EL2180C/EL2280C/EL2480C

250 MHz/3 mA Current Mode Feedback Amplifiers

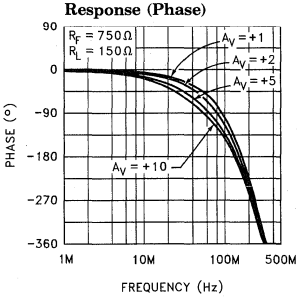
Typical Performance Curves

Non-Inverting Frequency Response (Gain)



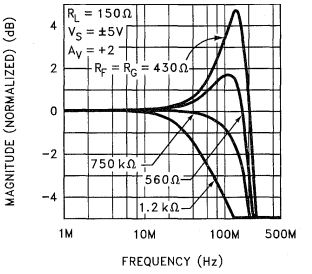
2180-5

Non-Inverting Frequency Response (Phase)



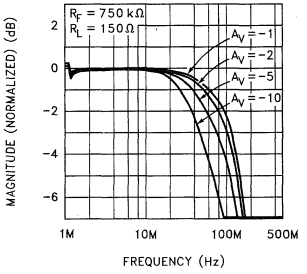
2180-6

Frequency Response for Various R_F and R_G



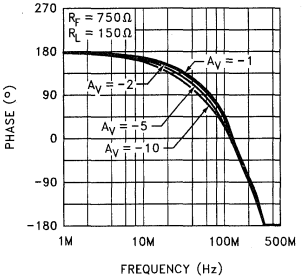
2180-7

Inverting Frequency Response (Gain)



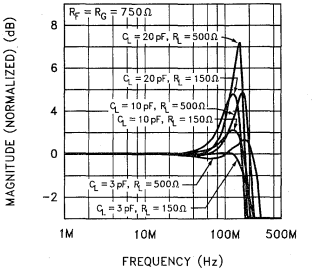
2180-8

Inverting Frequency Response (Phase)



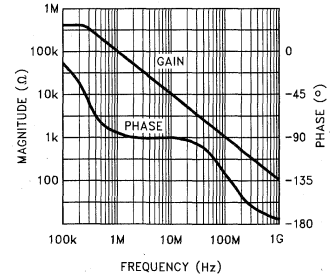
2180-9

Frequency Response for Various R_L and R_L



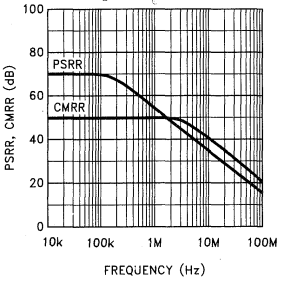
2180-10

Transimpedance (R_{OL}) vs Frequency



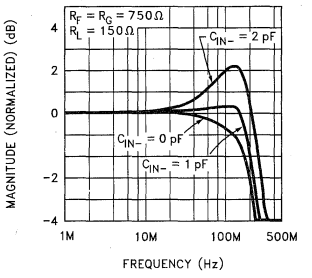
2180-11

PSRR and CMRR vs Frequency



2180-12

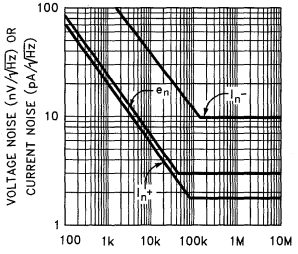
Frequency Response for Various C_{IN-}



2180-13

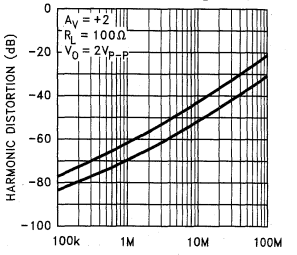
Typical Performance Curves — Contd.

Voltage and Current Noise vs Frequency



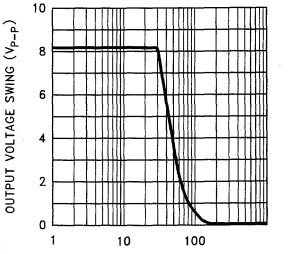
2180-14

2nd and 3rd Harmonic Distortion vs Frequency



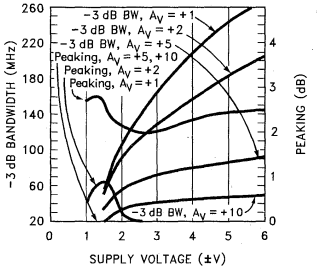
2180-15

Output Voltage Swing vs Frequency



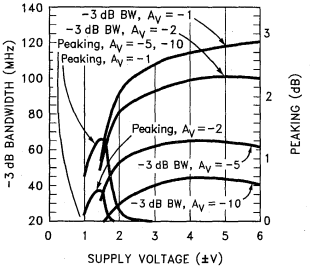
2180-16

−3 dB Bandwidth and Peaking vs Supply Voltage for Various Non-Inverting Gains



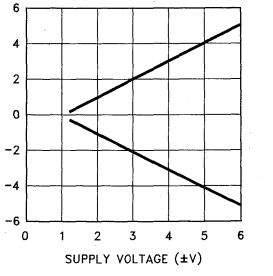
2180-17

−3 dB Bandwidth and Peaking vs Supply Voltage for Various Inverting Gains



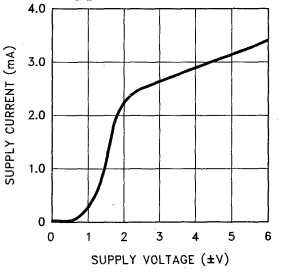
2180-18

Output Voltage Swing vs Supply Voltage



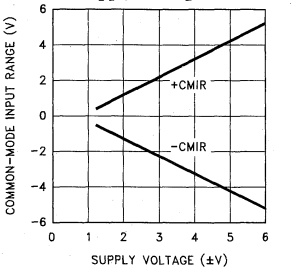
2180-19

Supply Current vs Supply Voltage



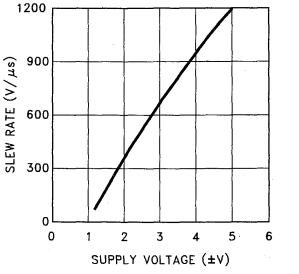
2180-20

Common-Mode Input Range vs Supply Voltage



2180-21

Slew Rate vs Supply Voltage



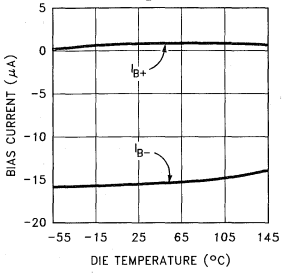
2180-22

EL2180C/EL2280C/EL2480C

250 MHz/3 mA Current Mode Feedback Amplifiers

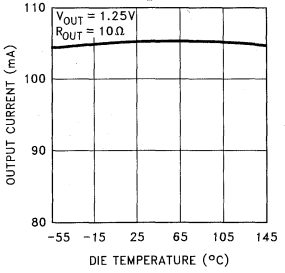
Typical Performance Curves — Contd.

Input Bias Current vs Die Temperature



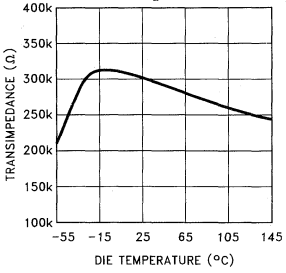
2180-23

Short-Circuit Current vs Die Temperature



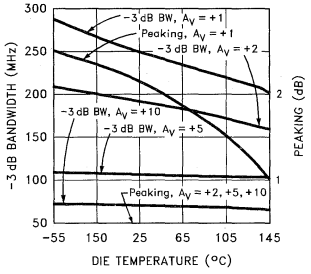
2180-24

Transimpedance (R_{OL}) vs Die Temperature



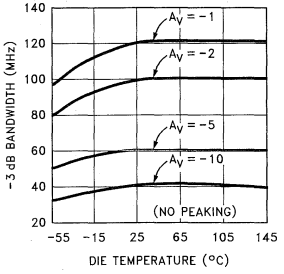
2180-25

−3 dB Bandwidth and Peaking vs Die Temperature for Various Non-Inverting Gains



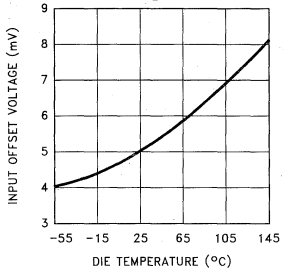
2180-26

−3 dB Bandwidth vs Die Temperature for Various Inverting Gains



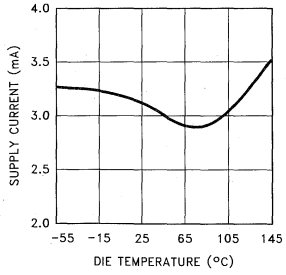
2180-27

Input Offset Voltage vs Die Temperature



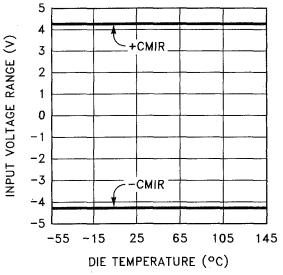
2180-28

Supply Current vs Die Temperature



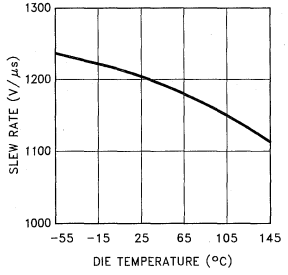
2180-29

Input Voltage Range vs Die Temperature



2180-30

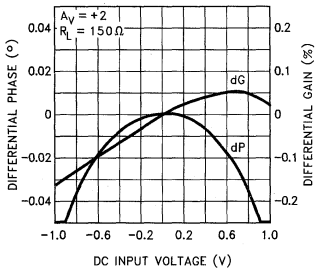
Slew Rate vs Die Temperature



2180-31

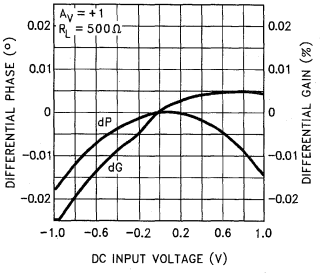
Typical Performance Curves — Contd.

Differential Gain and Phase vs DC Input Voltage at 3.58 MHz



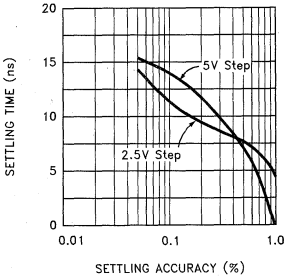
2180-32

Differential Gain and Phase vs DC Input Voltage at 3.58 MHz



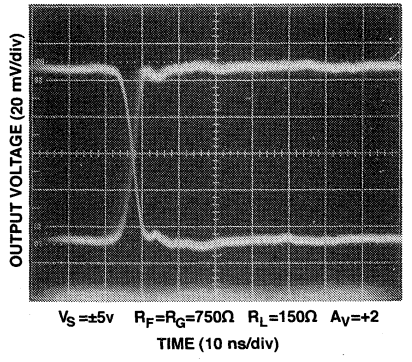
2180-33

Settling Time vs Settling Accuracy



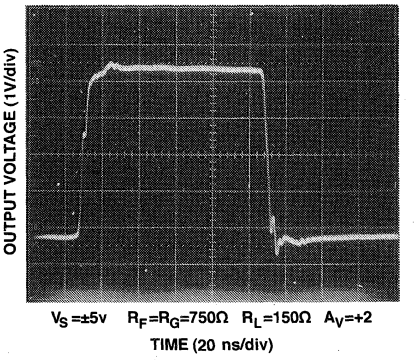
2180-34

Small-Signal Step Response



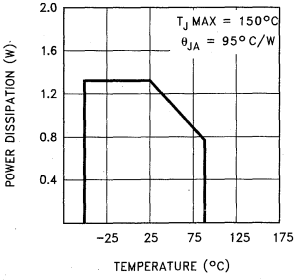
2180-35

Large-Signal Step Response



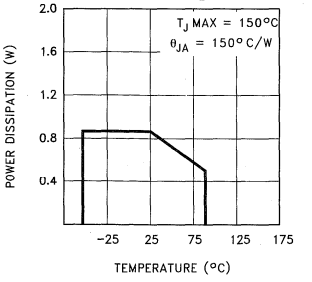
2180-36

8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



2180-37

8-Lead SO Maximum Power Dissipation vs Ambient Temperature



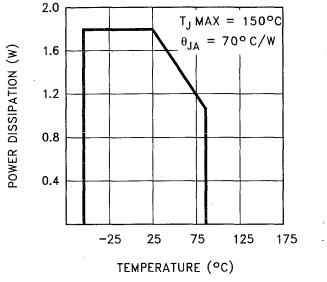
2180-38

EL2180C/EL2280C/EL2480C

250 MHz/3 mA Current Mode Feedback Amplifiers

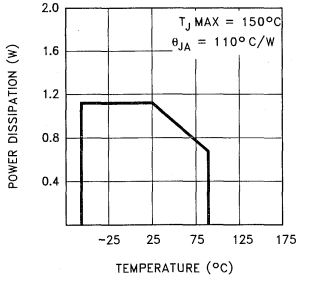
Typical Performance Curves — Contd.

14-Pin Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



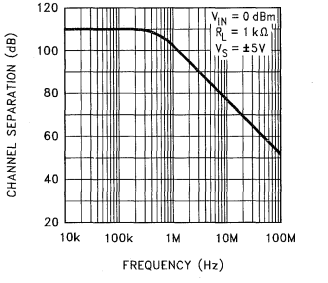
2180-39

14-Lead SO
Maximum Power Dissipation
vs Ambient Temperature



2180-40

Channel Separation
vs Frequency



2180-41

Applications Information

Product Description

The EL2180C/EL2280C/EL2480C are current-feedback operational amplifiers that offer a wide −3 dB bandwidth of 250 MHz and a low supply current of 3 mA per amplifier. All of these products also feature high output current drive. The EL2180C can output 100 mA, while the EL2280C and the EL2480C can output 55 mA per amplifier. The EL2180C/EL2280C/EL2480C work with supply voltages ranging from a single 3V to ±6V, and they are also capable of swinging to within 1V of either supply on the input and the output. Because of their current-feedback topology, the EL2180C/EL2280C/EL2480C do not have the normal gain-bandwidth product associated with voltage-feedback operational amplifiers. This allows their −3 dB bandwidth to remain relatively constant as closed-loop gain is increased. This combination of high bandwidth and low power, together with aggressive pricing make the EL2180C/EL2280C/EL2480C the ideal choice for many low-power/high-bandwidth applications such as portable computing, HDSL, and video processing.

For Single and Dual applications with disable, consider the EL2186C (8-Pin Single) and EL2286C (14-Pin Dual). If lower power is required, refer to the EL2170C/EL2176C family which provides Singles, Duals, and Quads with 70 MHz of bandwidth while consuming 1 mA of supply current per amplifier.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7 μF tantalum capacitor in parallel with a 0.1 μF capacitor has been shown to work well when placed at each supply pin.

For good AC performance, parasitic capacitance should be kept to a minimum especially at the inverting input (see the Capacitance at the Inverting Input section). Ground plane construction should be used, but it should be removed from the area near the inverting input to minimize any stray capacitance at that node. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of their additional series inductance. Use of sockets, particularly for the SO package, should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

Capacitance at the Inverting Input

Any manufacturer's high-speed voltage- or current-feedback amplifier can be affected by stray capacitance at the inverting input. For inverting gains this parasitic capacitance has little effect because the inverting input is a virtual ground, but for non-inverting gains this capacitance (in conjunction with the feedback and gain resistors) creates a pole in the feedback path of the amplifier. This pole, if low enough in frequency, has the same destabilizing effect as a zero in the forward open-loop response. The use of large value feedback and gain resistors further exacerbates the problem by further lowering the pole frequency.

The EL2180C/EL2280C/EL2480C have been specially designed to reduce power dissipation in the feedback network by using large 750Ω feedback and gain resistors. With the high bandwidths of these amplifiers, these large resistor values would normally cause stability problems when combined with parasitic capacitance, but by internally canceling the effects of a nominal amount of parasitic capacitance, the EL2180C/EL2280C/EL2480C remain very stable. For less experienced users, this feature makes the EL2180C/EL2280C/EL2480C much more forgiving, and therefore easier to use than other products not incorporating this proprietary circuitry.

EL2180C/EL2280C/EL2480C
250 MHz/3 mA Current Mode Feedback Amplifiers

Applications Information — Contd.

The experienced user with a large amount of PC board layout experience may find in rare cases that the EL2180C/EL2280C/EL2480C have less bandwidth than expected. In this case, the inverting input may have less parasitic capacitance than expected by the internal compensation circuitry of the EL2180C/EL2280C/EL2480C. The reduction of feedback resistor values (or the addition of a very small amount of external capacitance at the inverting input, e.g. 0.5 pF) will increase bandwidth as desired. Please see the curves for Frequency Response for Various R_F and R_G, and Frequency Response for Various $C_{IN}-$.

Feedback Resistor Values

The EL2180C/EL2280C/EL2480C have been designed and specified at gains of +1 and +2 with $R_F = 750\Omega$. This value of feedback resistor gives 250 MHz of −3 dB bandwidth at $A_V = +1$ with about 2.5 dB of peaking, and 180 MHz of −3 dB bandwidth at $A_V = +2$ with about 0.1 dB of peaking. Since the EL2180C/EL2280C/EL2480C are current-feedback amplifiers, it is also possible to change the value of R_F to get more bandwidth. As seen in the curve of Frequency Response For Various R_F and R_G, bandwidth and peaking can be easily modified by varying the value of the feedback resistor.

Because the EL2180C/EL2280C/EL2480C are current-feedback amplifiers, their gain-bandwidth product is not a constant for different closed-loop gains. This feature actually allows the EL2180C/EL2280C/EL2480C to maintain about the same −3 dB bandwidth, regardless of closed-loop gain. However, as closed-loop gain is increased, bandwidth decreases slightly while stability increases. Since the loop stability is improving with higher closed-loop gains, it becomes possible to reduce the value of R_F below the specified 750Ω and still retain stability, resulting in only a slight loss of bandwidth with increased closed-loop gain.

Supply Voltage Range and Single-Supply Operation

The EL2180C/EL2280C/EL2480C have been designed to operate with supply voltages having a span of greater than 3V, and less than 12V. In practical terms, this means that the EL2180C/EL2280C/EL2480C will operate on dual supplies ranging from ±1.5V to ±6V. With a single-supply, the EL2180C/EL2280C/EL2480C will operate from +3V to +12V.

As supply voltages continue to decrease, it becomes necessary to provide input and output voltage ranges that can get as close as possible to the supply voltages. The EL2180C/EL2280C/EL2480C have an input voltage range that extends to within 1V of either supply. So, for example, on a single +5V supply, the EL2180C/EL2280C/EL2480C have an input range which spans from 1V to 4V. The output range of the EL2180C/EL2280C/EL2480C is also quite large, extending to within 1V of the supply rail. On a ±5V supply, the output is therefore capable of swinging from −4V to +4V. Single-supply output range is even larger because of the increased negative swing due to the external pull-down resistor to ground. On a single +5V supply, output voltage range is about 0.3V to 4V.

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This is especially difficult when driving a standard video load of 150Ω, because of the change in output current with DC level. Until the EL2180C/EL2280C/EL2480C, good Differential Gain could only be achieved by running high idle currents through the output transistors (to reduce variations in output impedance). These currents were typically comparable to the entire 3 mA supply current of each EL2180C/EL2280C/EL2480C amplifier! Special circuitry has been incorporated in the EL2180C/EL2280C/EL2480C to reduce the variation of output impedance with current output. This results in dG and dP specifications of 0.05% and 0.05° while driving 150Ω at a gain of +2.

Applications Information — Contd.

Video Performance has also been measured with a 500Ω load at a gain of +1. Under these conditions, the EL2180C/EL2280C/EL2480C have dG and dP specifications of 0.01% and 0.01° respectively while driving 500Ω at A_V = +1.

Output Drive Capability

In spite of its low 3 mA of supply current, the EL2180C is capable of providing a minimum of ±80 mA of output current. Similarly, each amplifier of the EL2280C and the EL2480C is capable of providing a minimum of ±50 mA. These output drive levels are unprecedented in amplifiers running at these supply currents. With a minimum ±80 mA of output drive, the EL2180C is capable of driving 50Ω loads to ±4V, making it an excellent choice for driving isolation transformers in telecommunications applications. Similarly, the ±50 mA minimum output drive of each EL2280C and EL2480C amplifier allows swings of ±2.5V into 50Ω loads.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will decouple the EL2180C/EL2280C/EL2480C from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output to eliminate most peaking. The gain resistor (R_G) can then be chosen to make up for any gain loss which may be created by this additional resistor at the output. In many cases it is also possible to simply increase the value of the feedback resistor (R_F) to reduce the peaking.

Current Limiting

The EL2180C/EL2280C/EL2480C have no internal current-limiting circuitry. If any output is shorted, it is possible to exceed the Absolute Maximum Ratings for output current or power dissipation, potentially resulting in the destruction of the device.

Power Dissipation

With the high output drive capability of the EL2180C/EL2280C/EL2480C, it is possible to exceed the 150°C Absolute Maximum junction temperature under certain very high load current conditions. Generally speaking, when R_L falls below about 25Ω, it is important to calculate the maximum junction temperature (T_{Jmax}) for the application to determine if power-supply voltages, load conditions, or package type need to be modified for the EL2180C/EL2280C/EL2480C to remain in the safe operating area. These parameters are calculated as follows:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} * n * PD_{MAX}) \quad [1]$$

where:

T_{MAX} = Maximum Ambient Temperature
θ_{JA} = Thermal Resistance of the Package
n = Number of Amplifiers in the Package
PD_{MAX} = Maximum Power Dissipation of Each Amplifier in the Package.

PD_{MAX} for each amplifier can be calculated as follows:

$$PD_{MAX} = (2 * V_S * I_{SMAX}) + (V_S - V_{OUTMAX}) * (V_{OUTMAX}/R_L)) \quad [2]$$

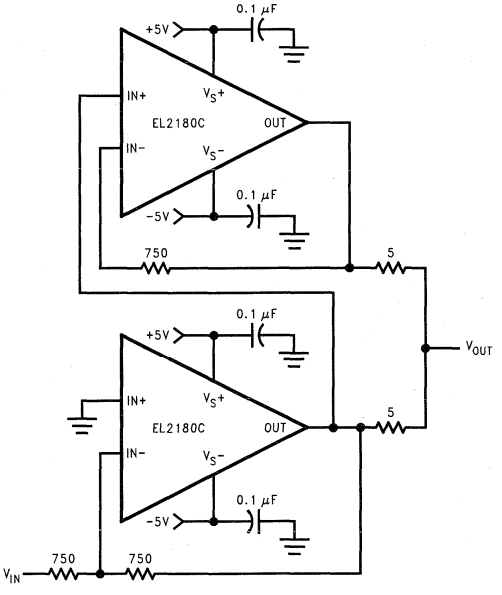
where:

V_S = Supply Voltage
I_{SMAX} = Maximum Supply Current of 1 Amplifier
V_{OUTMAX} = Max. Output Voltage of the Application
R_L = Load Resistance

EL2180C/EL2280C/EL2480C
250 MHz/3 mA Current Mode Feedback Amplifiers

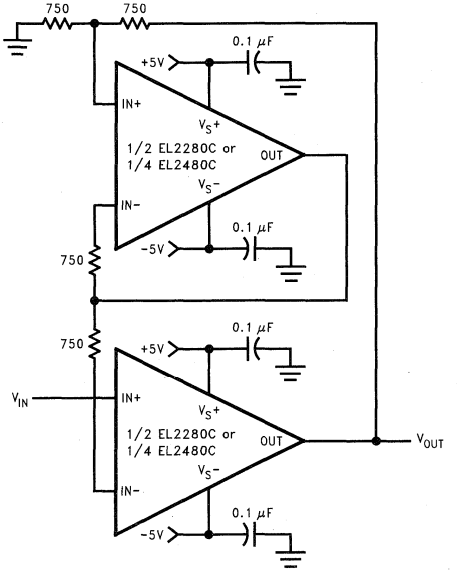
Typical Application Circuits

Inverting 200 mA Output Current Distribution Amplifier



2180-42

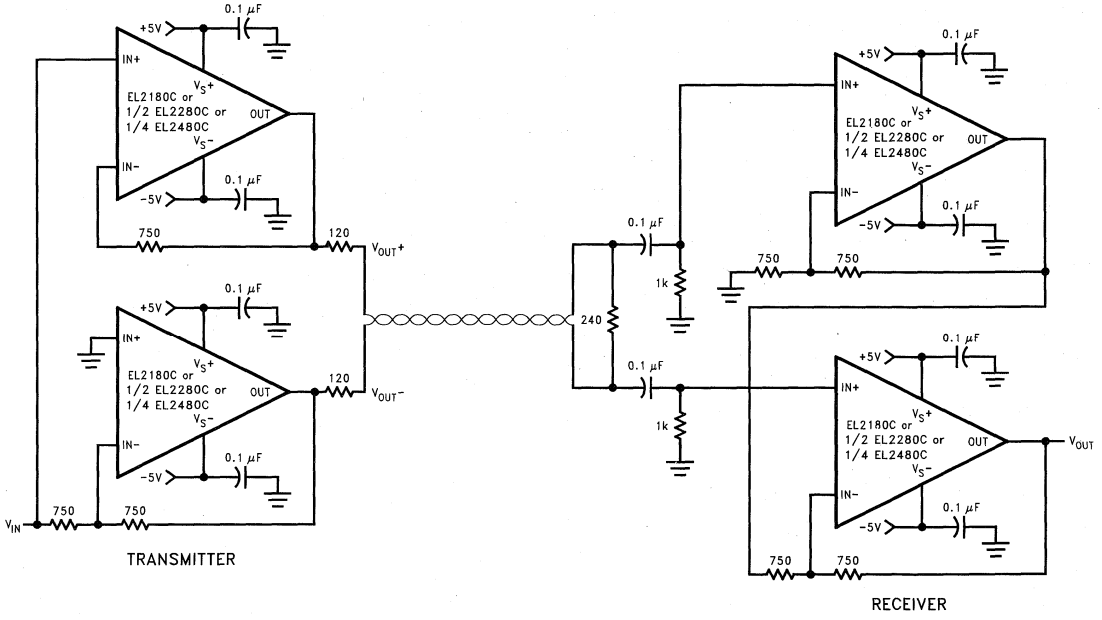
Fast-Settling Precision Amplifier



2180-43

Typical Application Circuits — Contd.

Differential Line-Driver/Receiver



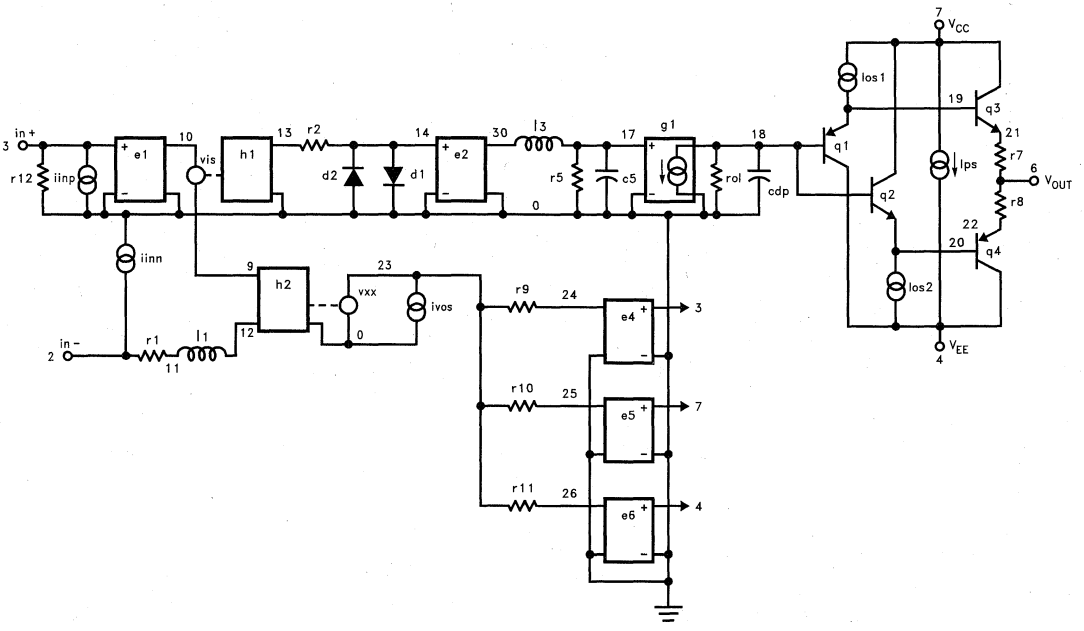
2180-44

EL2180C/EL2280C/EL2480C
250 MHz/3 mA Current Mode Feedback Amplifiers

EL2180C/EL2280C/EL2480C Macromodel

```
* EL2180 Macromodel
* Revision A, March 1995
* AC characteristics used: Rf = Rg = 750 ohms
* Connections:      +input
*                   |    -input
*                   |    |    +Vsupply
*                   |    |    |    -Vsupply
*                   |    |    |    |    output
*                   |    |    |    |    |
.subckt EL2180/el    3    2    7    4    6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 400
l1 11 12 25nH
iinp 3 0 1.5uA
iinm 2 0 3uA
r12 3 0 2Meg
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
e2 30 0 14 0 0.00166666666
l3 30 17 150nH
c5 17 0 0.8pF
r5 17 0 165
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 450K
cdp 18 0 0.675pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 1mA
ios2 20 4 1mA
*
* Supply Current
*
ips 7 4 0.2mA
*
* Error Terms
*
ivos 0 23 0.2mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 -1.0
r9 24 23 316
r10 25 23 3.2K
r11 26 23 3.2K
*
* Models
*
.model qn npn(is=5e-15 bf=200 tf=0.01nS)
.model qp pnp(is=5e-15 bf=200 tf=0.01nS)
.model dclamp d(is=1e-30 ibv=0.266
+ bv=0.71v n=4)
.ends
```

EL2180C/EL2280C/EL2480C Macromodel — Contd.



2180-45

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2186C/EL2286C

250 MHz/3 mA Current Mode Feedback Amp w/Disable

Features

- Single (EL2186C) and dual (EL2286C) topologies
- 3 mA supply current (per amplifier)
- 250 MHz −3 dB bandwidth
- Low cost
- Fast disable
- Powers down to 0 mA
- Single- and dual-supply operation down to ±1.5V
- 0.05%/0.05° diff. gain/diff. phase into 150Ω
- 1200V/μs slew rate
- Large output drive current:
  100 mA (EL2186C)
  55 mA (EL2286C)
- Also available without disable in single (EL2180C), dual (EL2280C) and quad (EL2480C)
- Lower power EL2170C/EL2176C family also available (1 mA/ 70 MHz) in single, dual and quad

Applications

- Low power/battery applications
- HDSL amplifiers
- Video amplifiers
- Cable drivers
- RGB amplifiers
- Test equipment amplifiers
- Current to voltage converters

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2186CN	−40°C to +85°C	8-Pin PDIP	MDP0031
EL2186CS	−40°C to +85°C	8-Pin SOIC	MDP0027
EL2286CN	−40°C to +85°C	14-Pin PDIP	MDP0031
EL2286CS	−40°C to +85°C	14-Pin SOIC	MDP0027

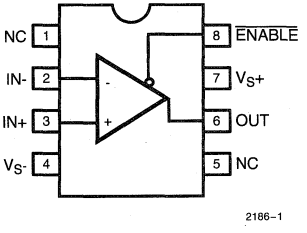
General Description

The EL2186C/EL2286C are single/dual current-feedback operational amplifiers which achieve a −3 dB bandwidth of 250 MHz at a gain of +1 while consuming only 3 mA of supply current per amplifier. They will operate with dual supplies ranging from ±1.5V to ±6V, or from single supplies ranging from +3V to +12V. The EL2186C/EL2286C also include a disable/power-down feature which reduces current consumption to 0 mA while placing the amplifier output in a high impedance state. In spite of its low supply current, the EL2286C can output 55 mA while swinging to ±4V on ±5V supplies. The EL2186C can output 100 mA with similar output swings. These attributes make the EL2186C/EL2286C excellent choices for low power and/or low voltage cable-driver, HDSL, or RGB applications.

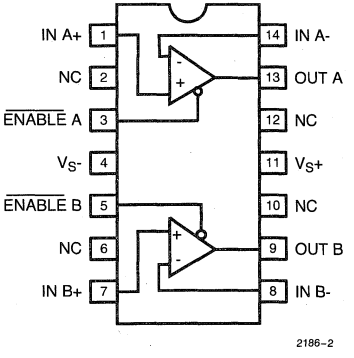
For Single, Dual and Quad applications without disable, consider the EL2180C (8-Pin Single), EL2280C (8-Pin Dual) or EL2480C (14-Pin Quad). For lower power applications where speed is still a concern, consider the EL2170C/El2176C family which also comes in similar Single, Dual and Quad configurations. The EL2170C/EL2176C family provides a −3 dB bandwidth of 70 MHz while consuming 1 mA of supply current per amplifier.

Connection Diagrams

EL2186C SO, P-DIP



EL2286C SO, P-DIP



EL2186C/EL2286C
250 MHz/3 mA Current Mode Feedback Amp w/Disable

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_S+ and V_S-	+12.6V	Operating Junction Temperature Plastic Packages	150°C
Common-Mode Input Voltage	V_S- to V_S+	Output Current (EL2186C)	±120 mA
Differential Input Voltage	±6V	Output Current (EL2286C)	±60 mA
Current into +IN or −IN	±7.5 mA	Storage Temperature Range	−65°C to +150°C
Internal Power Dissipation	See Curves		
Operating Ambient Temperature Range	−40°C to +85°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

V_S = ±5V, R_L = 150Ω, $\overline{ENABLE}$ = 0V, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage			2.5	15	I	mV
TCV_{OS}	Average Input Offset Voltage Drift	Measured from T_{MIN} to T_{MAX}		5		V	µV/°C
dV_{OS}	V_{OS} Matching	EL2286C only		0.5		V	mV
$+I_{IN}$	+ Input Current			1.5	15	I	µA
$d+I_{IN}$	+ I_{IN} Matching	EL2286C only		20		V	nA
$-I_{IN}$	− Input Current			16	30	I	µA
$d-I_{IN}$	$-I_{IN}$ Matching	EL2286C only		2		V	µA
CMRR	Common Mode Rejection Ratio	V_{CM} = ±3.5V	45	50		I	dB
−ICMR	− Input Current Common Mode Rejection	V_{CM} = ±3.5V		5	30	I	µA/V
PSRR	Power Supply Rejection Ratio	V_S is moved from ±4V to ±6V	60	70		I	dB
−IPSR	− Input Current Power Supply Rejection	V_S is moved from ±4V to ±6V		1	15	I	µA/V
R_{OL}	Transimpedance	V_{OUT} = ±2.5V	150	300		I	kΩ
$+R_{IN}$	+ Input Resistance	V_{CM} = ±3.5V	0.5	2		I	MΩ
$+C_{IN}$	+ Input Capacitance			1.2		V	pF
CMIR	Common Mode Input Range		±3.5	±4.0		I	V

EL2186C/EL2286C
250 MHz/3 mA Current Mode Feedback Amp w/Disable

DC Electrical Characteristics — Contd.

V_S = ±5V, R_L = 150Ω, $\overline{ENABLE}$ = 0V, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_O	Output Voltage Swing	V_S = ±5	±3.5	±4.0		I	V
		V_S = +5 Single-Supply, High		4.0		V	V
		V_S = +5 Single-Supply, Low		0.3		V	V
I_O	Output Current	EL2186C only	80	100		I	mA
		EL2286C only, per Amplifier	50	55		I	mA
I_S	Supply Current	$\overline{ENABLE}$ = 2.0V, per Amplifier		3	6	I	mA
$I_{S(DIS)}$	Supply Current (Disabled)	$\overline{ENABLE}$ = 4.5V		0	20	I	µA
$C_{OUT(DIS)}$	Output Capacitance (Disabled)	$\overline{ENABLE}$ = 4.5V		4.4		V	pF
R_{EN}	Enable Pin Input Resistance	Measured at $\overline{ENABLE}$ = 2.0V, 4.5V	45	85		I	kΩ
I_{IH}	Logic "1" Input Current	Measured at $\overline{ENABLE}$, $\overline{ENABLE}$ = 4.5V		−0.04		V	µA
I_{IL}	Logic "0" Input Current	Measured at $\overline{ENABLE}$, $\overline{ENABLE}$ = 0V		−53		V	µA
V_{DIS}	Minimum Voltage at $\overline{ENABLE}$ to Disable		4.5			I	V
V_{EN}	Maximum Voltage at $\overline{ENABLE}$ to Enable				2.0	I	V

AC Electrical Characteristics

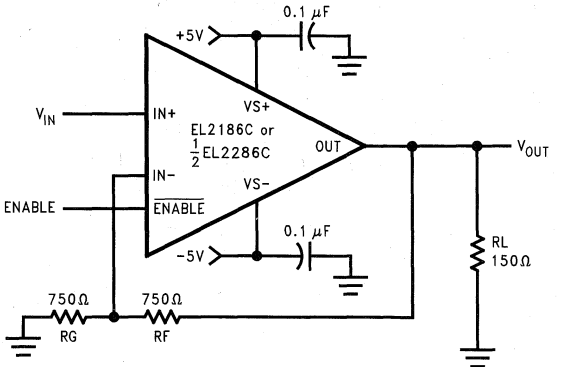
V_S = ±5V, R_F = R_G = 750Ω, R_L = 150Ω, $\overline{ENABLE}$ = 0V, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
−3 dB BW	−3 dB Bandwidth	A_V = +1		250		V	MHz
−3 dB BW	−3 dB Bandwidth	A_V = +2		180		V	MHz
0.1 dB BW	0.1 dB Bandwidth	A_V = +2		50		V	MHz
SR	Slew Rate	V_{OUT} = ±2.5V, A_V = +2	600	1200		IV	V/µs
t_r, t_f	Rise and Fall Time	V_{OUT} = ±500 mV		1.5		V	ns
t_{pd}	Propagation Delay	V_{OUT} = ±500 mV		1.5		V	ns
OS	Overshoot	V_{OUT} = ±500 mV		3.0		V	%
t_s	0.1% Settling	V_{OUT} = ±2.5V, A_V = −1		15		V	ns
dG	Differential Gain	A_V = +2, R_L = 150Ω (Note 1)		0.05		V	%
dP	Differential Phase	A_V = +2, R_L = 150Ω (Note 1)		0.05		V	
dG	Differential Gain	A_V = +1, R_L = 500Ω (Note 1)		0.01		V	%
dP	Differential Phase	A_V = +1, R_L = 500Ω (Note 1)		0.01		V	°
t_{ON}	Turn-On Time	A_V = +2, V_{IN} = +1V, R_L = 150Ω (Note 2)		40	100	I	ns
t_{OFF}	Turn-Off Time	A_V = +2, V_{IN} = +1V, R_L = 150Ω (Note 2)		500	1000	I	ns
CS	Channel Separation	EL2286C only, f = 5 MHz		85		V	dB

Note 1: DC offset from 0V to 0.714V, AC amplitude 286 mV_{P-P}, f = 3.58 MHz.

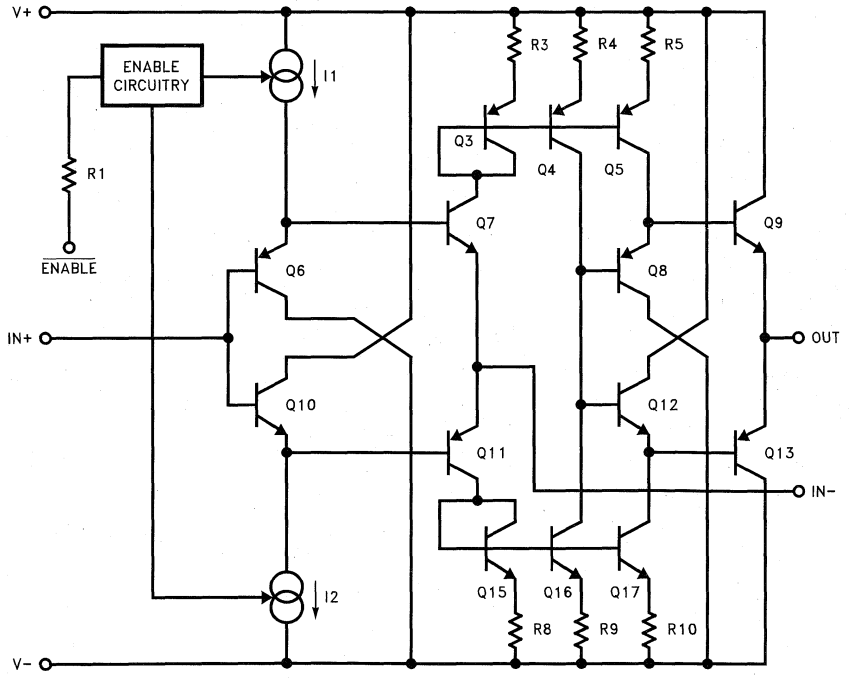
Note 2: Measured from the application of the logic signal until the output voltage is at the 50% point between initial and final values.

Test Circuit (per Amplifier)



2186-3

Simplified Schematic (per Amplifer)



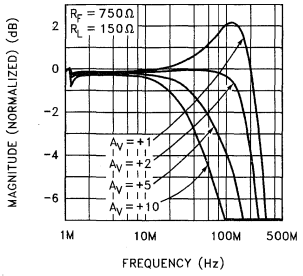
2186-4

EL2186C/EL2286C

250 MHz/3 mA Current Mode Feedback Amp w/Disable

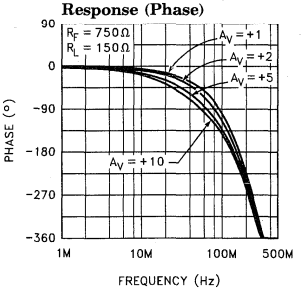
Typical Performance Curves

Non-Inverting Frequency Response (Gain)



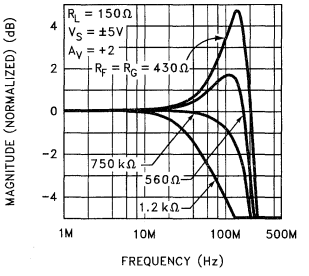
2186-5

Non-Inverting Frequency Response (Phase)



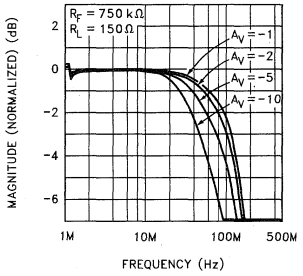
2186-6

Frequency Response for Various R_F and R_G



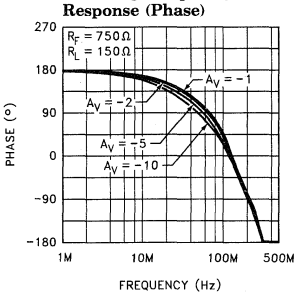
2186-7

Inverting Frequency Response (Gain)



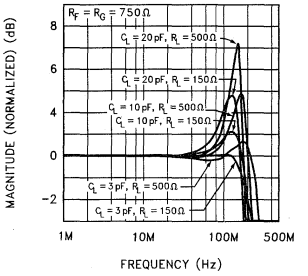
2186-8

Inverting Frequency Response (Phase)



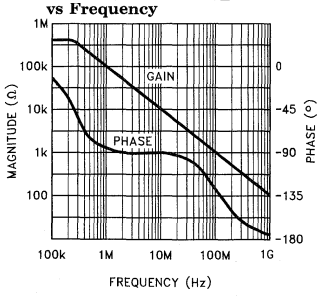
2186-9

Frequency Response for Various R_L and R_L



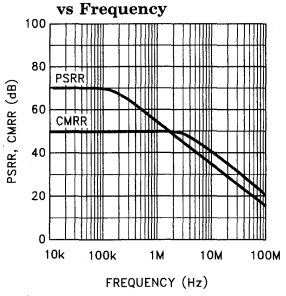
2186-10

Transimpedance (R_{OL}) vs Frequency



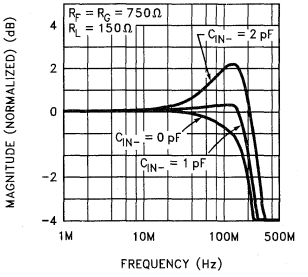
2186-11

PSRR and CMRR vs Frequency



2186-12

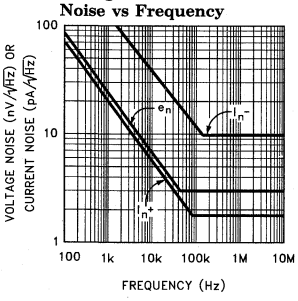
Frequency Response for Various C_{IN-}



2186-13

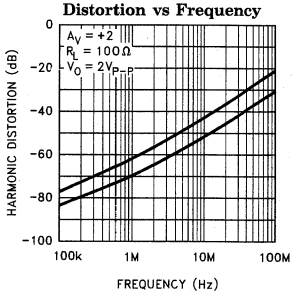
Typical Performance Curves — Contd.

Voltage and Current Noise vs Frequency



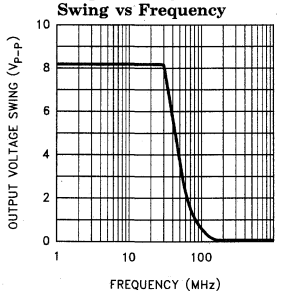
2186-14

2nd and 3rd Harmonic Distortion vs Frequency



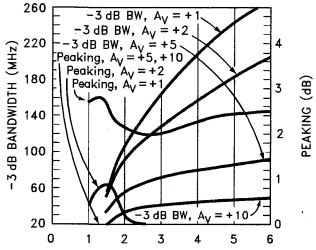
2186-15

Output Voltage Swing vs Frequency



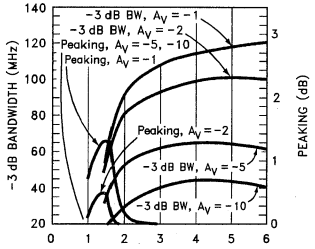
2186-16

−3 dB Bandwidth and Peaking vs Supply Voltage for Various Non-Inverting Gains



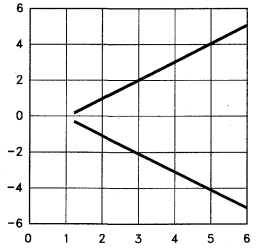
2186-17

−3 dB Bandwidth and Peaking vs Supply Voltage for Various Inverting Gains



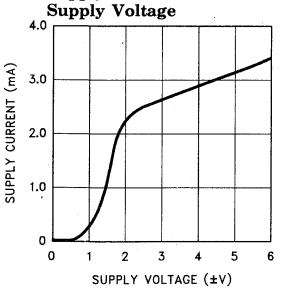
2186-18

Output Voltage Swing vs Supply Voltage



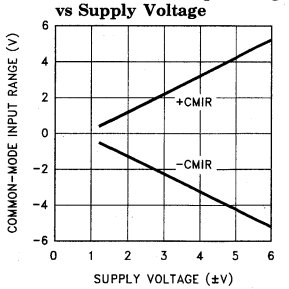
2186-19

Supply Current vs Supply Voltage



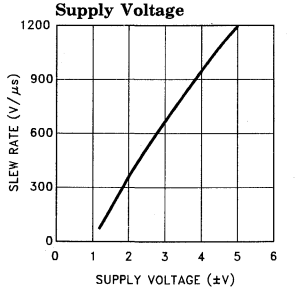
2186-20

Common-Mode Input Range vs Supply Voltage



2186-21

Slew Rate vs Supply Voltage



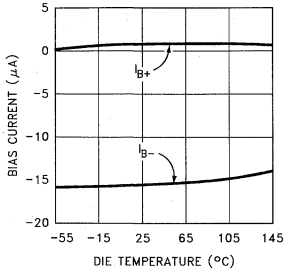
2186-22

EL2186C/EL2286C

250 MHz/3 mA Current Mode Feedback Amp w/Disable

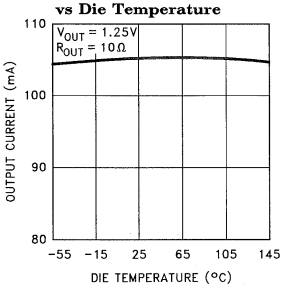
Typical Performance Curves — Contd.

Input Bias Current vs Die Temperature



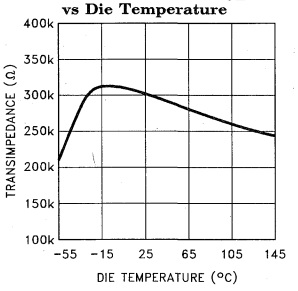
2186-23

Short-Circuit Current vs Die Temperature



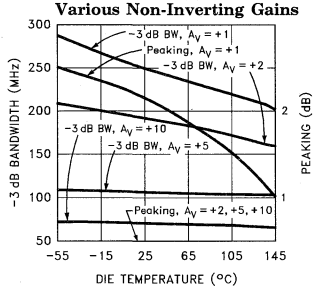
2186-24

Transimpedance (R_{OL}) vs Die Temperature



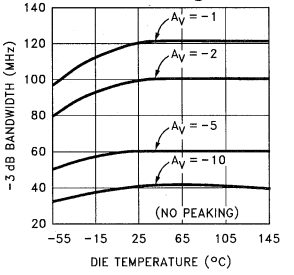
2186-25

−3 dB Bandwidth and Peaking vs Die Temperature for Various Non-Inverting Gains



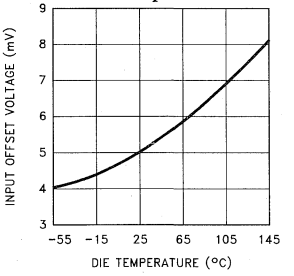
2186-26

−3 dB Bandwidth vs Die Temperature for Various Inverting Gains



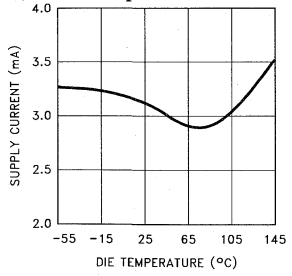
2186-27

Input Offset Voltage vs Die Temperature



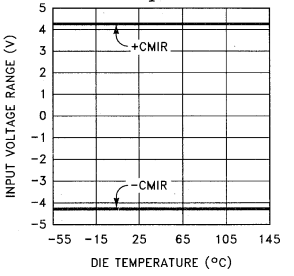
2186-28

Supply Current vs Die Temperature



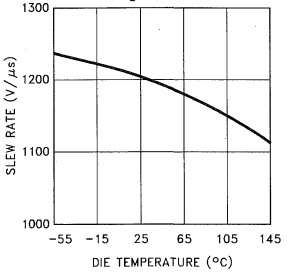
2186-29

Input Voltage Range vs Die Temperature



2186-30

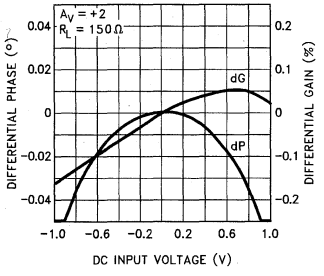
Slew Rate vs Die Temperature



2186-31

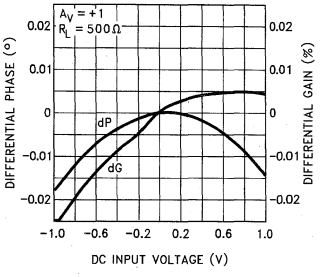
Typical Performance Curves — Contd.

Differential Gain and Phase vs DC Input Voltage at 3.58 MHz



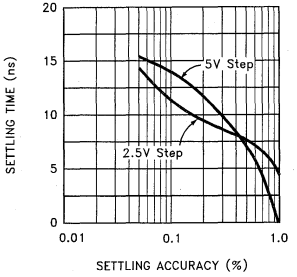
2186-32

Differential Gain and Phase vs DC Input Voltage at 3.58 MHz



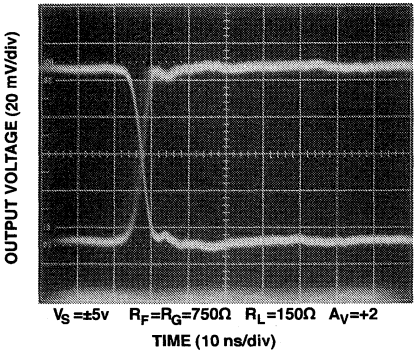
2186-33

Settling Time vs Settling Accuracy



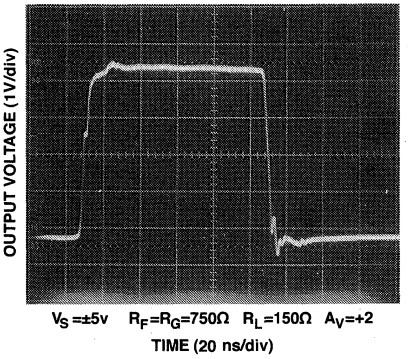
2186-34

Small-Signal Step Response



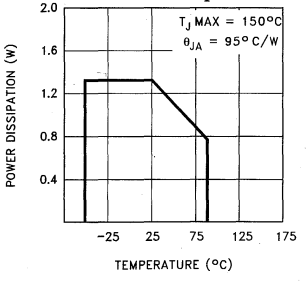
2186-35

Large-Signal Step Response



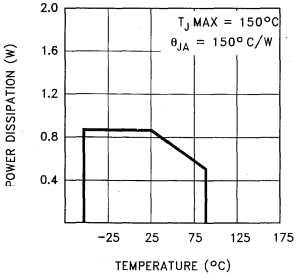
2186-36

8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



2186-37

8-Lead SO Maximum Power Dissipation vs Ambient Temperature

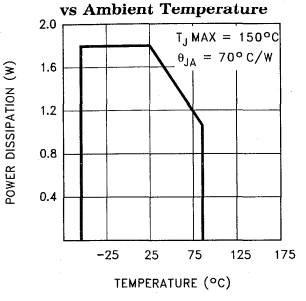


2186-38

EL2186C/EL2286C
250 MHz/3 mA Current Mode Feedback Amp w/Disable

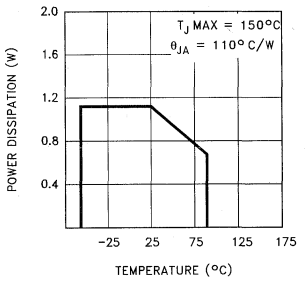
Typical Performance Curves — Contd.

14-Pin Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



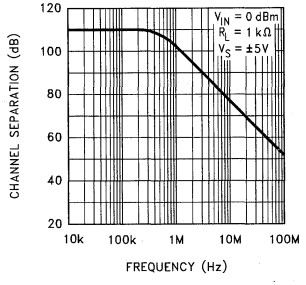
2186-39

14-Lead SO
Maximum Power Dissipation
vs Ambient Temperature



2186-40

Channel Separation
vs Frequency



2186-41

Applications Information

Product Description

The EL2186C/EL2286C are current-feedback operational amplifiers that offer a wide −3 dB bandwidth of 250 MHz, a low supply current of 3 mA per amplifier and the ability to disable to 0 mA. Both products also feature high output current drive. The EL2186C can output 100 mA, while the EL2286C can output 55 mA per amplifier. The EL2186C/EL2286C work with supply voltages ranging from a single 3V to ±6V, and they are also capable of swinging to within 1V of either supply on the input and the output. Because of their current-feedback topology, the EL2186C/EL2286C do not have the normal gain-bandwidth product associated with voltage-feedback operational amplifiers. This allows their −3 dB bandwidth to remain relatively constant as closed-loop gain is increased. This combination of high bandwidth and low power, together with aggressive pricing make the EL2186C/EL2286C the ideal choice for many low-power/high-bandwidth applications such as portable computing, HDSL, and video processing.

For Single, Dual and Quad applications without disable, consider the EL2180C (8-Pin Single), EL2280C (8-Pin Dual) and EL2480C (14-Pin Quad). If lower power is required, refer to the EL2170C/EL2176C family which provides Singles, Duals, and Quads with 70 MHz of bandwidth while consuming 1 mA of supply current per amplifier.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7 μF tantalum capacitor in parallel with a 0.1 μF capacitor has been shown to work well when placed at each supply pin.

For good AC performance, parasitic capacitance should be kept to a minimum especially at the inverting input (see the Capacitance at the Inverting Input section). Ground plane construction should be used, but it should be removed from the area near the inverting input to minimize any stray capacitance at that node. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of their additional series inductance. Use of sockets, particularly for the SO package should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

Disable/Power-Down

The EL2186C/EL2286C amplifiers can be disabled, placing their output in a high-impedance state. When disabled, each amplifier's supply current is reduced to 0 mA. Each EL2186C/EL2286C amplifier is disabled when its $\overline{\text{ENABLE}}$ pin is floating or pulled up to within 0.5V of the positive supply. Similarly, each amplifier is enabled by pulling its $\overline{\text{ENABLE}}$ pin at least 3V below the positive supply. For ±5V supplies, this means that an EL2186C/EL2286C amplifier will be enabled when $\overline{\text{ENABLE}}$ is at 2V or less, and disabled when $\overline{\text{ENABLE}}$ is above 4.5V. Although the logic levels are not standard TTL, this choice of logic voltages allows the EL2186C/EL2286C to be enabled by tying $\overline{\text{ENABLE}}$ to ground, even in +3V single-supply applications. The $\overline{\text{ENABLE}}$ pin can be driven from CMOS outputs or open-collector TTL.

When enabled, supply current does vary somewhat with the voltage applied at $\overline{\text{ENABLE}}$. For example, with the supply voltages of the EL2186C at ±5V, if $\overline{\text{ENABLE}}$ is tied to −5V (rather than ground) the supply current will increase about 15% to 3.45 mA.

Capacitance at the Inverting Input

Any manufacturer's high-speed voltage- or current-feedback amplifier can be affected by stray capacitance at the inverting input. For inverting gains this parasitic capacitance has little effect because the inverting input is a virtual ground, but for non-inverting gains this capacitance (in conjunction with the feedback and gain resistors) creates a pole in the feedback path of the amplifier. This pole, if low enough in frequency, has the

EL2186C/EL2286C
250 MHz/3 mA Current Mode Feedback Amp w/Disable

Applications Information — Contd.
same destabilizing effect as a zero in the forward open-loop response. The use of large value feedback and gain resistors further exacerbates the problem by further lowering the pole frequency.

The EL2186C/EL2286C have been specially designed to reduce power dissipation in the feedback network by using large 750Ω feedback and gain resistors. With the high bandwidths of these amplifiers, these large resistor values would normally cause stability problems when combined with parasitic capacitance, but by internally canceling the effects of a nominal amount of parasitic capacitance, the EL2186C/EL2286C remain very stable. For less experienced users, this feature makes the EL2186C/EL2286C much more forgiving, and therefore easier to use than other products not incorporating this proprietary circuitry.

The experienced user with a large amount of PC board layout experience may find in rare cases that the EL2186C/EL2286C have less bandwidth than expected. In this case, the inverting input may have less parasitic capacitance than expected by the internal compensation circuitry of the EL2186C/EL2286C. The reduction of feedback resistor values (or the addition of a very small amount of external capacitance at the inverting input, e.g. 0.5 pF) will increase bandwidth as desired. Please see the curves for Frequency Response for Various R_F and R_G, and Frequency Response for Various C_{IN-}.

Feedback Resistor Values
The EL2186C/EL2286C have been designed and specified at gains of +1 and +2 with R_F = 750Ω. This value of feedback resistor gives 250 MHz of −3 dB bandwidth at A_V = +1 with about 2.5 dB of peaking, and 180 MHz of −3 dB bandwidth at A_V = +2 with about 0.1 dB of peaking. Since the EL2186C/EL2286C are current-feedback amplifiers, it is also possible to change the value of R_F to get more bandwidth. As seen in the curve of Frequency Response For Various R_F and R_G, bandwidth and peaking can be easily modified by varying the value of the feedback resistor.

Because the EL2186C/EL2286C are current-feedback amplifiers, their gain-bandwidth product is not a constant for different closed-loop gains. This feature actually allows the EL2186C/EL2286C to maintain about the same −3 dB bandwidth, regardless of closed-loop gain. However, as closed-loop gain is increased, bandwidth decreases slightly while stability increases.

Since the loop stability is improving with higher closed-loop gains, it becomes possible to reduce the value of R_F below the specified 750Ω and still retain stability, resulting in only a slight loss of bandwidth with increased closed-loop gain.

Supply Voltage Range and Single-Supply Operation
The EL2186C/EL2286C have been designed to operate with supply voltages having a span of greater than 3V, and less than 12V. In practical terms, this means that the EL2186C/EL2286C will operate on dual supplies ranging from ±1.5V to ±6V. With a single-supply, the EL2176C will operate from +3V to +12V.

As supply voltages continue to decrease, it becomes necessary to provide input and output voltage ranges that can get as close as possible to the supply voltages. The EL2186C/EL2286C have an input voltage range that extends to within 1V of either supply. So, for example, on a single +5V supply, the EL2186C/EL2286C have an input range which spans from 1V to 4V. The output range of the EL2186C/EL2286C is also quite large, extending to within 1V of the supply rail. On a ±5V supply, the output is therefore capable of swinging from −4V to +4V. Single-supply output range is even larger because of the increased negative swing due to the external pull-down resistor to ground. On a single +5V supply, output voltage range is about 0.3V to 4V.

Video Performance
For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This is especially difficult when driving a standard video load of 150Ω, because of the change in output current with DC level. Until the EL2186C/EL2286C, good Differ-

Applications Information — Contd.

ential Gain could only be achieved by running high idle currents through the output transistors (to reduce variations in output impedance). These currents were typically comparable to the entire 3 mA supply current of each EL2186C/EL2286C amplifier! Special circuitry has been incorporated in the EL2186C/EL2286C to reduce the variation of output impedance with current output. This results in dG and dP specifications of 0.05% and 0.05° while driving 150Ω at a gain of +2.

Video Performance has also been measured with a 500Ω load at a gain of +1. Under these conditions, the EL2186C/EL2286C have dG and dP specifications of 0.01% and 0.01° respectively while driving 500Ω at $A_V = +1$.

Output Drive Capability

In spite of its low 3 mA of supply current, the EL2186C is capable of providing a minimum of ±80 mA of output current. Similarly, each amplifier of the EL2286C is capable of providing a minimum of ±50 mA. These output drive levels are unprecedented in amplifiers running at these supply currents. With a minimum ±80 mA of output drive, the EL2186C is capable of driving 50Ω loads to ±4V, making it an excellent choice for driving isolation transformers in telecommunications applications. Similarly, the ±50 mA minimum output drive of each EL2286C amplifier allows swings of ±2.5V into 50Ω loads.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will decouple the EL2186C/EL2286C from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output to eliminate most peaking. The gain resistor (R_G) can then be chosen to make up for any gain loss which may be created by this additional resistor at the output. In many cases it is also possible to simply increase the value of the feedback resistor (R_F) to reduce the peaking.

Current Limiting

The EL2186C/EL2286C have no internal current-limiting circuitry. If any output is shorted, it is possible to exceed the Absolute Maximum Ratings for output current or power dissipation, potentially resulting in the destruction of the device.

Power Dissipation

With the high output drive capability of the EL2186C/EL2286C, it is possible to exceed the 150°C Absolute Maximum junction temperature under certain very high load current conditions. Generally speaking, when R_L falls below about 25Ω, it is important to calculate the maximum junction temperature (T_{Jmax}) for the application to determine if power-supply voltages, load conditions, or package type need to be modified for the EL2186C/EL2286C to remain in the safe operating area. These parameters are calculated as follows:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} * n * PD_{MAX}) \quad [1]$$

where:

T_{MAX} = Maximum Ambient Temperature
θ_{JA} = Thermal Resistance of the Package
n = Number of Amplifiers in the Package
PD_{MAX} = Maximum Power Dissipation of Each Amplifier in the Package.

PD_{MAX} for each amplifier can be calculated as follows:

$$PD_{MAX} = (2 * V_S * I_{SMAX}) + (V_S - V_{OUTMAX}) * (V_{OUTMAX}/R_L) \quad [2]$$

where:

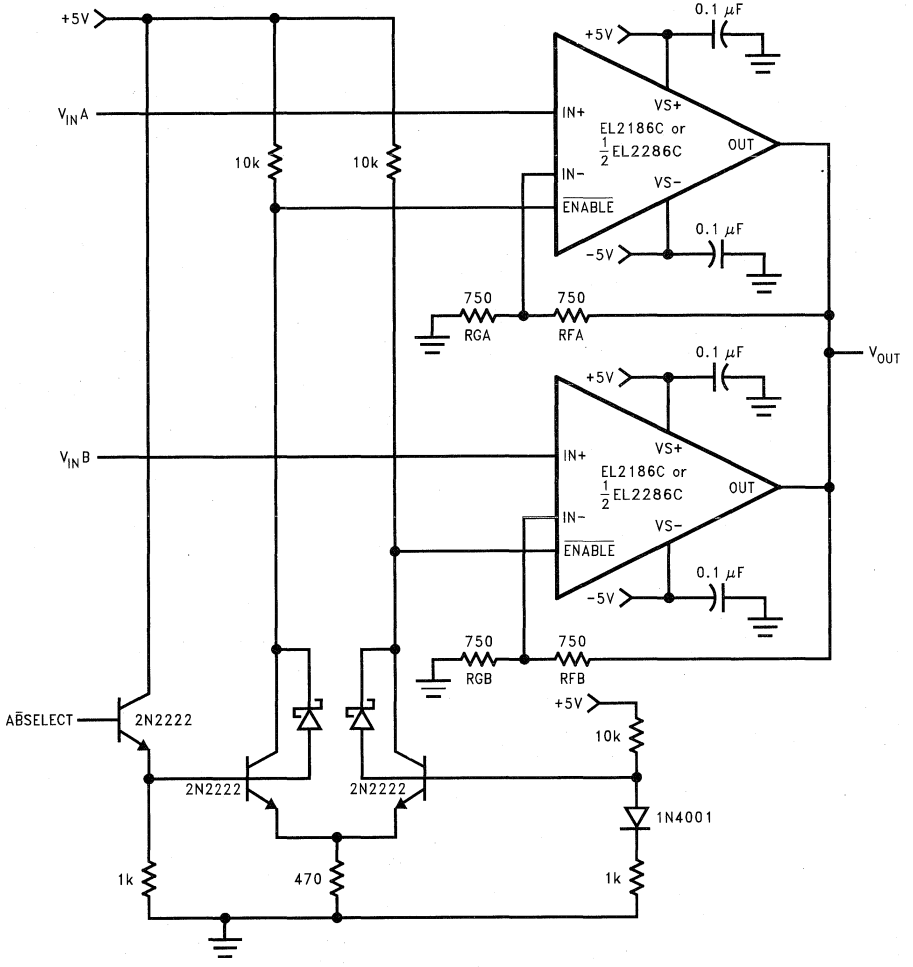
V_S = Supply Voltage
I_{SMAX} = Maximum Supply Current of 1 Amplifier
V_{OUTMAX} = Max. Output Voltage of the Application
R_L = Load Resistance

EL2186C/EL2286C

250 MHz/3 mA Current Mode Feedback Amp w/Disable

Typical Application Circuits

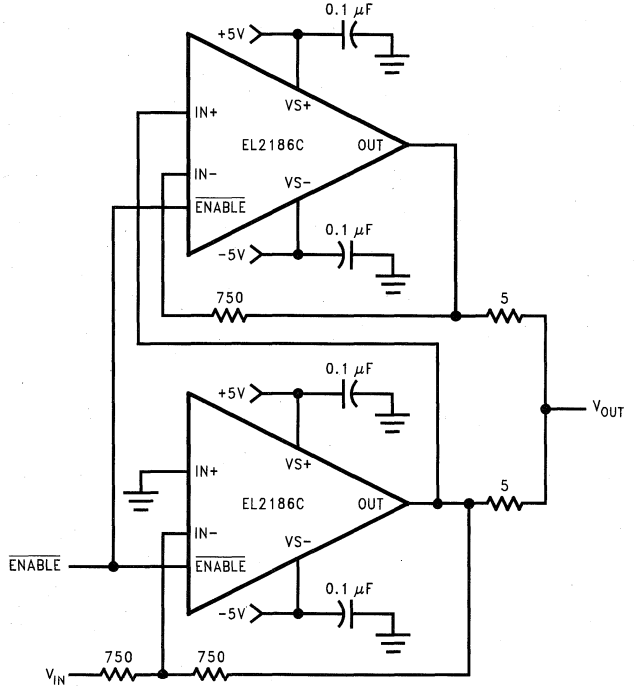
Low Power Multiplexer with Single-Ended TTL Input



2186-42

Typical Application Circuits — Contd.

Inverting 200 mA Output Current Distribution Amplifier



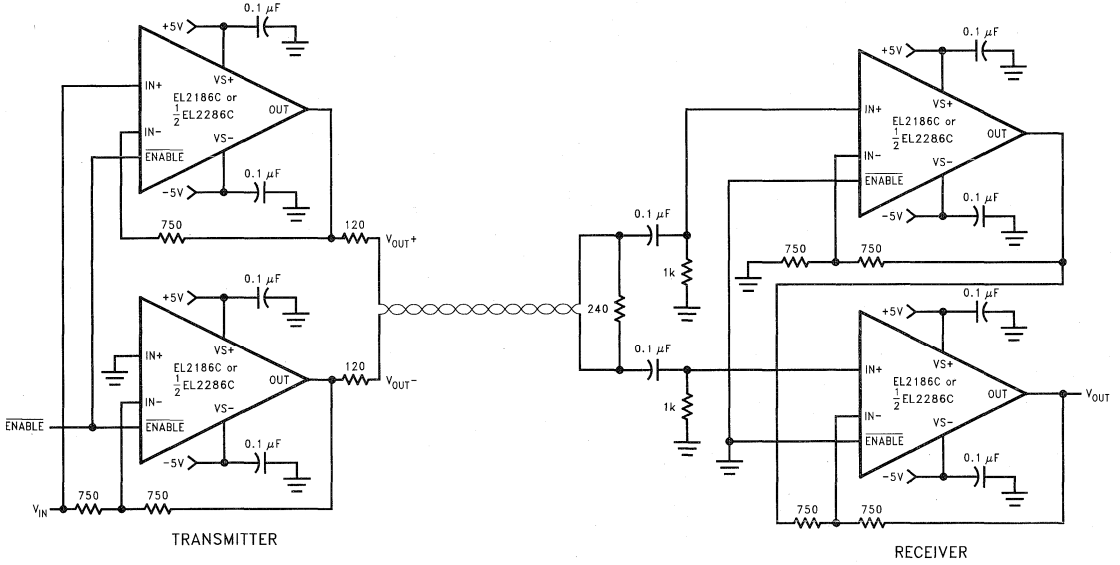
2186-43

EL2186C/EL2286C

250 MHz/3 mA Current Mode Feedback Amp w/Disable

Typical Application Circuits — Contd.

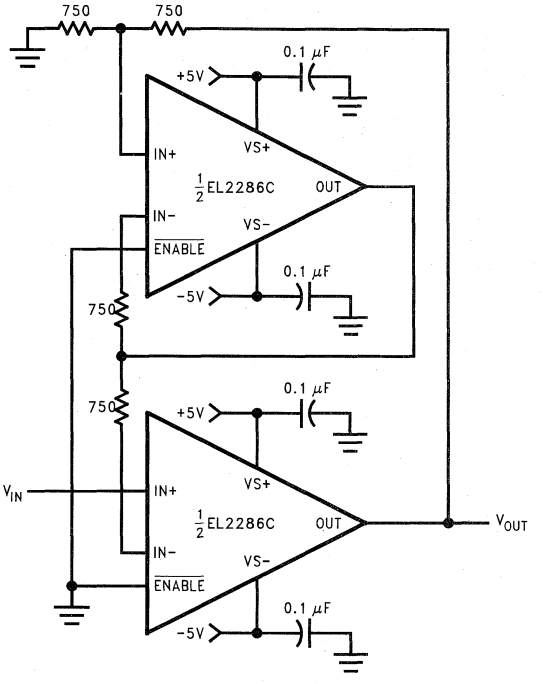
Differential Line-Driver/Receiver



2186-44

Typical Application Circuits — Contd.

Fast-Settling Precision Amplifer



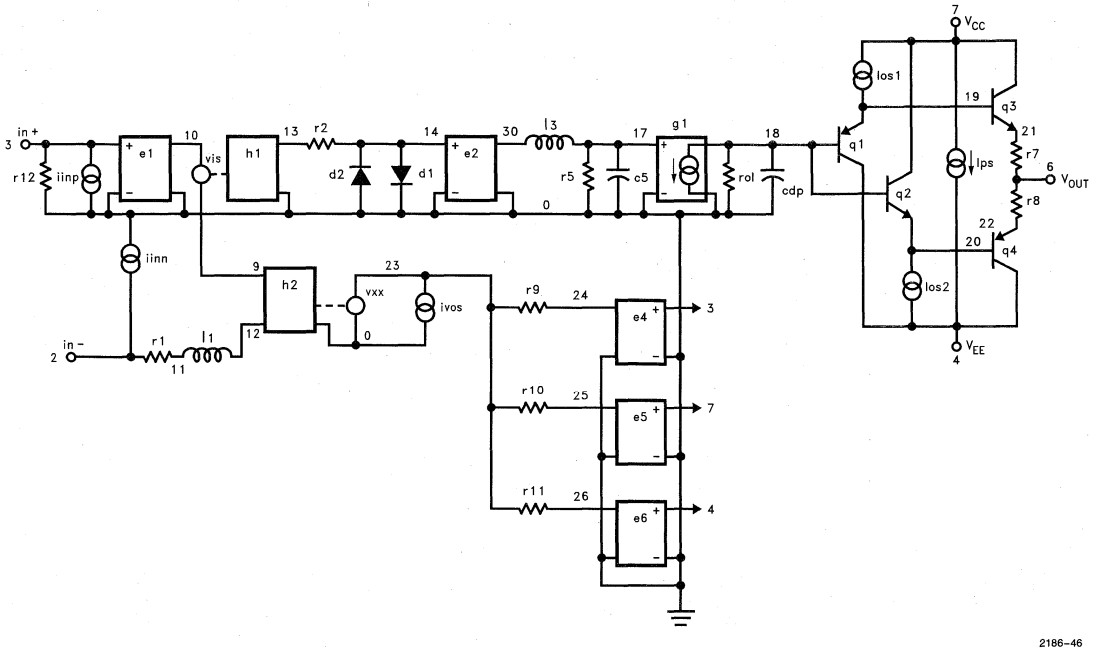
2186-45

EL2186C/EL2286C
250 MHz/3 mA Current Mode Feedback Amp w/Disable

EL2186C/EL2286C Macromodel

```
* EL2186 Macromodel
* Revision A, March 1995
* AC characteristics used: Rf = Rg = 750 ohms
* Connections:      +input
*                   |    -input
*                   |    |    +Vsupply
*                   |    |    |    -Vsupply
*                   |    |    |    |    output
*                   |    |    |    |    |
.subckt EL2186/el    3    2    7    4    6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 400
l1 11 12 25nH
iinp 3 0 1.5uA
iinm 2 0 3uA
r12 3 0 2Meg
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
e2 30 0 14 0 0.00166666666
l3 30 17 150nH
c5 17 0 0.8pF
r5 17 0 165
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 450K
cdp 18 0 0.675pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 1mA
ios2 20 4 1mA
*
* Supply Current
*
ips 7 4 0.2mA
*
* Error Terms
*
ivos 0 23 0.2mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 -1.0
r9 24 23 316
r10 25 23 3.2K
r11 26 23 3.2K
*
* Models
*
.model qn npn(is=5e-15 bf=200 tf=0.01nS)
.model qp pnp(is=5e-15 bf=200 tf=0.01nS)
.model dclamp d(is=1e-30 ibv=0.266
+ bv=0.71v n=4)
.ends
```

EL2186C/EL2286C Macromodel — Contd.



2186-46

Application Specific Video

élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL1882C
Video Sync Separator w/50% Slicing

Features

- NTSC, PAL, SECAM, non-standard video sync separation
- Precision 50% slicing of video input levels from 0.5 V_{P-P} to 2 V_{P-P}
- Low supply current - 1.5 mA typ.
- Single +5V supply
- Composite, vertical sync output
- Odd/Even field output
- Burst/Back porch output
- Plug-in compatible with industry standard LM1881 in 5V applications
- Available in 8-pin DIP and SO package

Applications

- Existing LM1881 applications
- Video special effects
- Video test equipment
- Video distribution
- Displays
- Imaging
- Video data capture
- Video triggers

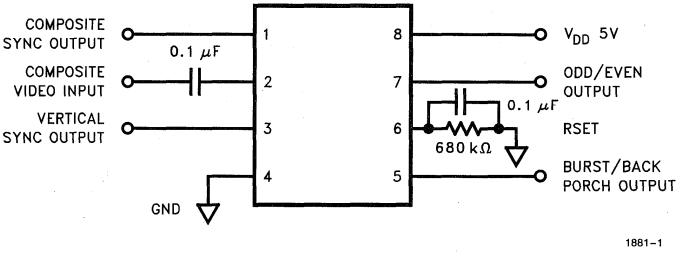
Ordering Information

Part No.	Temp. Range	Package	Outline #
EL1882CN	−40°C to +85°C	8-pin DIP	MDP0031
EL1882CS	−40°C to +85°C	8-lead SO	MDP0027

General Description

The EL1882C video sync separator is manufactured using Elantec's high performance analog CMOS process. This device extracts sync timing information from both standard and non-standard video input, including composite sync, vertical sync, burst/back porch timing and odd/even field detection. 50% sync tip slicing provides precise sync edge detection when the video input level is between 0.5 Vp-p and 2 Vp-p (sync tip amplitude 143 mV to 572 mV). A single external resistor sets all internal timing to adjust for various video standards. The **composite sync** output follows **video in** sync pulses, and a **vertical sync** pulse is output on the rising edge of the first vertical serration following the vertical pre-equalizing string. For non-standard vertical inputs, a default vertical pulse is output when the vertical signal stays low for longer than the vertical sync default delay time. The **odd/even** output indicates field polarity detected during the vertical blanking interval. The EL1882C is plug-in compatible with the industry standard LM1881 and can be substituted for that part in 5V applications with improved 50% slicing and lower required supply current.

Connection Diagram



1881-1

EL1882C
Video Sync Separator w/50% Slicing

Absolute Maximum Ratings (T_A = 25°C)

V_{CC} Supply	7V	Operating Ambient Temperature Range	−40°C to +85°C
Storage Temperature	−65°C to +150°C	Operating Junction Temperature	125°C
Lead Temperature (5 sec)	260°C	Power Dissipation	400 mW
Pin Voltages	−0.5V to V_{CC}+0.5V		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics Unless otherwise stated, V_{DD} = 5V, T_A = 25°C, R_{SET} = 680 kΩ

Parameter	Description	Min	Typ	Max	Test Level	Units
I_{DD}, Quiescent	V_{DD} = 5V	0.75	1.5	3.0	I	mA
Clamp Voltage	Pin 2, Unloaded	1.35	1.5	1.65	I	V
Clamp Discharge Current	Pin 2 = 2V	3.2	10	12	I	µA
Clamp Charge Current	Pin 2 = 1V	−2.0	−1.2	−0.8	I	mA
R_{SET} Pin Reference Voltage	Pin 6	1.2	1.32	1.44	I	V
V_{OL} Output Low Voltage	I_{OL} = 1.6 mA		0.4	0.8	I	V
V_{OH} Output High Voltage	I_{OH} = −40 µA I_{OH} = −1.6 mA	4 2.4	4.8 3.5		IV I	V

Dynamic Characteristics

Parameter	Description	Min	Typ	Max	Test Level	Units
Comp Sync Prop Delay, t_{CS}	50% Input–50% CS	10	30	40	I	ns
Vertical Sync Width, t_{VS}	Normal or Default trigger, 50%–50%	185	230	290	I	µs
Vertical Sync Default Delay, t_{VSD}	From start of Vert Sync at input to vert out pulse	35	60	85	I	µs
Burst Gate Delay, t_{BD}	From rising edge of input to falling edge of Burst	400	550	700	I	ns
Burst Gate Width, t_B		2.9	3.5	4.4	I	µs
Input Dynamic Range	Video in amplitude to maintain 50% slice spec	0.5		2	I	V_{P-P}
Slice Level	Within above dynamic range	40	50	60	I	%

Pin Descriptions

Pin No.	Pin Name	Function
1	Comp Sync	Composite sync pulse output. Sync pulses start on a falling edge and end on a rising edge.
2	Video In	AC coupled composite video input. Sync tip must be at the lowest potential (Positive picture phase).
3	Vert Sync	Vertical sync pulse output. The falling edge of Vert Sync is the start of the vertical period.
4	GND	Supply ground.
5	Burst	Burst/Back porch output. Low during burst portion of composite video.
6	R_{SET}	An external resistor to ground sets all internal timing. A 680k resistor will provide correct timing for NTSC signals.
7	Odd/Even	Odd/Even field output. Low during odd fields, high during even fields. Transitions occur at start of Vert Sync pulse.
8	V_{DD}	Positive supply. (5V)

EL1882C
Video Sync Separator w/50% Slicing

Timing Diagrams

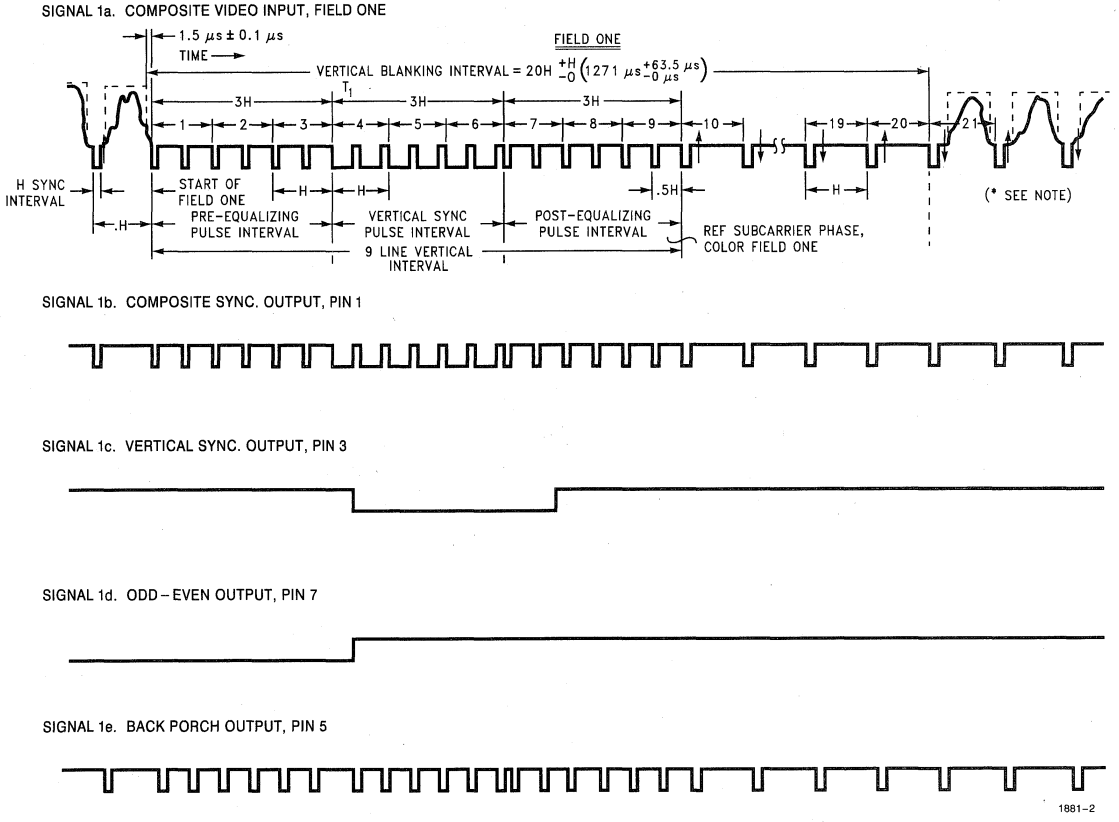


Figure 1

Notes:

b. The composite sync output reproduces all the video input sync pulses, with a propagation delay.

c. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.

d. Odd-even output is low for even field, and high for odd field.

e. Back porch goes low for a fixed pulse width on the trailing edge of video input sync pulses. Note that for serration pulses during vertical, the back porch starts on the rising edge of the serration pulse (with propagation delay).

* Signal 1a drawing reproduced with permission from EIA.

Applications Information

Video In

A simplified block diagram is shown following page.

An AC coupled video signal is input to **Video In** pin 2 via C1, nominally 0.1 μF. Clamp charge current will prevent the signal on pin 2 from going any more negative than Sync Tip Ref, about 1.5V. This charge current is nominally about 800 μA. A clamp discharge current of about 10 μA is always attempting to discharge C1 to Sync Tip Ref, thus charge is lost between sync pulses that must be replaced during sync pulses. The droop voltage that will occur can be calculated from IT = CV, where V is the droop voltage, I is the discharge current, T is the time between sync pulses (sync period − sync tip width), and C is C1.

An NTSC video signal has a horizontal frequency of 15.73 kHz, and a sync tip width of 4.7 μs. This gives a period of 63.6 μs and a time T = 58.9 μs. The droop voltage will then be V = 5.9 mV. This is less than 2% of a nominal sync tip amplitude of 286 mV. The charge represented by this droop is replaced in a time given by T=CV/I, where I = clamp charge current = 800 μA. Here T = 740 ns, about 16% of the sync pulse width of 4.7 μs. It is important to choose C1 so that the droop voltage does not approach the 50% switching threshold of the internal comparator.

AGC and Composite Sync

The clamped video signal then passes to the AGC, which will maintain the blanking level of its output (sensed during burst) at the blanking reference level. The AGC should therefore present a constant amplitude signal to the comparator, if the input is within the AGC's dynamic range. A 50% slicing reference is compared with the AGC's output at the comp circuit. Comp's output is level shifted and buffered to TTL levels, and sent out as **Comp Sync** on pin 1.

Burst

A low-going Burst pulse follows each rising edge of sync, and lasts approximately 3.5 μs for an R_{SET} of 680 kΩ. This signal is used internally to gate the AGC feedback for determining blanking level.

Vertical Sync

A low-going **Vertical Sync** pulse is output during the start of the vertical cycle of the incoming video signal. The vertical cycle starts with a pre-equalizing phase of pulses with a duty cycle of about 93%, followed by a vertical serration phase that has a duty cycle of about 15%. Vertical Sync is clocked out of the EL1882C on the first rising edge during the vertical serration phase. In the absence of vertical serration pulses, a vertical sync pulse will be forced out after the vertical sync default delay time, approximately 60 μs after the last falling edge of the vertical equalizing phase for R_{SET} = 680 kΩ.

Odd/Even

Because a typical television picture is composed of two interlaced frames, there is an odd frame that includes all the odd lines, and an even frame that consists of the even lines. This odd/even frame information is decoded by the EL1882C during the end of picture information and the beginning of vertical information. The odd/even circuit includes a T-flip-flop that is reset during full horizontal lines, but not during half lines or vertical equalization pulses. The T-flip-flop is clocked during each falling edge of these half h-period pulses. Even fields will toggle until a high state is clocked to the odd/even pin 7 at the beginning of vertical sync, and odd fields will cause a low state to be clocked to the odd/even pin at the start of the next vertical sync pulse. Odd/even can be ignored if using non-interlaced video, as there is no change in timing from one frame to the next.

R_{SET}

An external resistor R_{SET}, connected from R_{SET} pin 6 to ground, produces a reference current that is used internally as the timing reference for vertical sync width, vertical sync default delay, burst gate delay and burst width. Decreasing the value of R_{SET} increases the reference current, which in turn decreases reference times and pulse widths. A higher frequency video input necessitates a lower R_{SET} value.

EL1882C
Video Sync Separator w/50% Slicing

Simplified Block Diagram

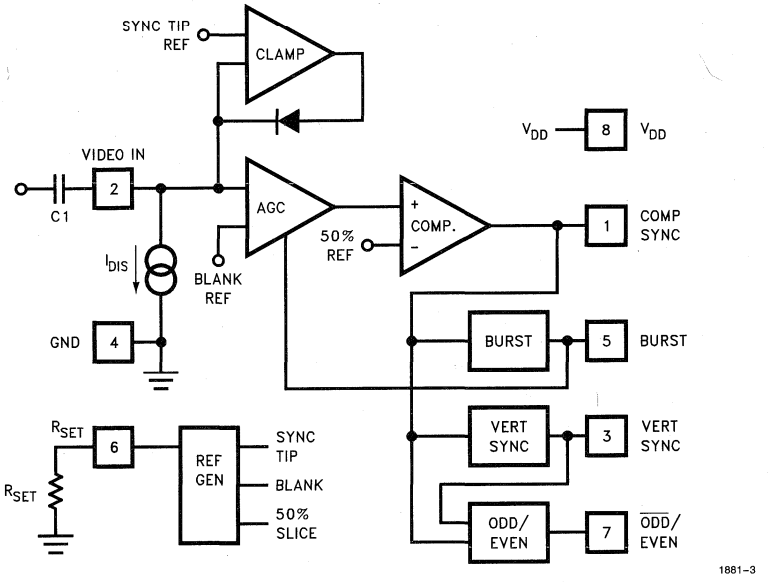


Figure 2

EL2210C/11C/EL2310C/11C/EL2410C/11C

Low Cost, Dual, Triple and Quad Video Op Amps

Features

- Stable at gain of 2 and 100 MHz gain—bandwidth product (EL2211, EL2311, EL2411)
- Stable at gain of 1 and 50 MHz gain—bandwidth product (EL2210, EL2310, EL2410)
- 130V/μs slew rate
- Drives 150Ω load to video levels
- Inputs and outputs operate at negative supply rail
- ±5V or +10V supplies
- −60 dB isolation at 4.2 MHz

Applications

- Consumer video amplifier
- Active filters/integrators
- Cost sensitive applications
- Single supply amplifiers

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2210CN	−40°C to +85°C	8-pin P-DIP	MDP0031
EL2211CN	−40°C to +85°C	8-pin P-DIP	MDP0031
EL2210CS	−40°C to +85°C	8-lead SO	MDP0027
EL2211CS	−40°C to +85°C	8-lead SO	MDP0027
EL2310CN	−40°C to +85°C	14-pin P-DIP	MDP0031
EL2311CN	−40°C to +85°C	14-pin P-DIP	MDP0031
EL2310CS	−40°C to +85°C	14-lead SO	MDP0027
EL2311CS	−40°C to +85°C	14-lead SO	MDP0027
EL2410CN	−40°C to +85°C	14-pin P-DIP	MDP0031
EL2411CN	−40°C to +85°C	14-pin P-DIP	MDP0031
EL2410CS	−40°C to +85°C	14-lead SO	MDP0027
EL2411CS	−40°C to +85°C	14-lead SO	MDP0027

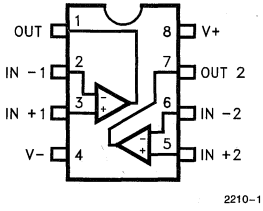
General Description

This family of dual, triple and quad operational amplifiers built using Elantec's Complementary Bipolar process offers unprecedented high frequency performance at a very low cost. They are suitable for any application such as consumer video, where traditional DC performance specifications are of secondary importance to the high frequency specifications. On ±5V supplies at a gain of +1 the EL2210C, EL2310C and the EL2410C will drive a 150Ω load to +2V, −1V with a bandwidth of 50 MHz and a channel to channel isolation of 60 dB or more. At a gain of +2 the EL2211C, EL2311C and EL2411C will drive a 150Ω load to +2V, −1V with a bandwidth of 100 MHz with the same channel to channel isolation. All four achieve 0.1 dB BW at 5 MHz.

The power supply operating range is fixed at ±5V or +10/0V. In single supply operation the inputs and outputs will operate to ground. Each amplifier draws only 7 mA of supply current.

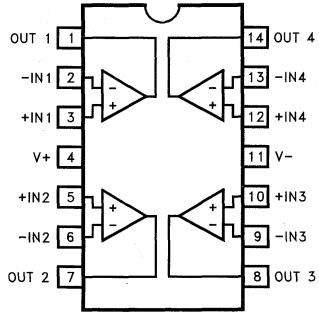
Connection Diagrams

EL2210C/EL2211C



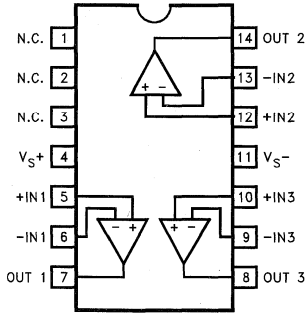
2210-1

EL2410C/EL2411C



2210-2

EL2310C/EL2311C



2210-5

EL2210C/11C/EL2310C/11C/EL2410C/11C
Low Cost, Dual, Triple and Quad Video Op Amps

Absolute Maximum Ratings

Total Voltage Supply	18V	Power Dissapation	See Curves
Input Voltage	±Vs	Storage Temperature Range	−65°C to +150°C
Differential Input Voltage	6V	Operating Temperature Range	−40°C to +85°C
Peak Output Current	75 mA per amplifier		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

EL2210, EL2310, EL2410

DC Electrical Characteristics V_S = ±5V, R_L = 1 KΩ, Temp. = 25°C unless otherwise noted

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage			10	20	I	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 2)		−25		V	µV/°C
I_B	Input Bias Current		−15	−7	−3	I	µA
I_{OS}	Input Offset Current			0.5	1.5	I	µA
TCI_{OS}	Average Offset Current Drift	(Note 2)		−7		V	nA/°C
A_{VOL}	Open-Loop Gain	V_{OUT} = ±2V, R_L = 1 KΩ	160	250		I	V/V
		V_{OUT} = +2V/0V, R_L = 150Ω	160	250		V	
PSRR	Power Supply Rejection	V_S = ±4.5V to ±5.5V	50	60		I	dB
CMRR	Common Mode Rejection	V_{CM} = ±2.4V, V_{OUT} = 0V	60	80		I	dB
CMIR	Common Mode Input Range	V_S = ±5V		−5/+3		V	V
V_{OUT}	OutputVoltage Swing	R_L = R_F = 1 KΩ R_L to Gnd	−2.5	−3, 3	2.7	I	V
		R_L = R_F = 1 KΩ +150Ω to Gnd	−0.45	−0.6, 2.9	2.5	I	
		R_L = R_F = 1 KΩ R_L to V_{EE}	−4.95		3	V	
I_{SC}	Output Short Circuit Current	Output to Gnd (Note 1)	75	125		I	mA
I_S	Supply Current	No Load (per channel)	5.5	6.8	8.5	I	mA
R_{IN}	Input Resistance	Differential		150		V	KΩ
		Common Mode		1.5		V	MΩ
C_{IN}	Input Capacitance	A_V = +1 @ 10 MHz		1		V	pF
R_{OUT}	Output Resistance			0.150		V	Ω
PSOR	Power Supply Operating Range	Dual Supply	±4.5		±6.5	V	V
		Single Supply	9		13	V	

EL2211, EL2311, EL2411

DC Electrical Characteristics $V_S = \pm 5V$, $R_L = 1\,K\Omega$, $A_V = +2$, Temp. = 25°C unless otherwise noted

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage			5	12	I	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 2)		−25		V	µV/°C
I_B	Input Bias Current		−15	−7	−3	I	µA
I_{OS}	Input Offset Current			0.5	1.5	I	µA
TCI_{OS}	Average Offset Current Drift	(Note 2)		−7		V	nA/°C
A_{VOL}	Open-Loop Gain	$V_{OUT} = \pm 2V$, $R_L = 1\,K\Omega$	250	380		I	V/V
		$V_{OUT} = +2V/0V$, $R_L = 150\Omega$	250	380		V	
PSRR	Power Supply Rejection	$V_S = \pm 4.5V$ to $\pm 5.5V$	55	68		I	dB
CMRR	Common Mode Rejection	$V_{CM} = \pm 2.5V$, $V_{OUT} = 0V$	70	90		I	dB
CMIR	Common Mode Input Range	$V_S = \pm 5V$		−5/+3		V	V
V_{OUT}	Output Voltage Swing	$R_L = R_F = 1\,K\Omega$ R_L to Gnd	2.5	−3.5, 3.3	2.7	I	V
		$R_L = R_F = 1\,K\Omega + 150\Omega$ to Gnd	−0.45	−0.6, 2.9	2.5	I	
		$R_L = R_F = 1\,K\Omega$ R_L to V_{EE}	−4.95		3	V	
I_{SC}	Output Short Circuit Current	Output to Gnd (Note 1)	75	125		I	mA
I_S	Supply Current	No Load	5.5	6.8	8.5	I	mA
R_{IN}	Input Resistance	Differential		150		V	KΩ
		Common Mode		1.5		V	MΩ
C_{IN}	Input Capacitance	$A_V = +1$ @ 10 MHz		1		V	pF
R_{OUT}	Output Resistance			0.150		V	Ω
PSOR	Power Supply Operating Range	Dual Supply	±4.5		6.5	V	V
		Single Supply	9		13	V	

EL2210, EL2310, EL2410

Closed-Loop AC Characteristics V_S = ±5V, AC Test Figure 1, Temp. = 25°C unless otherwise noted

Parameter	Description	Conditions	Min.	Typ.	Max.	Test Level	Units
BW	−3 dB Bandwidth (V_{OUT} = 0.4 V_{PP})	A_V = +1		110		V	MHz
BW	±0.1 dB Bandwidth (V_{OUT} = 0.4 V_{PP})	A_V = +1		12		V	MHz
GBWP	Gain Bandwidth Product			55		V	MHz
PM	Phase Margin			60		V	(°)
SR	Slew Rate		85	130		V	V/µs
FBWP	Full Power Bandwidth	(Note 3)	8	11		V	MHz
t_r, t_f	Rise Time, Fall Time	0.1V Step		2		V	ns
OS	Overshoot	0.1V Step		15		V	%
t_{PD}	Propagation Delay			3.5		V	ns
t_S	Settling to 0.1% (A_V = 1)	V_S = ±5V, 2V Step		80		V	ns
d_G	Differential Gain (Note 4)	NTSC/PAL		0.1		V	%
d_P	Differential Phase (Note 4)	NTSC/PAL		0.2		V	(°)
e_N	Input Noise Voltage	10 KHz		15		V	nV/rt (Hz)
i_N	Input Noise Current	10 KHz		1.5		V	pA/rt (Hz)
CS	Channel Separation	P = 5 MHz		55		V	dB

Note 1: A heat-sink is required to keep junction temperature below absolute maximum when an output is shorted.
Note 2: Measured from T_{MIN} to T_{MAX}
Note 3: For V_S = ±5V, V_{OUT} = 4 V_{PP}. Full power bandwidth is based on slew rate measurement using:
FPBW = SR/(2pi * V_{peak})
Note 4: Video performance measured at V_S = ±5V, A_V = +2 with 2 times normal video level across R_L = 150Ω.

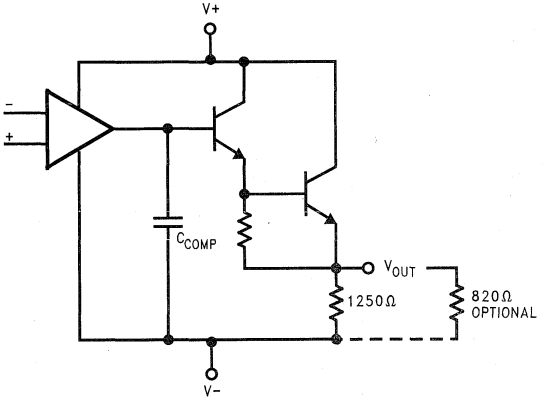
EL2211, EL2311, EL2411

Closed-Loop AC Characteristics V_S = ±5V, AC Test Figure 1, Temp. = 25°C unless otherwise noted

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
BW	−3 dB Bandwidth (V_{OUT} = 0.4 V_{PP})	A_V = +2		100		V	MHz
BW	±0.1 dB Bandwidth (V_{OUT} = 0.4 V_{PP})	A_V = +2		8		V	MHz
GBWP	Gain Bandwidth Product			130		V	MHz
PM	Phase Margin			60		V	(°)
SR	Slew Rate		100	140		V	V/µs
FBWP	Full Power Bandwidth	(Note 3)	8	11		V	MHz
t_r, t_f	Rise Time, Fall Time	0.1V Step		2.5		V	ns
OS	Overshoot	0.1V Step		6		V	%
t_{PD}	Propagation Delay			3.5		V	ns
t_S	Settling to 0.1% (A_V = 1)	V_S = ±5V, 2V Step		80		V	ns
d_G	Differential Gain (Note 4)	NTSC/PAL		0.04		V	%
d_P	Differential Phase (Note 4)	NTSC/PAL		0.15		V	(°)
e_N	Input Noise Voltage	10 KHz		15		V	nV/rt (Hz)
i_N	Input Noise Current	10 KHz		1.5		V	pA/rt (Hz)
CS	Channel Separation	P = 5 MHz		55		V	dB

Note 1: A heat-sink is required to keep junction temperature below absolute maximum when an output is shorted.
Note 2: Measured from T_{MIN} to T_{MAX}
Note 3: For V_S = ±5V, V_{OUT} = 4 V_{PP}. Full power bandwidth is based on slew rate measurement using:
FPBW = SR/(2pi * V_{peak})
Note 4: Video performance measured at V_S = ±5V, A_V = +2 with 2 times normal video level across R_L = 150Ω.

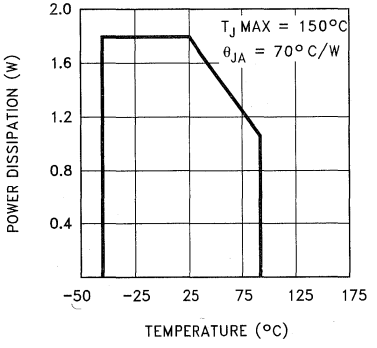
Simplified Block Diagram



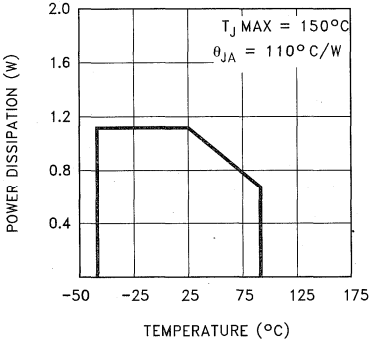
2210-3

Typical Performance Curves

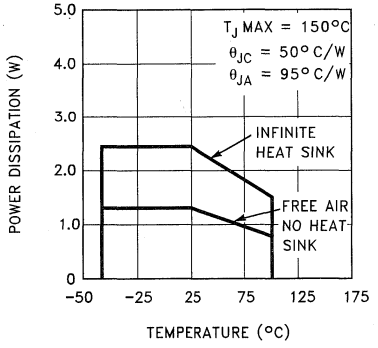
14-Pin Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



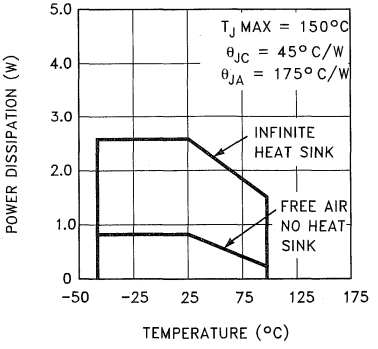
14-Lead SO
Maximum Power Dissipation
vs Ambient Temperature



8-Pin Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



8-Lead SO
Maximum Power Dissipation
vs Ambient Temperature



2210-4

Application Information

Product Description

The EL2210, EL2310 and EL2410 are dual, triple and quad operational amplifiers stable at a gain of 1. The EL2211, EL2311 and the EL2411 are dual, triple and quad operational amplifiers stable at a gain of 2. All six are built on Elantec's proprietary complimentary process and share the same voltage mode feedback topology. This topology allows them to be used in a variety of applications where current mode feedback amplifiers are not appropriate because of restrictions placed on the feedback elements. These products are especially designed for applications where high bandwidth and good video performance characteristics are desired but the higher cost of more flexible and sophisticated products are prohibitive.

Power Supplies

These amplifiers are designed to work at a supply voltage difference of 10V to 12V. These amplifers will work on any combination of ± supplies. All Electrical characteristics are measured with ±5V supplies. Below 9V total supply voltage the amplifiers' performance will degrade dramatically. The quiescent current is a direct function of total supply voltage. With a total supply voltage of 12V the quiescent supply current will increase from a typical 6.8 mA per amplifier to 8.5 mA per amplifer.

Output Swing vs Load

Please refer to the simplified block diagram. These amplifiers provide an NPN pull-up transistor output and a passive 1250Ω pull-down resistor to the most negative supply. In an application where the load is connected to V_S- the output voltage can swing to within 200 mV of V_S-. In split supply applications where the DC load is connected to ground the negative swing is limited by the voltage divider formed by the load, the internal 1250Ω resistor and any external pull-down resistor. If R_L were 150Ω then it and the 1250Ω internal resistor limit the maximum negative swing to (V_{EE}(150/1250+150)) or −0.53V. The negative swing can be increased by adding an external resistor of appropriate value from the output to the negative supply. The simplified block diagram shows an 820Ω external pull-down resistor. This resistor is in parallel with the internal 1250Ω resistor. This will increase the negative swing to V_{EE} (150/((1250 * 820/(1250 + 820) + 150) or −1.16V.

Power Dissipation and Loading

Without any load and a 10V supply difference the power dissipation is 70 mW per amplifier. At 12V supply difference this increases to 105 mW per amplifier. At 12V this translates to a junction temperature rise above ambient of 33° for the dual and 40° for the quad amplifier. When the amplifiers provide load current the power dissipation can rapidly rise.

In ±5V operation each output can drive a grounded 150Ω load to more than 2V. This operating condition will not exceed the maximum junction temperature limit as long as the ambient temperature is below 85°C, the device is soldered in place, and the extra pull-down resistor is 820Ω or more.

If the load is connected to the most negative voltage (ground in single supply operation) you can easily exceed the absolute maximum die temperature. For example the maximum die temperature should be 150°C. At a maximum expected ambient temperature of 85°C, the total allowable power dissipation for the SO-8 package would be:

P_D = (150 − 75)/180°C/W = 416 mW

At 12V total supply voltage each amplifier draws a maximum of 8.5 mA and dissipates 12V * 8.5 mA = 100 mW or 200 mW for the dual amplifier. Which leaves 216 mW of increased power due to the load. If the load were 150Ω connected to the most negative voltage and the maximum voltage out were V_S- +2V the load current would be 13 mA. Then an extra 266 mW ((12V − 2V) * 13.3 mA * 2) would be dissipated in the EL2210 or EL2211. The total dual amplifier power dissipation would be 266 mW + 200 mW = 466 mW, more than the maximum 416 mW allowed. If the total supply difference were reduced to 10V, the same calculations would yield 170 mW quiescent power dissipation and 213 mW due to loading. This results in a die temperature of 143°C (75°C + 69°C).

Application Information — Contd.

In the above example, if the supplies were split ±6V and the 150Ω loads were connected to ground, the load induced power dissipation would drop to 106 mW (13.3 mA * (6 − 2) * 2) and the die temperature would be below the rated maximum.

Video Performance

Following industry standard practices (see EL2044 applications section) these six devices exhibit good differential gain (dG) and good differential phase (dP) with ±5V supplies and an external 820Ω resistor to the negative supply, in a gain of 2 configuration. Driving 75Ω back terminated cables to standard video levels (1.428V at the amplifier) the EL2210, EL2310 and EL2410 have dG of 0.1% and dP of 0.2°. The EL2211, EL2311 and the EL2411 have dG of 0.04% and dP of 0.15°.

Due to the negative swing limitations described above, inverted video at a gain of 2 is just not practical. If swings below ground are required then changing the extra 820Ω resistor to 500Ω will allow reasonable dG and dP to approximately −0.75 mV. The EL2211, EL2311 and EL2411 will achieve approximately 0.1%/0.4° between 0V and −0.75V. Beyond −0.75V dG and dP get worse by orders of magnitude.

Differential gain and differential phase are fairly constant for all loads above 150Ω. Differential phase performance will improve by a factor of 3 if the supply voltage is increased to ±6V.

Output Drive Capability

None of these devices have short circuit protection. Each output is capable of more than 100 mA into a shorted output. Care must be used in the design to limit the output current with a series resistor.

Printed-Circuit Layout

The EL2210C/EL2211C/EL2310C/EL2311C/EL2410C/EL2411C are well behaved, and easy to apply in most applications. However, a few simple techniques will help assure rapid, high quality results. As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 0.1 μF ceramic capacitor is recommended for bypassing both supplies. Lead lengths should be as short as possible, and bypass capacitors should be as close to the device pins as possible. For good AC performance, parasitic capacitances should be kept to a minimum at both inputs and at the output. Resistor values should be kept under 5 KΩ because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wirewound resistors is not recommended because of their parasitic inductance. Similarly, capacitors should be low-inductance for best performance.

EL4390C

Triple 80 MHz Video Amplifier with DC Restore

Features

- 80 MHz −3 dB bandwidth for gains of 1 to 10
- 800 V/μs slew rate
- 15 MHz bandwidth flat to 0.1 dB
- Excellent differential gain and phase
- TTL/CMOS compatible DC restore function
- Available in 16 lead P-DIP, 16 lead SOL

Applications

- RGB drivers requiring DC restoration
- RGB multiplexers requiring DC restoration
- RGB building blocks
- Video gain blocks requiring DC restoration
- Sync and color burst processing

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4390CN	−40°C to +85°C	16-Pin P-DIP	MDP0031
EL4390CM	−40°C to +85°C	16-Lead SOL	MDP0027

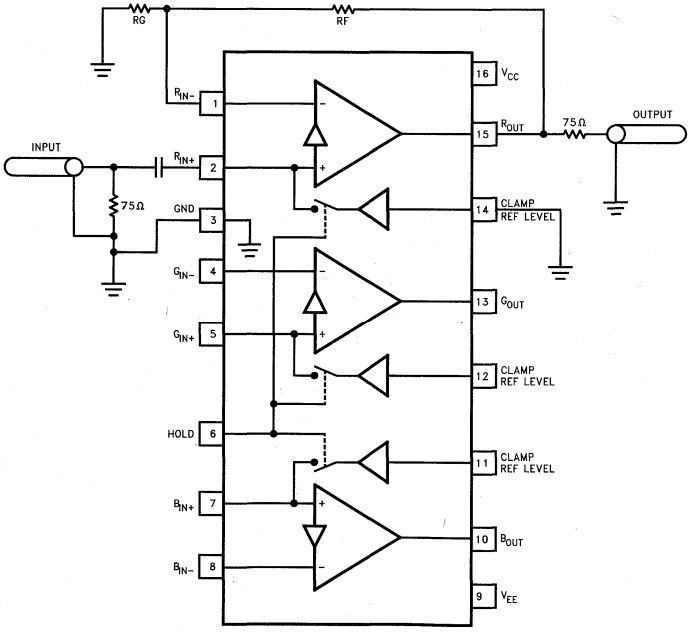
General Description

The EL4390C is three wideband current-mode feedback amplifiers optimized for video performance, each with a DC restore amplifier. The DC restore function is activated by a common TTL/CMOS compatible control signal while each channel has a separate restore reference.

Each amplifier can drive a load of 150Ω at video signal levels. The EL4390C operates on supplies as low as ±4V up to ±15V.

Being a current-mode feedback design, the bandwidth stays relatively constant at approximately 80MHz over the ±1 to ±10 gain range. The EL4390C has been optimized for use with 1300Ω feedback resistors.

Connection Diagram



4390-1

EL4390C
Triple 80 MHz Video Amplifier with DC Restore

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_S+ and V_S-	+33V	Internal Power Dissipation	See Curves
Voltage at V_S+	+18V	Operating Ambient Temp. Range	−40°C to +85°C
Voltage at V_S-	−18V	Operating Junction Temperature	150°C
Voltage between $V_{IN}+$ and $V_{IN}-$	±6V	Storage Temperature Range	−65°C to +150°C
Current into $V_{IN}+$ and $V_{IN}-$	5mA		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics Supplies at ±15V, Load = 1KΩ

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
Amplifier Section (not restored)							
V_{OS}	Input Offset Voltage	+25°C		2	15	II	mV
I_B+	$I_{IN}+$ Input Bias Current	+25°C		0.2	5	II	µA
I_B-	$I_{IN}-$ Input Bias Current	+25°C		10	65	II	µA
R_{OL}	Transimpedance (Note 1)	+25°C	100	220		II	kΩ
$R_{IN}-$	I_N- Resistance	+25°C		50		V	Ω
CMRR	Common-Mode Rejection Ratio (Note 2)	+25°C	50	56		II	dB
PSRR	Power Supply Rejection Ratio (Note 4)	+25°C	50	70		II	dB
V_O	Output Voltage Swing; R_L = 1kΩ	+25°C	±12	±13		II	V
I_{SC}	Short-Circuit Current	+25°C	45	70	100	II	mA
I_{SY}	Supply Current (Quiescent)	+25°C	10	20	32	II	mA
Restoring Section							
V_{OS}, COMP	Composite Input Offset Voltage (Note 3)	+25°C		8	35	II	mV
I_B+, R	Restore I_N+ Input Bias Current	+25°C		0.2	5	II	µA
I_{OUT}	Restoring Current Available	+25°C	2	4		II	mA
PSRR	Power Supply Rejection Ratio (Note 4)	+25°C	50	70		II	dB
G_{OUT}	Conductance	+25°C		8		V	mA/V
I_{SY}, RES	Supply Current, Restoring	+25°C	10	23	37	II	mA
V_{IL}, RES	RES Logic Low Threshold	+25°C		1.0	1.4	II	V
V_{IH}, RES	RES Logic High Threshold	+25°C	1.4	1.8		II	V

Open Loop DC Electrical Characteristics Supplies at ±15V, Load = 1KΩ — Contd.

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
Restoring Section							
I_{IL}, RES	RES Input Current, Logic Low	+25°C		2	10	II	μA
I_{IH}, RES	RES Input Current, Logic High	+25°C		0.5	3	II	μA

Note 1: For current feedback amplifiers, $A_{VOL} = R_{OL}/R_{IN}-$.
Note 2: $V_{CM} = \pm 10V$ for $V_S = \pm 15V$.
Note 3: Measured from V_{CL} to amplifier output, while restoring.
Note 4: V_{OS} is measured at $V_S = \pm 4.5V$ and $V_S = \pm 16V$, both supplies are changed simultaneously.

Closed Loop AC Electrical Characteristics

Supplies at ±15V, Load = 150Ω and 15 pF, T_A = 25°C (See note 7 re: test fixture)

Parameter	Description	Min	Typ	Max	Test Level	Units
Amplifier Section						
SR	Slew Rate (Note 5)		800		V	V/μs
SR	Slew Rate w/ ±5V Supplies (Note 5)		550		V	V/μs
BW	Bandwidth, −3dB, A_V = 1 ±5V Supplies, −3dB		95 72		V V	MHz MHz
BW	Bandwidth, −0.1 dB ±5V Supplies, −0.1dB		20 14		V V	MHz MHz
dG	Differential Gain at 3.58 MHz at ±5V Supplies (Note 6)		0.02 0.02		V V	% %
dθ	Differential Phase at 3.58 MHz at ±5V Supplies (Note 6)		0.03 0.06		V V	(°) (°)
Restoring Section						
T_{RE}	Time to Enable Restore		35		V	ns
T_{RD}	Time to Disable Restore		35		V	ns

Note 5: SR is measured at 20% to 80% of 4V pk-pk square wave, with $A_V = 5$, $R_F = 820\Omega$, $R_G = 200\Omega$.
Note 6: DC offset from −0.714V to +0.714V, AC amplitude is 286m Vp-p, equivalent to 40 ire.
Note 7: Test fixture was designed to minimize capacitance at the I_N- input. A "good" fixture should have less than 2 pF of stray capacitance to ground at this very sensitive pin. See application notes for further details.

Table 1. Charge Storage Capacitor Value vs. Droop and Charging Rates

Cap Value (nF)	Droop in 60μS (mV)	Charge in 2μS (mV)	Charge in 4μS (mV)
10	30	400	800
22	13.6	182	364
47	6.4	85	170
100	3.0	40	80
220	1.36	18	36

These numbers represent the worst case bias current, and the worst case charging current. Note that to get the full (2mA+) charging current, the clamp input must have >250mV of error voltage.

Note that the magnitude of the bias current will decrease as temperature increases.

The basic droop formula is :

$V\ (droop) = I_{B+} \times (Line\ time - Charge\ time) / capacitor\ value$

and the basic charging formula is:

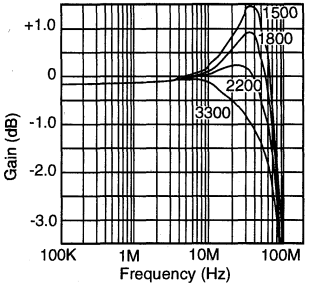
$V\ (charge) = I_{OUT} \times Charge\ time / capacitor\ value$

Where I_{OUT} is:

$I_{OUT} = (Clamp\ voltage - IN+\ voltage) / 120$

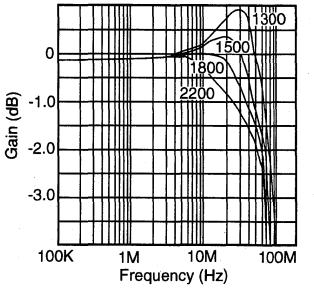
Typical Performance Curves

Gain Flatness for Various R_F $V_S = \pm 15V$, $A_V = 0$ dB



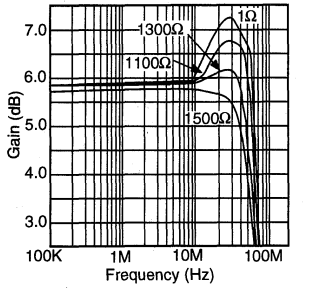
4390-2

Gain Flatness for Various R_F $V_S = \pm 5V$, $A_V = 0$ dB



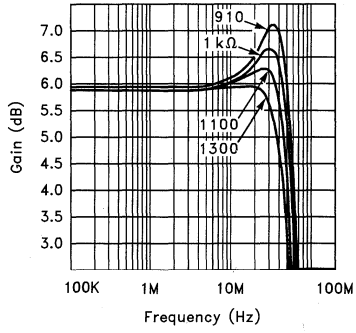
4390-3

Gain Flatness for Various R_F and R_G Values $V_S = \pm 15V$, $A_V = 6$ dB



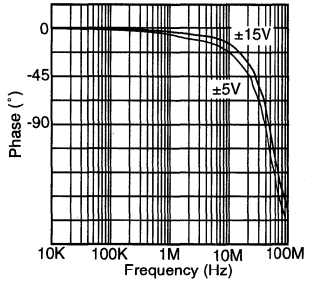
4390-4

Gain Flatness for Various R_F and R_G Values $V_S = \pm 5V$, $A_V = 6$ dB



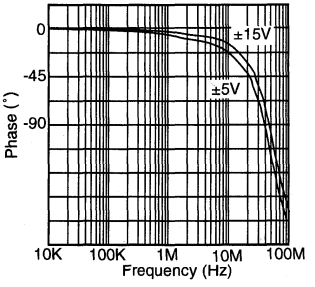
4390-6

Phase Shift for $A_V = 2$, $R_F = R_G = 1300\Omega$



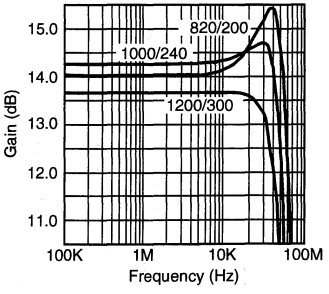
4390-5

Phase Shift for $A_V = 2$, $R_F = R_G = 1000\Omega$ at $V_S = \pm 5V$ and $V_S = \pm 15V$



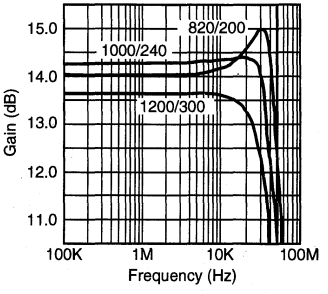
4390-7

Gain Flatness $V_S = \pm 15V$, $A_V = 14$ dB, R_F/R_G as Shown



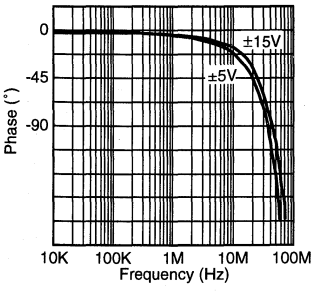
4390-8

Gain Flatness $V_S = \pm 5V$, $A_V = 14$ dB, R_F/R_G as Shown



4390-9

Phase Shift for $A_V = 5$ dB, $R_F = 820\Omega$, $R_G = 200\Omega$, $V_S = \pm 5V$

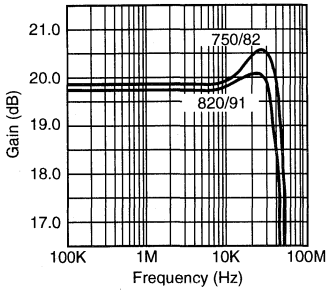


4390-10

EL4390C
Triple 80 MHz Video Amplifier with DC Restore

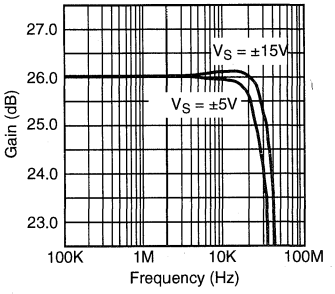
Typical Performance Curves — Contd.

Gain Flatness
V_S = ±5V, A_V = 20 dB,
R_F/R_G as Shown



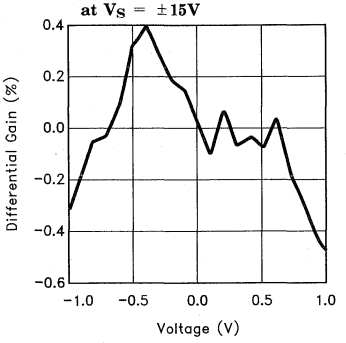
4390-11

Gain Flatness
V_S = ±5V, A_V = 26 dB,
R_F = 680Ω, R_G = 36Ω



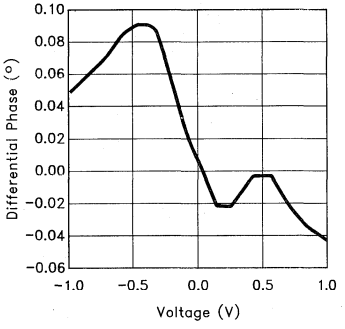
4390-12

Differential Gain
at V_S = ±15V



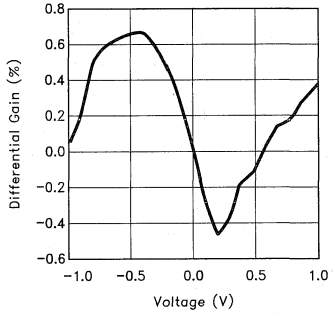
4390-17

Differential Phase
at V_S = ±15V



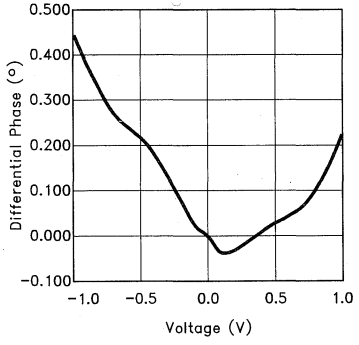
4390-18

Differential Gain
at V_S = ±5V



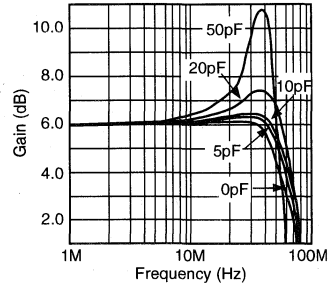
4390-19

Differential Phase
at V_S = ±5V



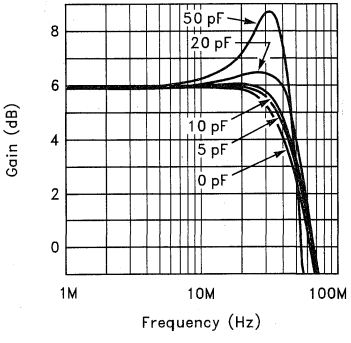
4390-20

Frequency Response
for Various C_{LOAD}, V_S = ±15V,
R_F = R_G = 1300Ω



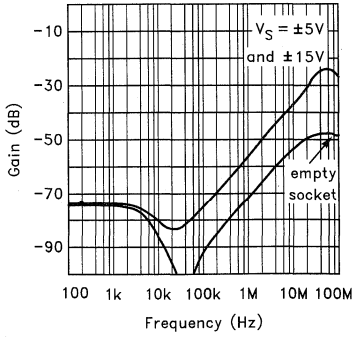
4390-13

Frequency Response
for Various C_{LOAD}, V_S = ±5V,
R_F = R_G = 1300Ω



4390-14

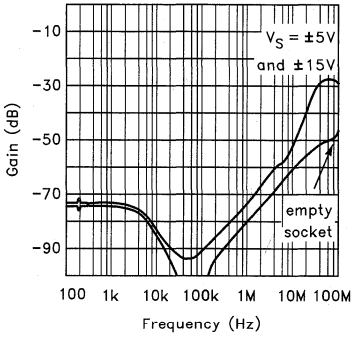
Crosstalk,
Channel R and B to Channel G,
V_S = ±5V, R_F = 1300Ω



4390-15

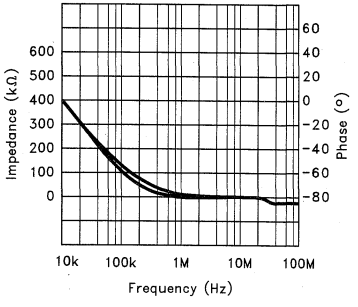
Typical Performance Curves — Contd.

Crosstalk, Channel R and G to Channel B, $V_S = \pm5V$, $R_F = 1300\Omega$



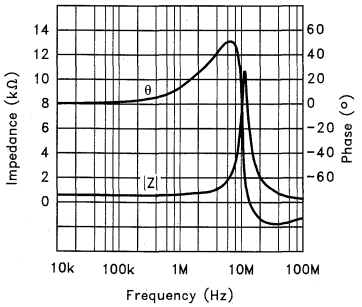
4390-16

I_N+ Input Impedance during HOLD, $V_S = \pm5V$



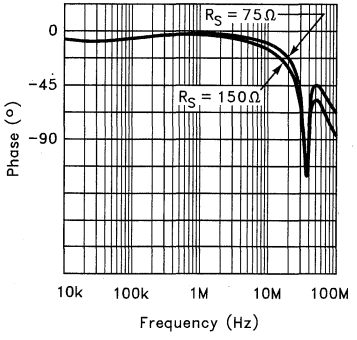
4390-21

I_N+ Input Impedance during SAMPLE, $V_S = \pm5V$



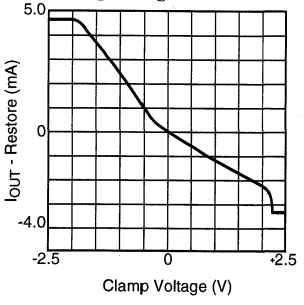
4390-22

Phase Shift at I_N+ Pin during Restore, $R_S = 75\Omega$ and 150Ω, $V_S = \pm5V$



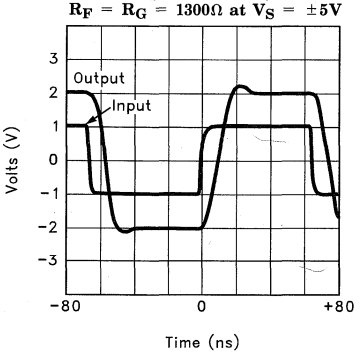
4390-23

I_{OUT} Restoring vs Clamp, Voltage at $V_S = \pm5V$



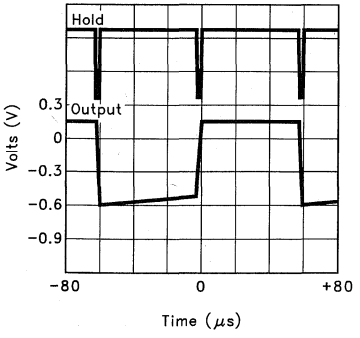
4390-24

Pulse Response with $A_V = 2$, $R_F = R_G = 1300\Omega$ at $V_S = \pm5V$



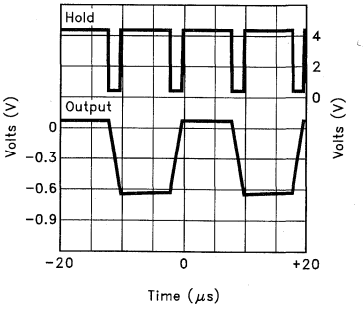
4390-25

Output during DC-Restoration, Showing DC Droop $R_F = R_G = 1300\Omega$, $V_S = \pm5V$



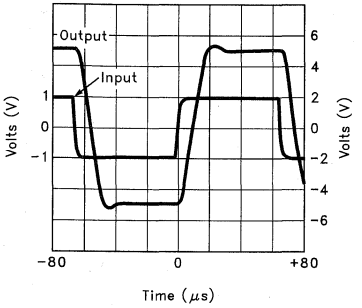
4390-26

Output during DC-Restoration, $R_F = R_G = 1300\Omega$, $V_S = \pm5V$



4390-27

Pulse Response with $A_V = 5$, $R_F = 820\Omega$ and $R_G = 200\Omega$ at $V_S = \pm15V$

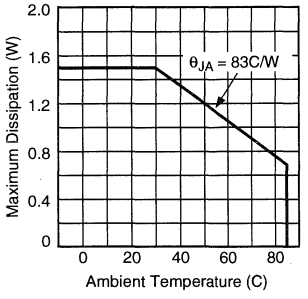


4390-28

EL4390C
Triple 80 MHz Video Amplifier with DC Restore

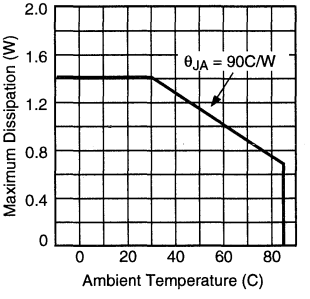
Typical Performance Curves — Contd.

Maximum Power Dissipation vs Ambient Temperature— 16-Pin PDIP

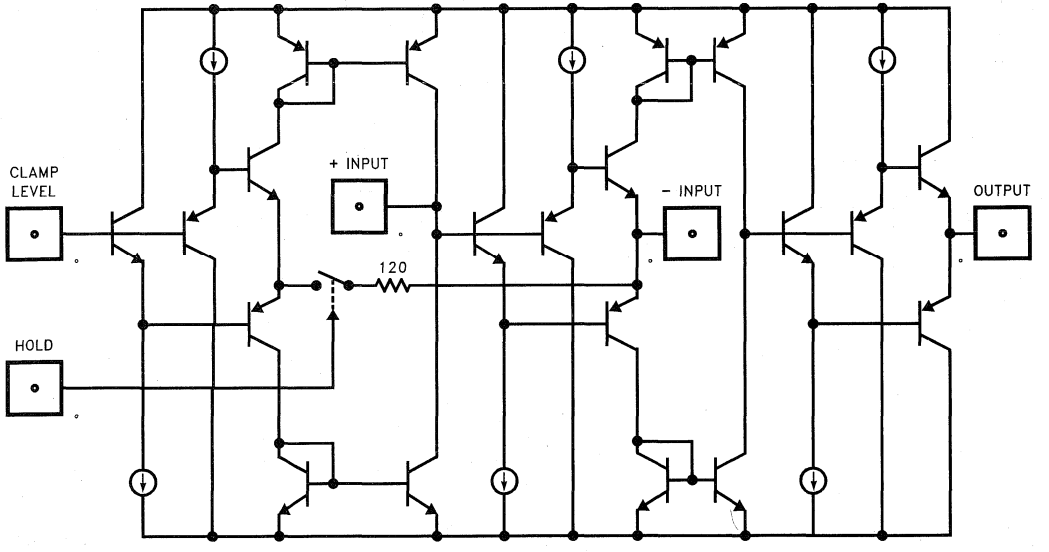


4390-29

Maximum Power Dissipation vs Ambient Temperature— 16-Pin SOL



4390-30



4390-31

Simplified Schematic of One Channel of EL4390

Applications Information

Circuit Operation

Each channel of the EL4390 contains a current feedback amplifier and a TTL/CMOS compatible clamp circuit. The current that the clamp can source or sink into the non-inverting input is approximately:

$$I = (V_{CLAMP} - V_{IN+}) / 120$$

So, when the non-inverting input is at the same voltage as the clamp reference, no current will flow, and hence no charge is added to the capacitor. When there is a difference in voltage, current will flow, in an attempt to cancel the error AT THE NON-INVERTING input. The amplifier's offset voltage and ($I_{B-} \times R_F$) DC errors are not cancelled with this loop. It is purely a method of adding a controlled DC offset to the signal.

As well as the offset voltage error, which goes up with gain, and the $I_{B-} \times R_F$ error which drops with gain, there is also the I_{B+} error term. Since the amplifier is capacitively coupled, this small current is slowly integrated and shows up as a very slow ramp voltage. Table below shows the output voltage drift in 60μS for various values of coupling capacitor, all assuming the very worst I_{B+} current.

Table 1. Charge Storage Capacitor Value vs. Droop and Charging Rates

Cap Value (nF)	Droop in 60μS (mV)	Charge in 2μS (mV)	Charge in 4μS (mV)
10	30	400	800
22	13.6	182	364
47	6.4	85	170
100	3.0	40	80
220	1.36	18	36

In normal circuit operation, the picture content will also cause a slow change in voltage across the capacitor, so at every back porch time period, these error terms can be corrected.

When a signal source is being switched, eg. from two different surveillance cameras, it is recommended to synchronize the switching with the vertical blanking period, and to drive the HOLD pin (pin 6) low, during these lines. This will ensure that the system has been completely restored, regardless of the average intensity of the two pictures.

Application Hints

Figures 1 & 2 shows a three channel DC-restoring system, suitable for R-G-B or Y-U-V component video, or three synchronous composite signals.

Figure 1 shows the amplifiers configured for non-inverting gain, and Figure 2 shows the amplifiers configured for inverting gains. Note that since the DC-restoring function is accomplished by clamping the amplifier's non-inverting input, during the back porch period, any signal on the non-inverting input will be distorted. For this reason, it is recommended to use the inverting configuration for composite video, since this avoids the color burst being altered during the clamp time period.

Since all three amplifiers are monolithic, they run at the same temperature, and will have very similar input bias currents. This can be used to advantage, in situations where the droop voltage needs to be compensated, since a single trim circuit can be used for all three channels. A 560KΩ or similar value resistor helps to isolate each signal. See Figure 2. The advantage of compensating for the droop voltage, is that a smaller capacitor can be used, which allows a larger level restoration within one line. See Table 1 for values of capacitor and charge/droop rates.

EL4390C
Triple 80 MHz Video Amplifier with DC Restore

Applications Information — Contd.

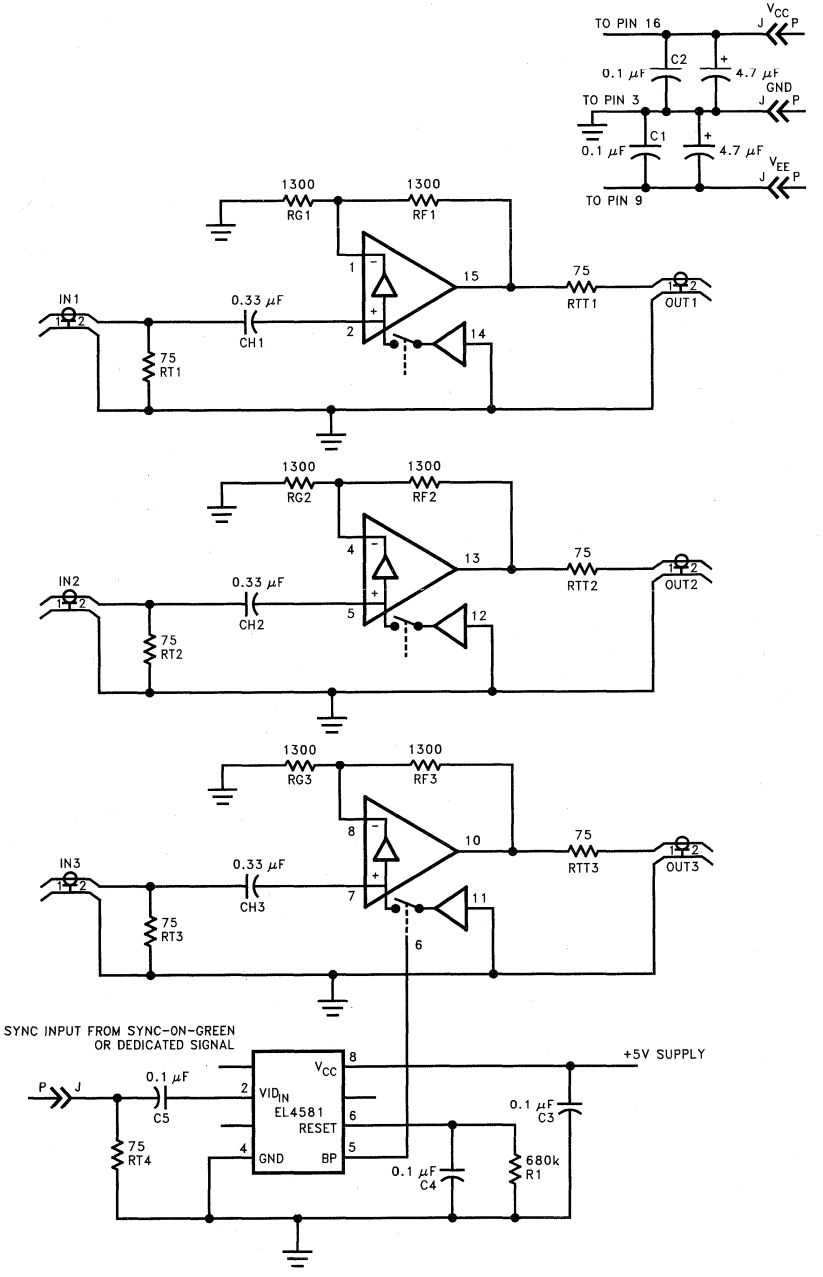
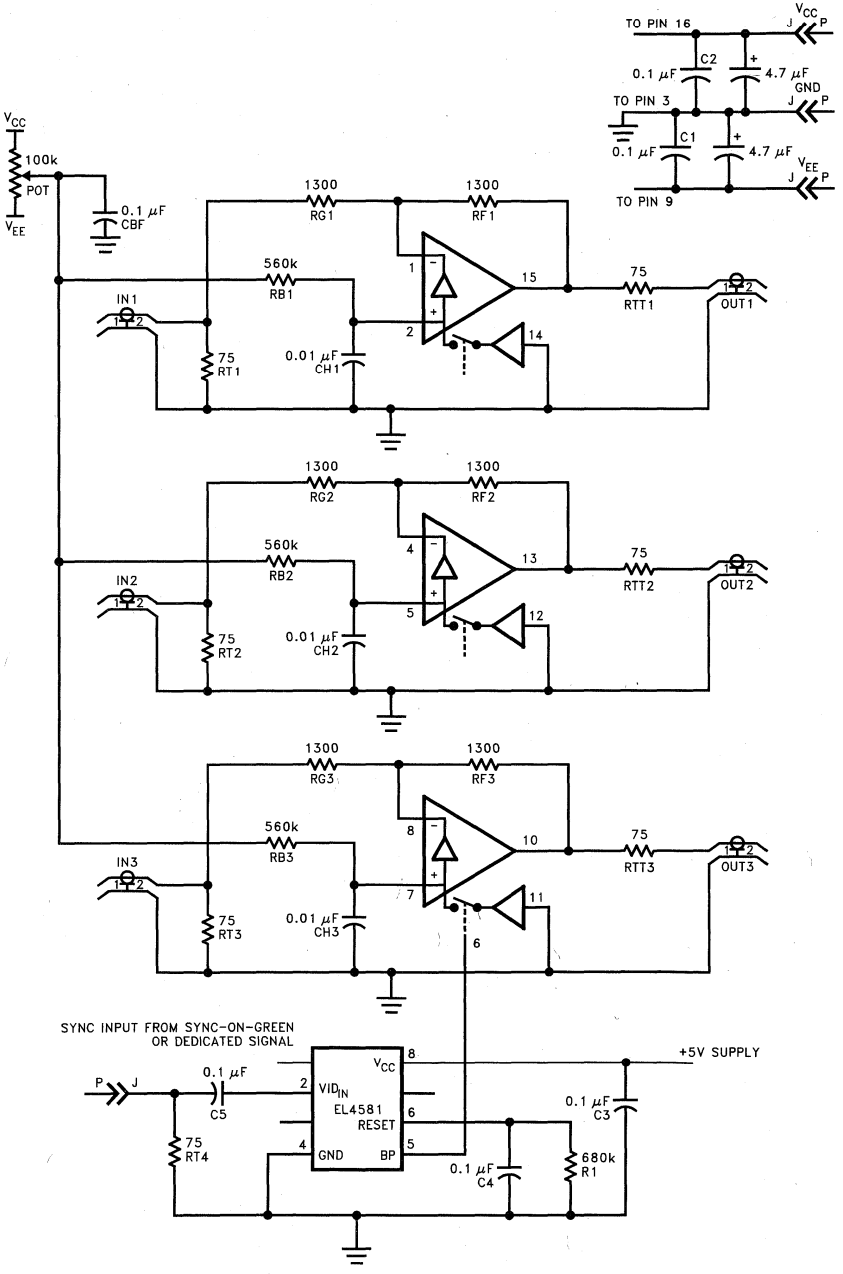


Figure 1

Applications Information — Contd.



4390-33

Figure 2

EL4390C
Triple 80 MHz Video Amplifier with DC Restore

Applications Information — Contd.

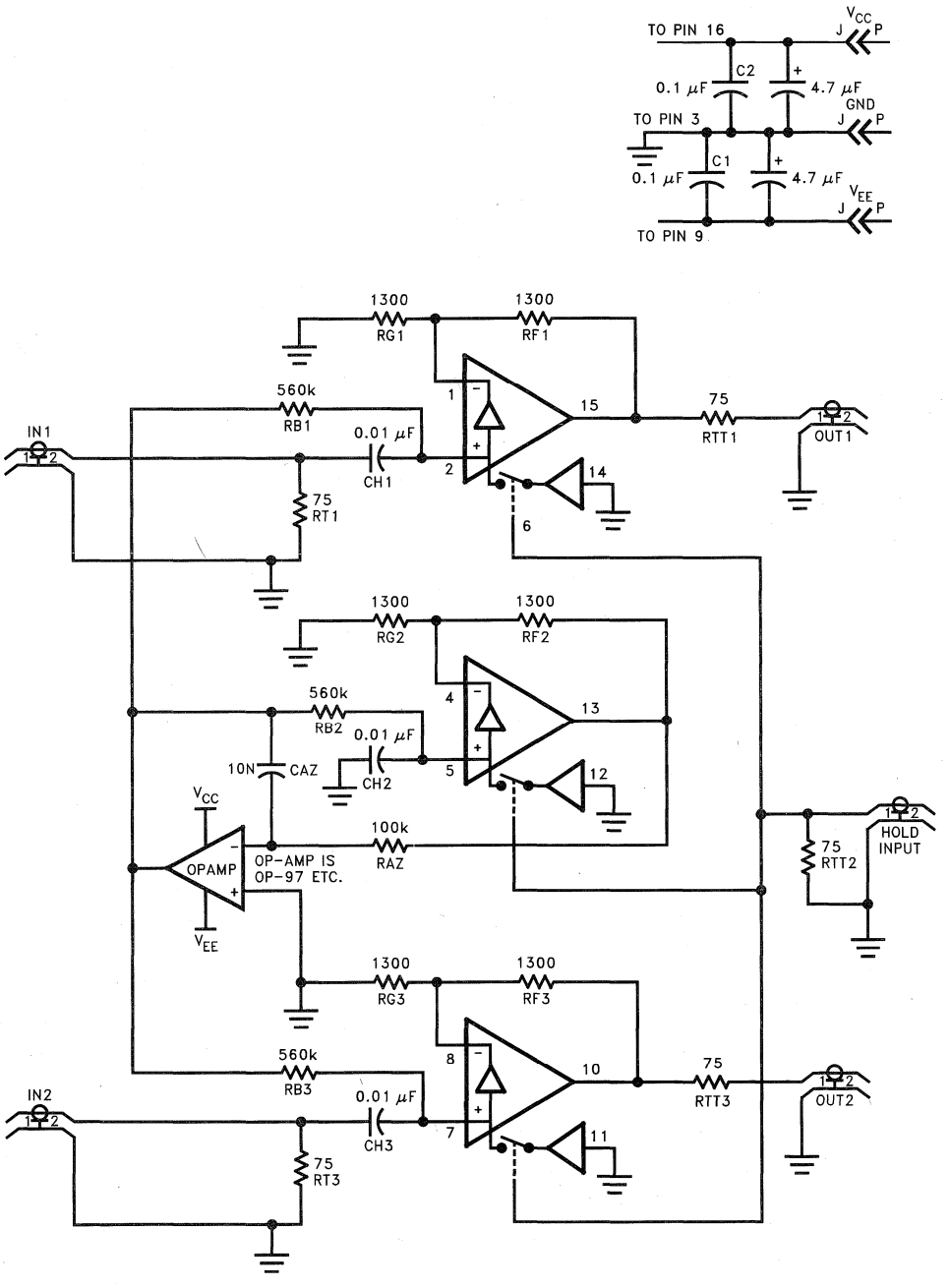


Figure 3

Applications Information — Contd.

In Figure 3, one of the three channels is used, together with a low-offset op-amp, to automatically trim the bias current of the other two channels. The two remaining channels are shown in the non-inverting configuration, but could equally well be set to provide inverting gains. Two DC-restored channels are typically needed in fader applications. See the EL4094 and EL4095 for suitable, monolithic video faders.

Layout and Dissipation Considerations

As with all high frequency circuits, the supplies should be bypassed with a 0.1μF ceramic capacitor very close to the supply pins, and a 4.7μF tantalum capacitor fairly close, to handle the high current surges. While a ground plane is recommended, the amplifier will work well with a "star" grounding scheme. The pin 3 ground is only used for the internal bias generator and the reference for the TTL compatible "HOLD" input.

As with all current feedback capacitors, all stray capacitance to the inverting inputs should be kept as low as possible, to avoid unwanted peaking at the output. This is especially true if the value of Rf has already been reduced to raise the bandwidth of the part, while tolerating some peaking. In this situation, additional capacitance on the inverting input can lead to an unstable amplifier.

Since there are three amplifiers all in one package, and each amplifier can sink or source typically more than 70mA, some care is needed to avoid excessive die temperatures. Sustained, DC currents, of over 30mA, are not recommended, due to the limited current handling capability of the metal traces inside the IC. Also, the short circuit protection can be tripped with currents as low as 45mA, which is seen as excessive distortion in the output waveform. As a quick rule of thumb, both the SOL and DIP 16 pin packages can dissipate about 1.4 watts at 25°C, and with ±15V supplies and a worst case quiescent current of 32mA, yields 0.96 watts, before any load is driven.

Dissipation of the EL4390 can be reduced by lowering the supply voltage. Although some performance is degraded at lower supplies, as seen in the characteristic curves, it is often found to be a useful compromise. The bandwidth can be recovered, by reducing the value of R_F, and R_G as appropriate.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4421C/22C/41C/42C/43C/44C
Multiplexed-Input Video Amplifiers

Features

- Unity or + 2-gain bandwidth of 80 MHz
- 70 dB off-channel isolation at 4 MHz
- Directly drives high-impedance or 75Ω loads
- .02% and .02° differential gain and phase errors
- 8 ns switching time
- <100 mV switching glitch
- 0.2% loaded gain error
- Compatible with ±3V to ±15V supplies
- 160 mW maximum dissipation at ±5V supplies

Ordering Information

Part No.	Temp. Range	Package	Outline
EL4421CN	−40°C to +85°C	8-Pin PDIP	MDP0031
EL4421CS	−40°C to +85°C	8-Pin SO	MDP0027
EL4422CN	−40°C to +85°C	8-Pin PDIP	MDP0031
EL4422CS	−40°C to +85°C	8-Pin SO	MDP0027
EL4441CN	−40°C to +85°C	14-Pin PDIP	MDP0031
EL4441CS	−40°C to +85°C	14-Pin SO	MDP0027
EL4442CN	−40°C to +85°C	14-Pin PDIP	MDP0031
EL4442CS	−40°C to +85°C	14-Pin SO	MDP0027
EL4443CN	−40°C to +85°C	14-Pin PDIP	MDP0031
EL4443CS	−40°C to +85°C	14-Pin SO	MDP0027
EL4444CN	−40°C to +85°C	14-Pin PDIP	MDP0031
EL4444CS	−40°C to +85°C	14-Pin SO	MDP0027

General Description

The EL44XX family of video multiplexed-amplifiers offers a very quick 8 ns switching time and low glitch along with very low video distortion. The amplifiers have good gain accuracy even when driving low-impedance loads. To save power, the amplifiers do not require heavy loading to remain stable.

The EL4421 and EL4422 are two-input multiplexed amplifiers. The -inputs of the input stages are wired together and the device can be used as a pin-compatible upgrade from the MAX453.

The EL4441 and EL4442 have four inputs, also with common feedback. These may be used as upgrades of the MAX454.

The EL4443 and EL4444 are also 4-input multiplexed amplifiers, but both positive and negative inputs are wired separately. A wide variety of gain- and phase-switching circuits can be built using independent feedback paths for each channel.

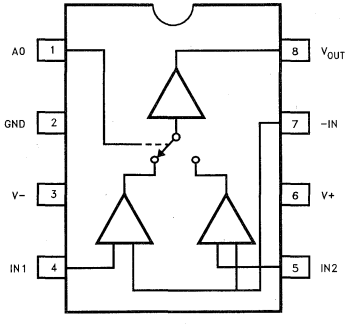
The EL4421, EL4441, and EL4443 are internally compensated for unity-gain operation. The EL4422, EL4442, and EL4444 are compensated for gains of + 2 or more, especially useful for driving back-matched cables.

The amplifiers have an operational temperature of −40°C to +85°C and are packaged in plastic 8- and 14-pin DIP and 8- and 14-pin SO.

The EL44XX multiplexed-amplifier family is fabricated with Elantec's proprietary complementary bipolar process which gives excellent signal symmetry and is very rugged.

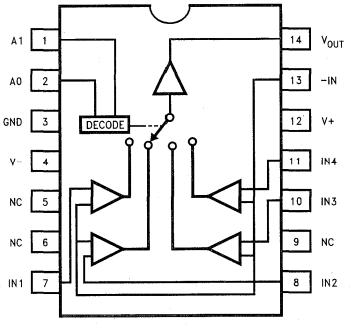
Connection Diagrams

EL4421/EL4422



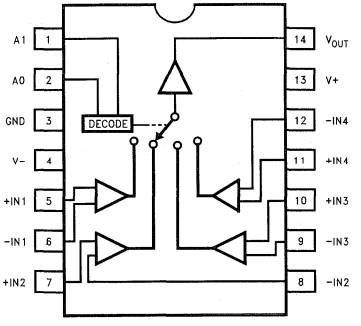
4421-1

EL4441/EL4442



4421-2

EL4443/EL4444



4421-3

Absolute Maximum Ratings

V+	Positive Supply Voltage	16.5V	V_{LOGIC}	Voltage at A0 or A1	−4V to 6V
V_S	V+ to V− Supply Voltage	33V	I_{IN}	Current into any Input,	4 mA
V_{IN}	Voltage at any Input or Feedback	V+ to V−		Feedback, or Logic Pin	
ΔV_{IN}	Difference between Pairs of		I_{OUT}	Output Current	30 mA
	Inputs or Feedback	6V	P_D	Maximum Power Dissipation	See Curves

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open-Loop DC Electrical Characteristics

Power supplies at ±5V, T_A = 25°C, R_L = 500Ω, unless otherwise specified

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage '21, '41, and '43	−9	±3	9	I	mV
	'22, '42, and '44	−7	±2	7	I	
I_B	Input Bias Current, Positive Inputs Only of the '21, '22, '41, '42, and All Inputs of the '43 and '44	−12	−5	0	I	µA
I_{FB}	Input Bias Currents of Common Feedback					
	−'21 and '22	−24	−10	0	I	µA
	−'41 and '42	−48	−20	0	I	µA
I_{OS}	Input Offset Currents of the '43 and '44		60	350	I	nA
E_G	Gain Error of the '21 and '41 and '43		0.2	0.6	I	%
	(Note 1) '22, '42 and '44		0.1	0.6	I	V/V
A_{VOL}	Open-Loop Gain EL4443	350	500		I	V/V
	(Note 1) EL4444	500	750		I	V/V
V_{IN}	Input Signal Range, EL4421 and EL4441 (Note 2)	±2.5	±3		I	V
CMRR	Common-Mode Rejection Ratio, EL4443 and EL4444	70	90		I	dB
PSRR	Power Supply Rejection Ratio V_s from ±5V to ±15V	60	70		I	dB

Open-Loop DC Electrical Characteristics — Contd.

Power supplies at ±5V, T_A = 25°C

Parameter	Description	Min	Typ	Max	Test Level	Units
CMIR	Common-Mode Input Range (Note 3) EL4443 and EL4444	±2.5	±3		I	V
V_{OUT}	Output Swing	±2.5	±3.5		I	V
I_{SC}	Output Short-Circuit Current	±40	±80		I	mA
F_T	Unselected Channel Feedthrough '21, '41, '43	70	80		I	dB
	Attenuation, (Note 1) '22, '42, '44	55	64		I	dB
I_{LOGIC}	Input Current at A0 and A1 with Input = 0V and 5V	−16	−8	0	I	µA
V_{LOGIC}	Logic Valid High and Low Input Levels	0.8		2.0	I	V
I_S	Supply Current EL4421 and EL4422		11	14	I	mA
	EL4441, EL4442, EL4443, and EL4444		13	16		

Note 1: The '21, '41, and '43 devices are connected for unity-gain operation with 75Ω load and an input span of ±1V. The '22, '42, and '44 devices are connected for a gain of +2 with a 150Ω load and a ±1V input span with R_F = R_G = 270Ω.

Note 2: The '21 and '41 devices are connected for unity gain with a ±3V input span while the output swing is measured.

Note 3: CMIR is assured by passing the CMRR test at input voltage extremes.

Closed-Loop AC Electrical Characteristics

Power supplies at ±5V. T_A = 25°C, for EL4421, EL4441, and EL4443 A_V = +1 and R_L = 500Ω, for EL4422, EL4442, and EL4444 A_V = +2 and R_L = 150Ω with R_F = R_G = 270Ω and C_F = 3 pF; for all C_L = 15 pF

Parameter	Description	Min	Typ	Max	Test Level	Units
BW − 3 dB	−3 dB Small-Signal Bandwidth, EL4421, '41, '43		80		V	MHz
	EL4422, '42, '44		65		V	MHz
BW ± 0.1 dB	0.1 dB Flatness Bandwidth		10		V	MHz
Peaking	Frequency Response Peaking		0.5		V	dB
SR	Slewrate, V_{OUT} between −2.5V and +2.5V, V_S = ±12V					
	EL4421, EL4441, EL4443	150	200		I	V/µsec
	EL4422, EL4442, EL4444	180	240		I	V/µsec
V_n	Input-Referred Noise Voltage Density					
	EL4421, EL4441, EL4443		18		V	nV/rt-hz
	EL4422, EL4442, EL4444		14		V	nV/rt-hz
d_G	Differential Gain Error, V_{OFFSET} between −0.7V and +0.7V					
	EL4421, EL4441, EL4443 (V_S = ±12V)		0.01		V	%
	EL4421, EL4441, EL4443 (V_S = ±5V)		0.10		V	%
	EL4422, EL4442, EL4444 (V_S = ±12V)		0.02		V	%
	EL4422, EL4442, EL4444 (V_S = ±5V)		0.03		V	%

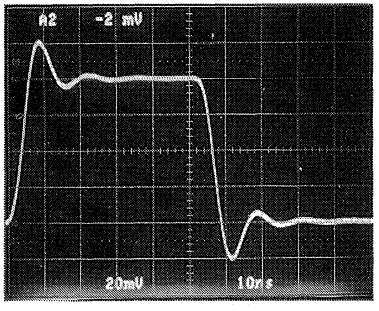
Closed-Loop AC Electrical Characteristics

Power supplies at ±5V. T_A = 25°C, for EL4421, EL4441, and EL4443 A_V = +1 and R_L = 500Ω, for EL4422, EL4442, and EL4444 A_V = 2 and R_L = 150Ω with R_F = R_G = 270Ω and C_F = 3 pF; for all C_L = 15 pF — Contd.

Parameter	Description	Min	Typ	Max	Test Level	Units
dØ	Differential Phase Error, V_{OFFSET} between −0.7V and +0.7V					
	EL4421, EL4441, EL4443 (V_S = ±12V)		0.01		V	°
	EL4421, EL4441, EL4443 (V_S = ±5V)		0.01		V	°
	EL4422, EL4442, EL4444 (V_S = ±12V)		0.02		V	°
	EL4422, EL4442, EL4444 (V_S = ±5V)		0.15		V	°
T_{MUX}	Multiplex Delay Time, Logic Threshold to 50% Signal Change					
	EL4421, '22		8		V	nsec
	EL4441, '42, '43, '44		12		V	nsec
V_{GLITCH}	Peak Multiplex Glitch					
	EL4421, '22		70		V	mV
	EL4441, '42, '43, '44		100		V	mV
ISO	Channel Off Isolation at 3.58 MHz (See Text)					
	EL4421, EL4441, EL4443		76		V	dB
	EL4422, EL4442, EL4444		63		V	dB

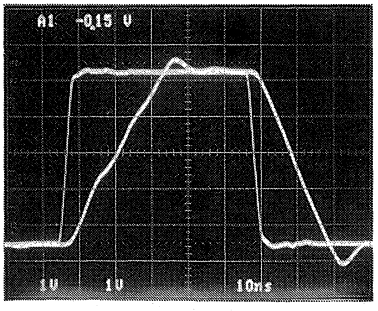
Typical Performance Curves

EL4421, EL4441, and EL4443
Small-Signal Transient Response
V_S = ±5V, R_L = 500Ω



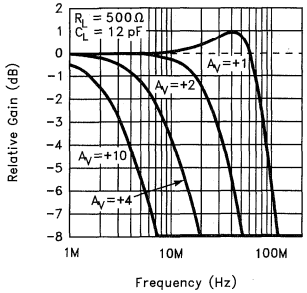
4421-5

EL4421, EL4441, and EL4443
Large-Signal Response
V_S = ±12V, R_L = 500Ω



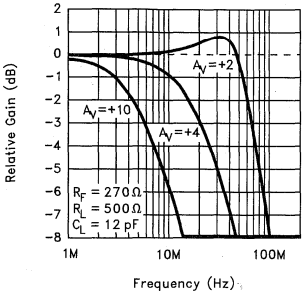
4421-6

EL4421, EL4441, and EL4443
Frequency Response for Various Gains



4421-7

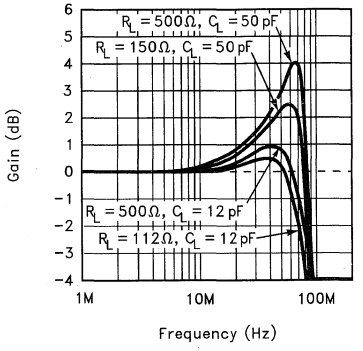
EL4422, EL4442, and EL4444
Frequency Response for Various Gains



4421-8

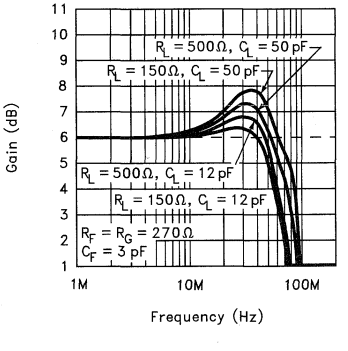
Typical Performance Curves — Contd.

EL4421, EL4441, and EL4443
Frequency Response for Various Loads
$V_S = \pm 5V$, $A_V = +1$



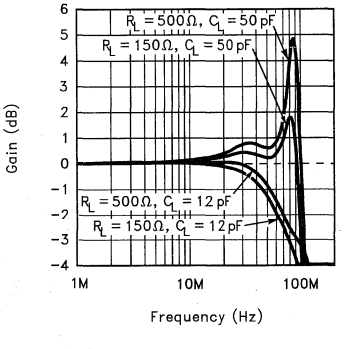
4421-9

EL4422, EL4442, and EL4444
Frequency Response for Various Loads
$V_S = \pm 5V$, $A_V = +2$



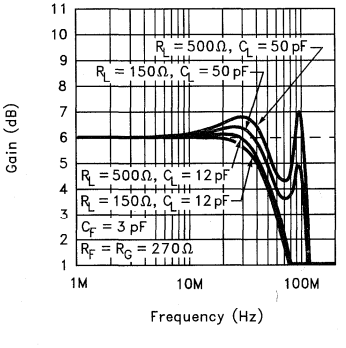
4421-10

Frequency Response
for Various Loads
$V_S = \pm 15V$, $A_V = +1$



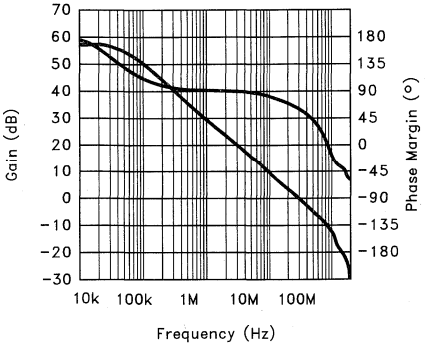
4421-11

EL4422, EL4442, and EL4444
Frequency Response for Various Loads
$V_S = \pm 15V$, $A_V = +2$



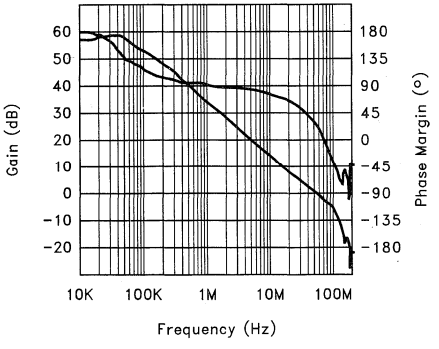
4421-12

EL4443 Open-Loop Gain and
Phase vs Frequency



4421-13

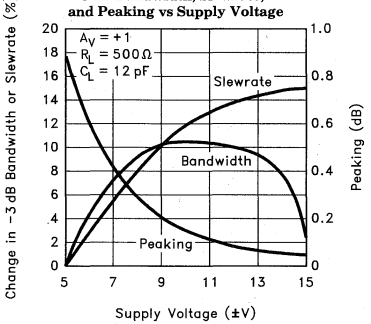
EL4444 Open-Loop Gain and
Phase vs Frequency



4421-37

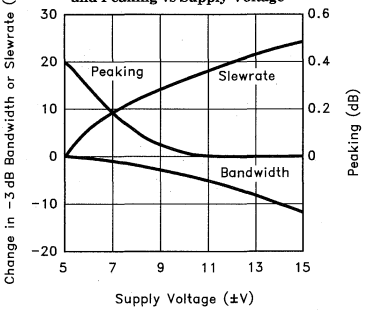
Typical Performance Curves — Contd.

EL4421, EL4441, and EL4443 −3 dB Bandwidth, Slewrate, and Peaking vs Supply Voltage



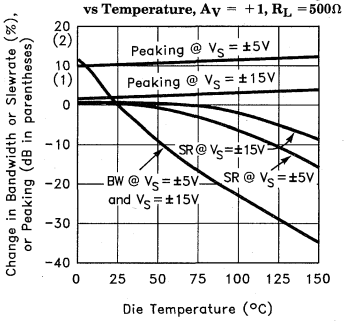
4421-14

EL4422, EL4442, and EL4444 −3 dB Bandwidth, Slewrate, and Peaking vs Supply Voltage



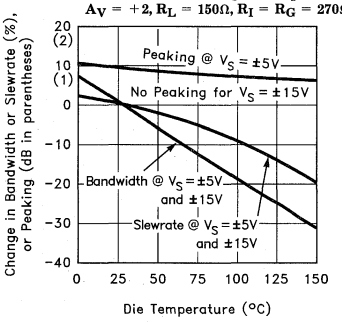
4421-15

EL4421, EL4441, and EL4443 Bandwidth, Slewrate, and Peaking vs Temperature, A_V = +1, R_L = 500Ω



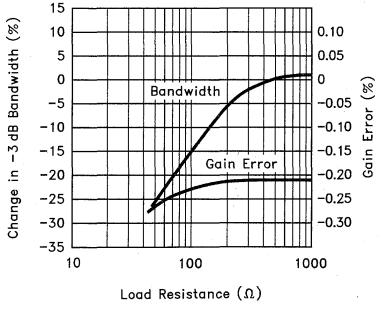
4421-16

EL4422, EL4442, and EL4444 Bandwidth, Slewrate, and Peaking vs Temperature, A_V = +2, R_L = 150Ω, R_I = R_G = 270Ω, C_F = 3 pF



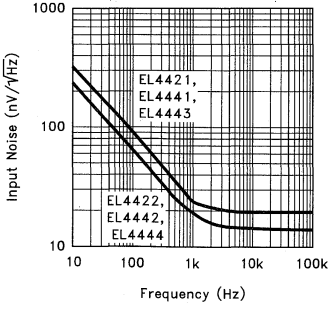
4421-17

EL4421, EL4441, and EL4443 −3 dB Bandwidth and Gain Error vs Load Resistance



4421-18

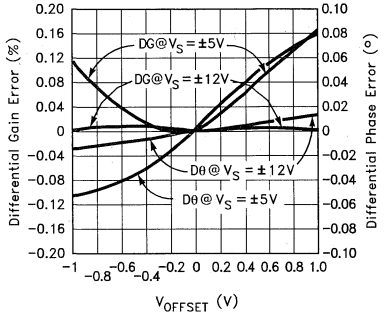
Input Noise vs Frequency



4421-19

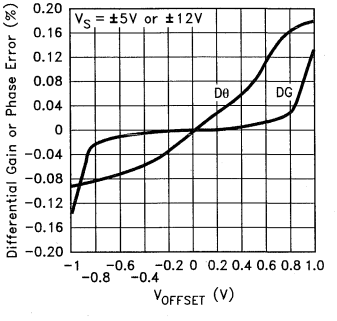
Typical Performance Curves — Contd.

EL4421, EL4441, and EL4443 Differential Gain and Phase Errors, vs Input Offset, A_V = +1, R_L = 500Ω, F = 3.58 MHz



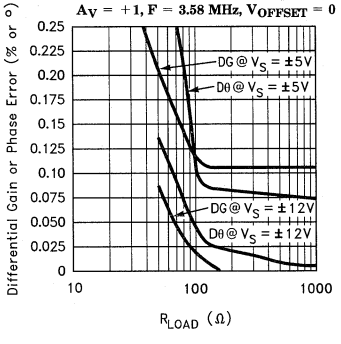
4421-20

EL4422, EL4442, and EL4444 Differential Gain and Phase Error vs Input Offset; A_V = +2, R_L = 150Ω, F = 3.58 MHz



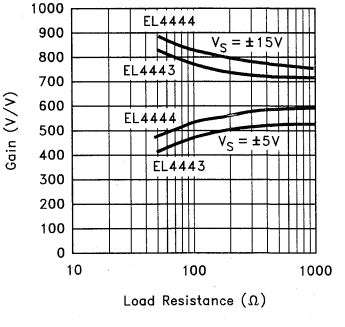
4421-21

EL4421, EL4441, and EL4443 Differential Gain and Phase Error vs Load Resistance; A_V = +1, F = 3.58 MHz, V_{OFFSET} = 0 → 0.714V



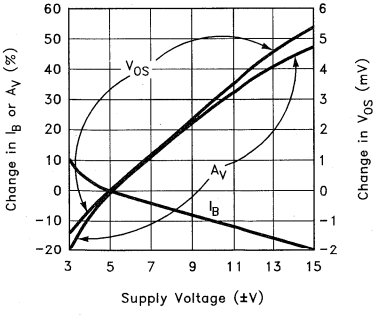
4421-22

EL4443 and EL4444 Open-Loop Gain vs Load Resistance



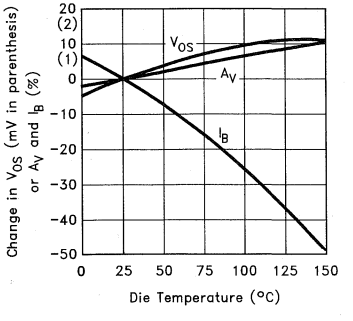
4421-23

Change in V_{OS}, A_V, and I_B with Supply Voltage



4421-24

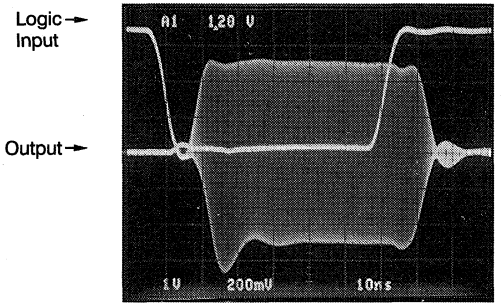
Change in V_{OS}, I_B, and A_V vs Temperature



4421-25

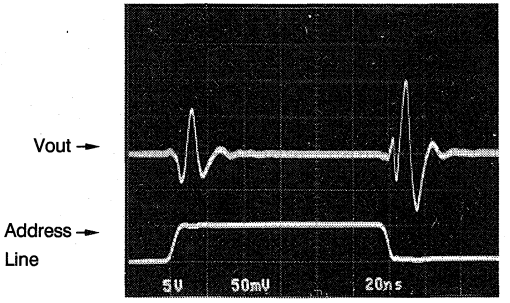
Typical Performance Curves — Contd.

Switching Waveforms
Switching from Grounded Input to Uncorrelated Sinewave and Back



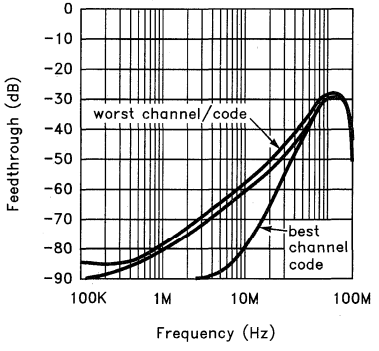
4421-26

Channel-to-Channel Switching Glitch



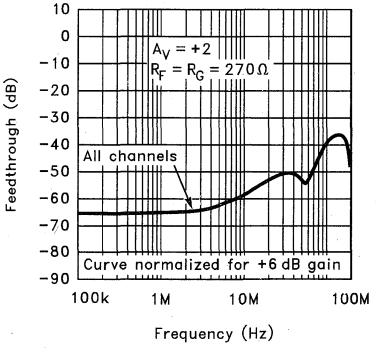
4421-27

EL4421, EL4441, and EL4443
Unselected Channel Feedthrough vs Frequency



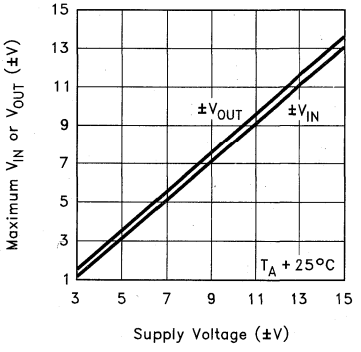
4421-28

EL4422, EL4442, and EL4444
Unselected Channel Feedthrough vs Frequency



4421-29

EL4443 and EL4444
Input and Output Range vs Supply Voltage (Output Unloaded)

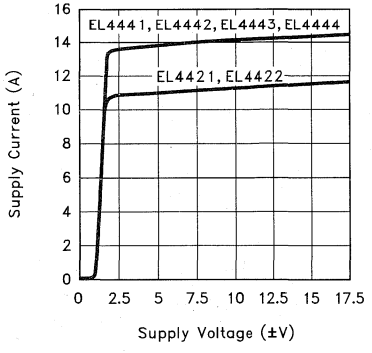


4421-30

EL4421C/22C/41C/42C/43C/44C
Multiplexed-Input Video Amplifiers

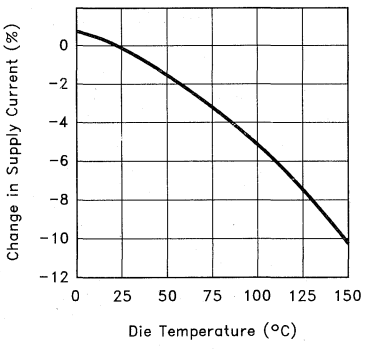
Typical Performance Curves — Contd.

Supply Current vs Supply Voltage



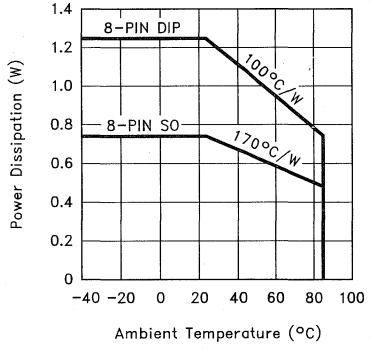
4421-31

Supply Current vs Temperature



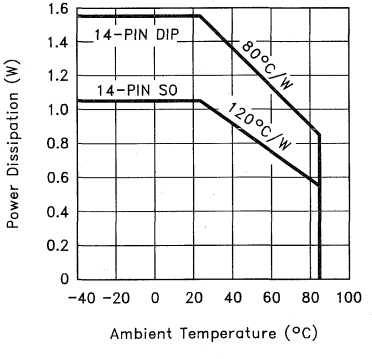
4421-32

8-Pin Package Power Dissipation vs Ambient Temperature



4421-33

14-Pin Package Power Dissipation vs Ambient Temperature



4421-34

Applications Information

General Description

The EL44XX family of video mux-amps are composed of two or four input stages whose inputs are selected and control an output stage. One of the inputs is active at a time and the circuit behaves as a traditional voltage-feedback op-amp for that input, rejecting signals present at the unselected inputs. Selection is controlled by one or two logic inputs.

The EL4421, EL4422, EL4441, and EL4442 have all −inputs wired in parallel, allowing a single feedback network to set the gain of all inputs. These devices are wired for positive gains. The EL4443 and EL4444, on the other hand, have all +inputs and −inputs brought out separately so that the input stage can be wired for independent gains and gain polarities with separate feedback networks.

The EL4421, EL4441, and EL4443 are compensated for unity-gain stability, while the EL4422, EL4442, and EL4444 are compensated for a feedback gain of +2, ideal for driving back-terminated cables or maintaining bandwidth at higher fed-back gains.

Applications Information — Contd.

Switching Characteristics

The logic inputs work with standard TTL levels of 0.8V or less for a logic 0 and 2.0V or more for a logic 1, making them compatible for TTL and CMOS drivers. The ground pin is the logic threshold biasing reference. The simplified input circuitry is shown below:

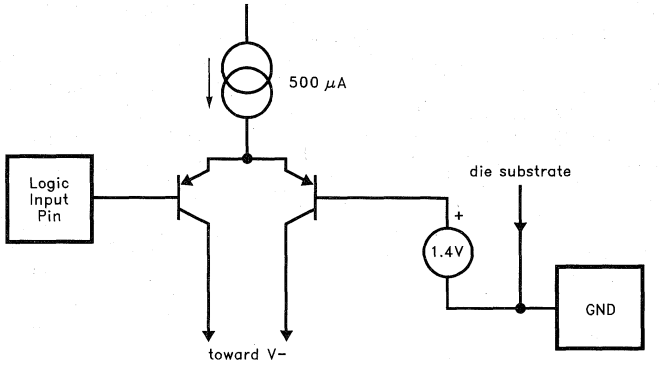


Figure 1. Simplified Logic Input Circuitry

The ground pin draws a maximum DC current of 6 μA, and may be biased anywhere between (V−) +2.5V and (V+) −3.5V. The logic inputs may range from (V−)+2.5V to V+, and are additionally required to be no more negative than V(Gnd pin)−4V and no more positive than V(Gnd pin)+6V.

For example, within these constraints, we can power the EL44XX's from +5V and +12V without a negative supply by using these connections:

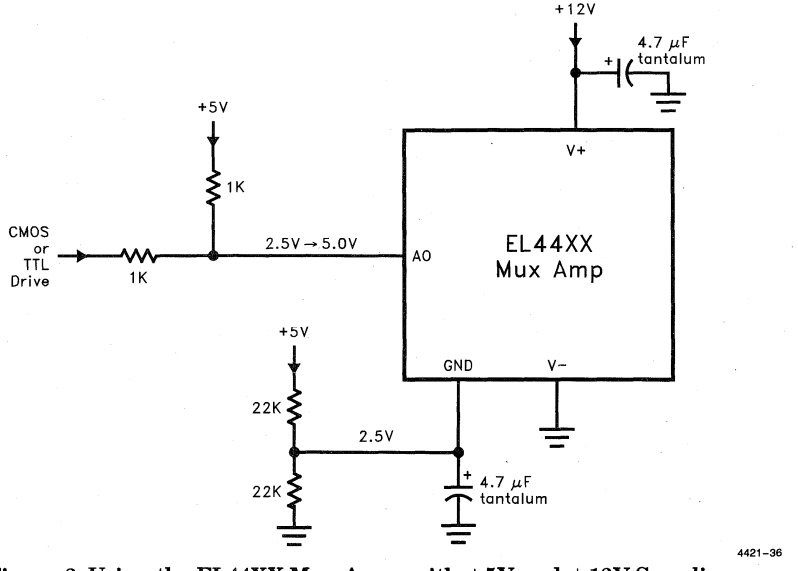


Figure 2. Using the EL44XX Mux Amps with +5V and +12V Supplies

Applications Information — Contd.

The logic input(s) and ground pin are shifted 2.5V above system ground to correctly bias the mux-amp. Of course, all the signal inputs and output will have to be shifted 2.5V above system ground to ensure proper signal path biasing.

A final caution: the ground pin is also connected to the IC's substrate and frequency compensation components. The ground pin must be returned to system ground by a short wire or nearby bypass capacitor. In figure 2, the 22 KΩ resistors also serve to isolate the bypassed ground pin from the +5V supply noise.

Signal Amplitudes

Signal input and output voltages must be between (V−)+2.5V and (V+)−2.5V to ensure linearity. Additionally, the differential voltage on any input stage must be limited to ±6V to prevent damage. In unity-gain connections, any input could have ±3V applied and the output would be at ±3V, putting us at our 6V differential limit. Higher-gain circuit applications divide the output voltage and allow for larger outputs. For instance, at a gain of +2 the maximum input is again ±3V and the output swing is ±6V. The EL4443 or EL4444 can be wired for inverting gain with even more amplitude possible.

The output and positive inputs respond to overloading amplitudes correctly; that is, they simply clamp and remain monotonic with increasing +input overdrive. A condition exists, however, where the −input of an active stage is overdriven by large outputs. This occurs mainly in unity-gain connections, and only happens for negative inputs. The overloaded input cannot control the feedback loop correctly and the output can become non-monotonic. A typical scenario has the circuit running on ±5V supplies, connected for unity gain, and the input is the maximum ±3V. Negative input extremes can cause the output to jump from −3V to around −2.3V. This will never happen if the input is restricted to ±2.5V, which is the guaranteed maximum input compliance with ±5V supplies, and is not a problem with greater supply voltages. Connecting the feedback network with a divider will prevent the overloaded output voltage from being large enough to overload the −input and monotonic

Applications Information — Contd.

behavior is assured. In any event, keeping signals within guaranteed compliance limits will assure freedom from overload problems.

The input and output ranges are substantially constant with temperature.

Power Supplies

The mux-amps work well on any supplies from ±3V to ±15V. The supplies may be of different voltages as long as the requirements of the Gnd pin are observed (see the Switching Characteristics section for a discussion). The supplies should be bypassed close to the device with short leads. 4.7 μF tantalum capacitors are very good, and no smaller bypasses need be placed in parallel. Capacitors as small as 0.01 μF can be used if small load currents flow.

Single-polarity supplies, such as +12V with +5V can be used as described in the Switching Characteristics section. The inputs and outputs will have to have their levels shifted above ground to accommodate the lack of negative supply.

The dissipation of the mux-amps increases with power supply voltage, and this must be compatible with the package chosen. This is a close estimate for the dissipation of a circuit:

$$P_D = 2V_S \times I_s,max + (V_S - V_O) \times V_O / R_{PAR}$$

Where I_s, max is the maximum supply current

V_S is the ± supply voltage (assumed equal)

V_O if the output voltage

R_{PAR} is the parallel of all resistors loading the output

For instance, the EL4422 draws a maximum of 14 mA and we might require a 2V peak output into 150Ω and a 270Ω +270Ω feedback divider. The R_{PAR} is 117Ω. The dissipation with ±5V supplies is 191 mW. The maximum Supply voltage that the device can run on for a given P_D and the other parameter is

$$V_S, max = (P_D + V_O^2/R_{PAR})/2Is + V_O/R_{PAR})$$

The maximum dissipation a package support is

$$P_D, max = (T_D, max - T_A, max)/R_{TH}$$

Where T_D, max is the maximum die temperature, 150°C for reliability, less to retain optimum electrical performance

T_A, max is the ambient temperature, 70° for commercial and 85°C for industrial range

R_{TH} is the thermal resistance of the mounted package, obtained from data sheet dissipation curves

The most difficult case is the SO-8 package. With a maximum die temperature of 150°C and a maximum ambient temperature of 85°, the 65° temperature rise and package thermal resistance of 170°/W gives a maximum dissipation of 382 mW. This allows a maximum supply voltage of ±9.2V for the EL4422 operated in our example. If the EL4421 were driving a light load ($R_{PAR} \rightarrow \infty$), it could operate on ±15V supplies at a 70° maximum ambient.

The EL4441 through EL4444 can operate on ±12V supplies in the SO package, and all parts can be powered by ±15V supplies in DIP packages.

Output Loading

The output stage of the mux-amp is very powerful, and can source 80 mA and sink 120 mA. Of course, this is too much current to sustain and the part will eventually be destroyed by excessive dissipation or by metal traces on the die opening. The metal traces are completely reliable while delivering the 30 mA continuous output given in the Absolute Maximum Ratings table in this data sheet, or higher purely transient currents.

Gain or gain accuracy degrades only 10% from no load to 100Ω load. Heavy resistive loading will degrade frequency response and video distortion only a bit, becoming noticeably worse for loads < 100Ω.

Applications Information — Contd.

Capacitive loads will cause peaking in the frequency response. If capacitive loads must be driven, a small-valued series resistor can be used to isolate it. 12Ω to 51Ω should suffice. A 22Ω series resistor will limit peaking to 2.5 dB with even a 220 pF load.

Input Connections

The input transistors can be driven from resistive and capacitive sources but are capable of oscillation when presented with an inductive input. It takes about 80 nH of series inductance to make the inputs actually oscillate, equivalent to four inches of unshielded wiring or about 6″ of unterminated input transmission line. The oscillation has a characteristic frequency of 500 MHz.

Often simply placing one's finger (via a metal probe) or an oscilloscope probe on the input will kill the oscillation. Normal high-frequency construction obviates any such problems, where the input source is reasonably close to the mux-amp input. If this is not possible, one can insert series resistors of around 51Ω to de-Q the inputs.

Feedback Connections

A feedback divider is used to increase circuit gain, and some precautions should be observed. The first is that parasitic capacitance at the −input will add phase lag to the feedback path and increase frequency response peaking or even cause oscillation. One solution is to choose feedback resistors whose parallel value is low. The pole frequency of the feedback network should be maintained above at least 200 MHz. For a 3 pF parasitic, this requires that the feedback divider have less than 265Ω impedance, equivalent to two 510Ω resistors when a gain of +2 is desired. Alternatively, a small capacitor across R_F can be used to create more of a frequency-compensated divider. The value of the capacitor should match the parasitic capacitance at the −input. It is also practical to place small capacitors across both the feedback resistors (whose values maintain the desired gain) to swamp out parasitics. For instance, two 10 pF capacitors across equal divider resistors will dominate parasitic effects and allow a higher divider resistance.

The other major concern about the divider concerns unselected-channel crosstalk. The differential input impedance of each input stage is around 200 KΩ. The unselected input's signal sources thus drive current through that input impedance into the feedback divider, inducing an unwanted output. The gain from unselected input to output, the crosstalk attenuation, if R_F/R_{IN}. In unity-gain connection the feedback resistor is 0Ω and very little crosstalk is induced. For a gain of +2, the crosstalk is about −60 dB.

Feedthrough Attenuation

The channels have different crosstalk levels with different inputs. Here is the typical attenuation for all combinations of inputs for the mux-amps at 3.58 MHz:

Feedthrough of EL4441 and EL4443 at 3.58 MHz

		In1	In2	In3	In4
Select Inputs, A1A0	00	Selected	−77 dB	−90 dB	−92 dB
	01	−80 dB	Selected	−77 dB	−90 dB
	10	−101 dB	−76 dB	Selected	−66 dB
	11	−96 dB	−84 dB	−66 dB	Selected

Feedthrough of EL4421 at 3.58 MHz

		In1	In2
Channel Select Input, A0	0	Selected	−88 dB
	1	−93 dB	Selected

Switching Glitches

The output of the mux-amps produces a small "glitch" voltage in response to a logic input change. A peak amplitude of only about 90 mV occurs, and the transient settles out in 20 ns. The glitch does not change amplitude with different gain settings.

With the four-input multiplexers, when two logic inputs are simultaneously changed, the glitch amplitude doubles. The increase can be a avoided by keeping transitions at least 6 ns apart. This can be accomplished by inserting one gate delay in one of the two logic inputs when they are truly synchronous.

EL4430C/EL4431C
Video Instrumentation Amplifiers

Features

- Fully differential inputs and feedback
  - — Differential input range of ±2V
  - — Common-mode range of ±12V
  - — High CMRR at 4 MHz of 70 dB
  - — Stable at gains of 1, 2
- Calibrated and clean input clipping
- 4430—80 MHz @ G = 1
- 4431—160 MHz GBWP
- 380V/μs slew rate
- 0.02% or ° differential gain or phase
- Operates on ±5 to ±15V supplies with no AC degradation

Applications

- Line receivers
- "Loop-through" interface
- Level translation
- Magnetic head pre-amplification
- Differential-to-single-ended conversion

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4430CN	−40°C to +85°C	8-pin P-DIP	MDP0031
EL4430CS	−40°C to +85°C	8-lead SO	MDP0027
EL4431CN	−40°C to +85°C	8-pin P-DIP	MDP0031
EL4431CS	−40°C to +85°C	8-lead SO	MDP0027

General Description

The EL4430 and 4431 are video instrumentation amplifiers which are ideal for line receivers, differential-to-single-ended converters, transducer interfacing, and any situation where a differential signal must be extracted from a background of common-mode noise or DC offset.

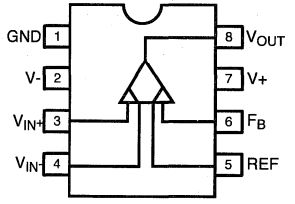
These devices have two differential signal inputs and two differential feedback terminals. The FB terminal connects to the amplifier output, or a divided version of it to increase circuit gain, and the REF terminal is connected to the output ground or offset reference.

The EL4430 is compensated to be stable at a gain of 1 or more, and the EL4431 for a gain of 2 or more.

The amplifiers have an operational temperature of −40°C to +85°C and are packaged in plastic 8-pin DIP and SO-8.

The EL4430 and EL4431 are fabricated with Elantec's proprietary complementary bipolar process which gives excellent signal symmetry and is free from latchup.

Connection Diagram



4430-1

EL4430C/EL4431C
Video Instrumentation Amplifiers

Absolute Maximum Ratings (T_A = 25°C)

V+	Positive Supply Voltage	16.5V	I_{OUT}	Continuous Output Current	30 mA
V_S	V+ to V− Supply Voltage	33V	P_D	Maximum Power Dissipation	See Curves
V_{IN}	Voltage at any Input or Feedback	V+ to V−	T_A	Operating Temperature Range	−40°C to +85°C
ΔV_{IN}	Difference between Pairs of Inputs or Feedback	6V	T_S	Storage Temperature Range	−60°C to +150°C
I_{IN}	Current into any Input, or Feedback Pin	4 mA			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open-Loop DC Electrical Characteristics Power supplies at ±5V, T_A = 25°. For the EL4431, $R_F = R_G = 500\Omega$.

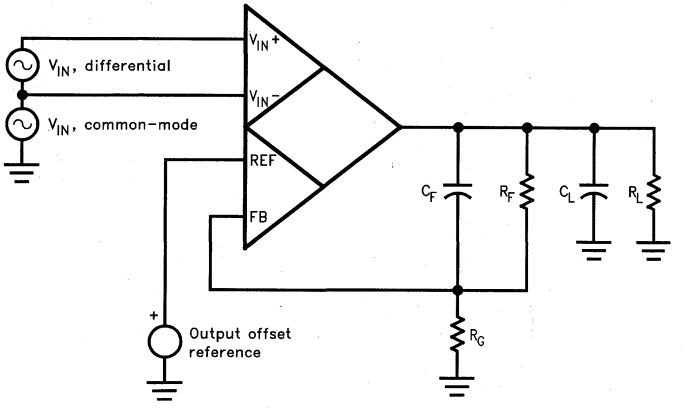
Parameter	Description		Min	Typ	Max	Test Level	Units
V_{DIFF}	Differential input voltage - Clipping (V_{CM} = 0)	EL4430/31	2.0	2.3		I	V
	0.1% nonlinearity	EL4430/31		1.8		V	V
V_{CM}	Common-mode range (V_{DIFF} = 0)	V_S = ±5V	±2	±3.0		I	V
		V_S = ±15V	+12	+13.0		I	V
V_{OS}	Input offset voltage	EL4430/31		2	8	I	mV
I_B	Input bias current (IN+, IN−, REF, and FB terminals)			12	20	I	µA
I_{OS}	Input offset current between IN+ and IN− and between REF and FB			0.2	2	I	µA
R_{IN}	Input resistance	EL4430/31	100	230		I	kΩ
CMRR	Common-mode rejection ratio		70	90		I	dB
PSRR	Power supply rejection ratio	EL4430/31		60		V	dB
E_G	Gain error, excluding feedback resistors	EL4430/31	−0.7	−0.2	+0.3	I	%
V_O	Output voltage swing	EL4430, V_S = ±5V	±2	±2.8		I	V
		V_S = ±15V	±12	±12.8		I	V
		EL4431, V_S = ±5V	±2.5	±3.0		I	V
		V_S = ±15V	±12.5	±13.0		I	V
I_{SC}	Output short-circuit current		40	90		I	mA
I_S	Supply current, V_S = ±15V			13.5	16	I	mA

Closed-Loop AC Electrical Characteristics

Power supplies at ±12V, T_A = 25°C, R_L = 500Ω for the EL4430, R_L = 150Ω for the EL4431, C_L = 15 pF. For the EL4431, R_F = R_G = 500Ω.

Parameter	Description		Min	Typ	Max	Test Level	Units
BW, −3 dB	−3 dB small-signal bandwidth	EL4430		82		V	MHz
		EL4431		80		V	MHz
BW, ±0.1 dB	0.1 dB flatness bandwidth	EL4430		20		V	MHz
		EL4431		14		V	MHz
Peaking	Frequency response peaking	EL4430		0.6		V	dB
		EL4431		1.0		V	dB
SR	Slew rate, V_{OUT} between −2V and +2V	All		380		V	V/μs
V_N	Input-referred noise voltage density	EL4430/31		26		V	nV/rt-Hz
dG	Differential gain error, Voffset between −0.7V and +0.7V	EL4430		0.02		V	%
		EL4431, R_L = 150Ω		0.04		V	%
dθ	Differential gain error, Voffset between −0.7V and +0.7V	EL4430		0.02		V	(°)
		EL4431, R_L = 150Ω		0.08		V	(°)
T_S	Settling time, to 0.1% from a 4V step	EL4430		48		V	ns

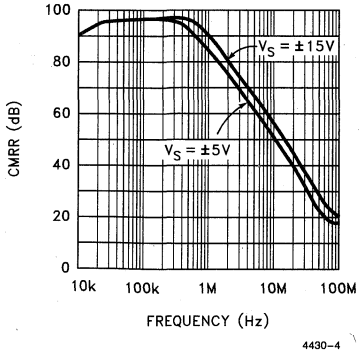
Test Circuit



4430-3

Typical Performance Curves

EL4430 and EL4431 Common-Mode Rejection Ratio vs Frequency

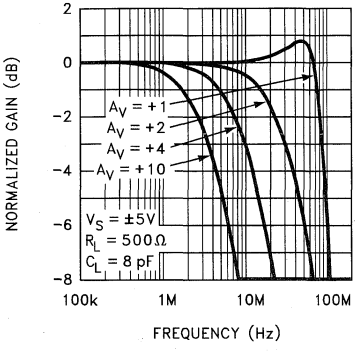


4430-4

EL4430C/EL4431C
Video Instrumentation Amplifiers

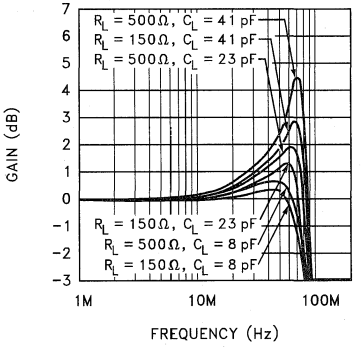
Typical Performance Curves — Contd.

EL4430 Frequency Response vs Gain



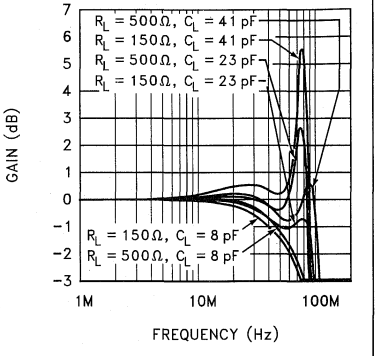
4430-5

EL4430 Frequency Response for Various R_L, C_L V_S = ±5V



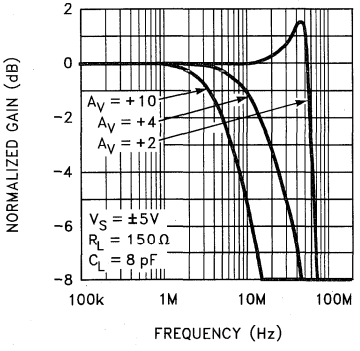
4430-6

EL4430 Frequency Response for Various R_L, C_L V_S = ±15V



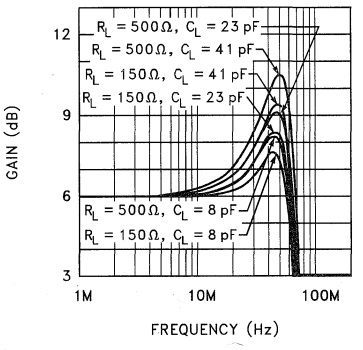
4430-7

EL4431 Frequency Response vs Gain



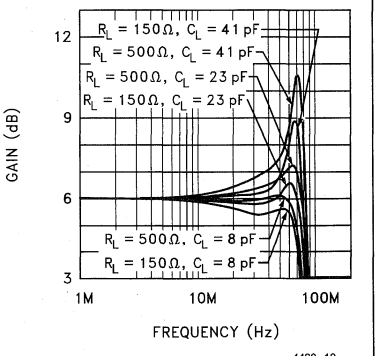
4430-8

EL4431 Frequency Response for Various R_L, C_L V_S = ±5V



4430-9

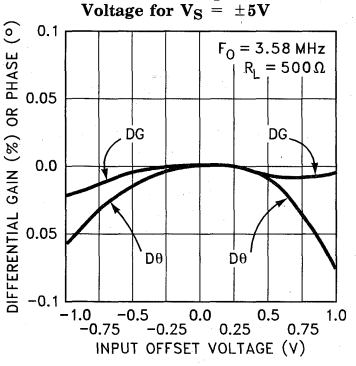
EL4431 Frequency Response for Various R_L, C_L V_S = ±15V



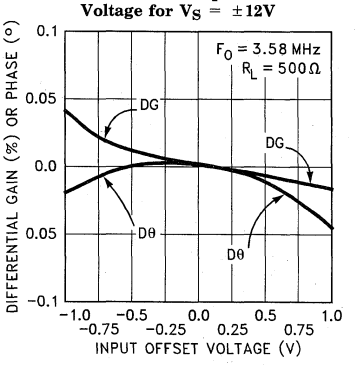
4430-10

Typical Performance Curves — Contd.

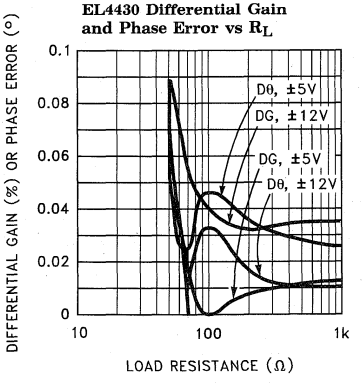
EL4430 Differential Gain and Phase vs Input Offset Voltage for V_S = ±5V



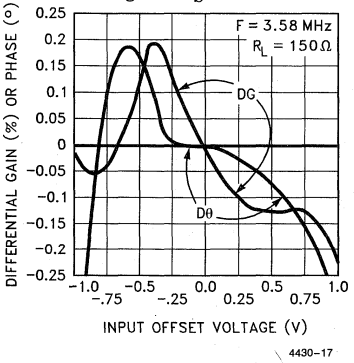
EL4430 Differential Gain and Phase vs Input Offset Voltage for V_S = ±12V



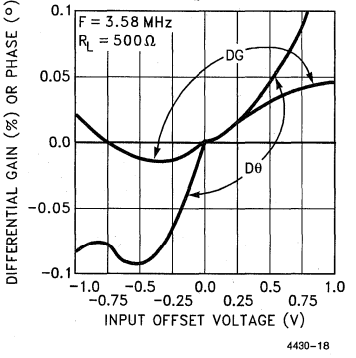
EL4430 Differential Gain and Phase Error vs R_L



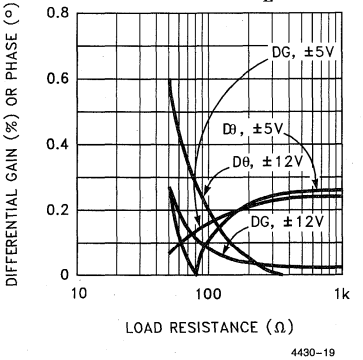
EL4431 Differential Gain and Phase vs Input Offset Voltage for V_S = ±5V



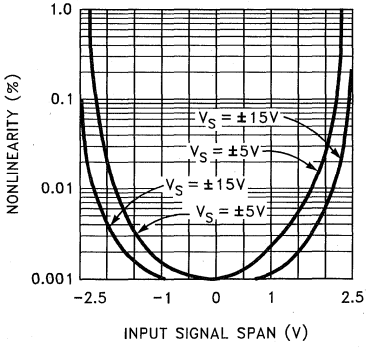
EL4431 Differential Gain and Phase vs Input Offset Voltage for V_S = ±12V



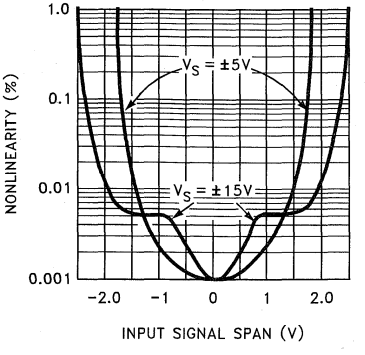
EL4431 Differential Gain and Phase Error vs R_L



EL4430 Nonlinearity vs Input Signal Span



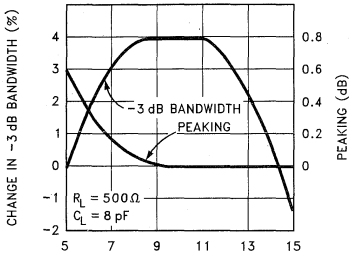
EL4431 Nonlinearity vs Input Signal Span



EL4430C/EL4431C
Video Instrumentation Amplifiers

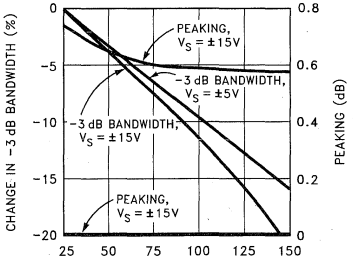
Typical Performance Curves — Contd.

EL4430 −3 dB Bandwidth and Peaking vs Supply Voltage for A_V = +1



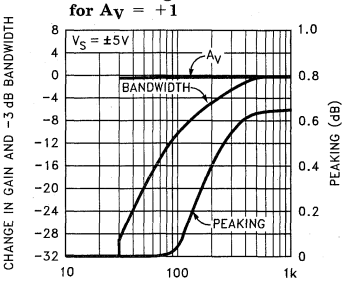
4430-23

EL4430 −3 dB Bandwidth and Peaking vs Die Temperature for A_V = +1



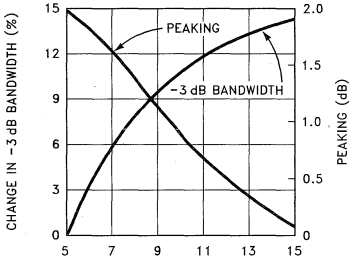
4430-24

EL4430 Gain, −3 dB Bandwidth and Peaking vs Load Resistance for A_V = +1



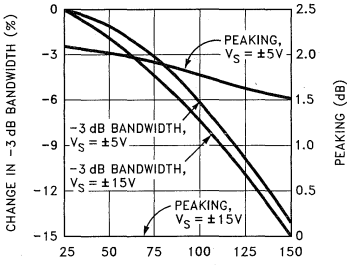
4430-25

EL4431 −3 dB Bandwidth and Peaking vs Supply Voltage



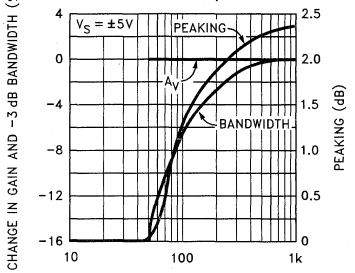
4430-26

EL4431 −3 dB Bandwidth and Peaking vs Die Temperature for A_V = +2



4430-27

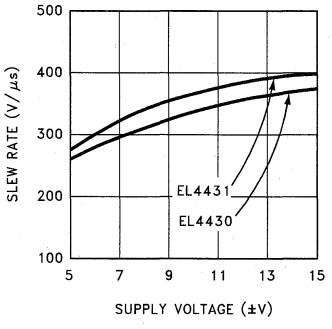
EL4431 Gain, −3 dB Bandwidth and Peaking vs Load Resistance for A_V = +2



4430-28

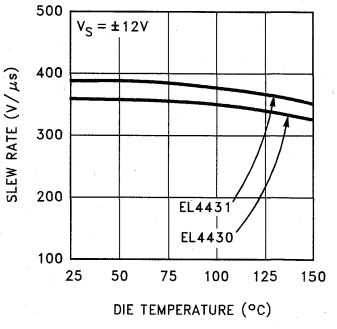
Typical Performance Curves — Contd.

Slew Rate vs Supply Voltage



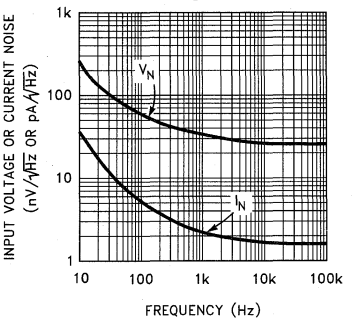
4430-32

Slew Rate vs Die Temperature



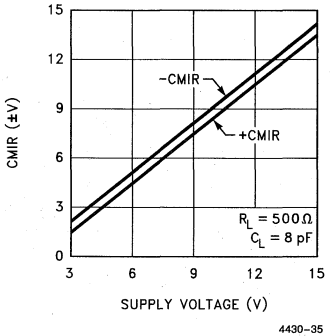
4430-33

Input Voltage and Current Noise vs Frequency



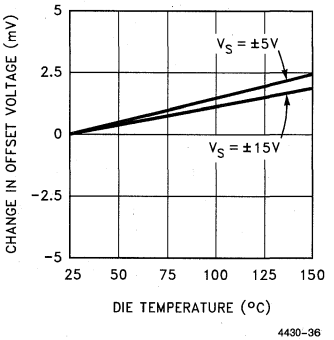
4430-34

Common Mode Input Range vs Supply Voltage



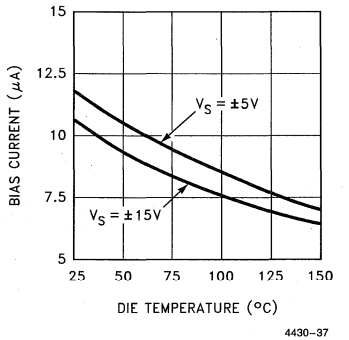
4430-35

Offset Voltage vs Die Temperature



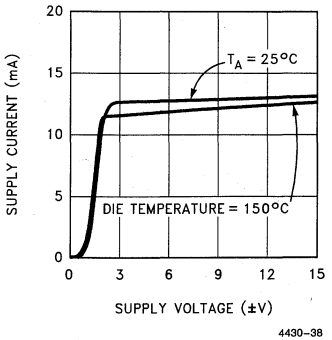
4430-36

Bias Current vs Die Temperature



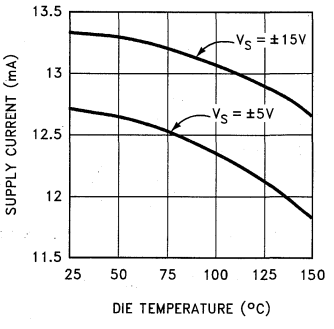
4430-37

Supply Current vs Supply Voltage



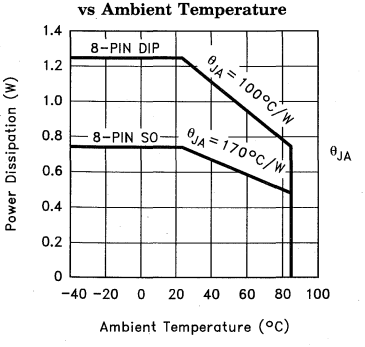
4430-38

Supply Current vs Die Temperature



4430-39

Power Dissipation vs Ambient Temperature

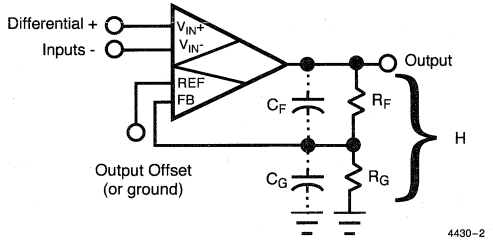


4430-40

EL4430C/EL4431C
Video Instrumentation Amplifiers

Applications Information

The EL4430 and EL4431 are designed to convert a fully differential input to a single-ended output. It has two sets of inputs; one which is connected to the signal and does not respond to its common-mode level, and another which is used to complete a feedback loop with the output. Here is a typical connection:



The gain of the feedback divider is H. The transfer function of the part is

$$V_{OUT} = A_O \times ((V_{IN}+) - (V_{IN}-) + (V_{REF} - V_{FB})).$$

V_{FB} is connected to V_{OUT} through a feedback network, so $V_{FB} = H \times V_{OUT}$. A_O is the open-loop gain of the amplifier, and is about 600 for the EL4430 and EL4431. The large value of A_O drives

$$(V_{IN}+) - (V_{IN}-) + (V_{REF} - V_{FB}) \rightarrow 0.$$

Rearranging and substituting for V_{FB}

$$V_{OUT} = ((V_{IN}+) - (V_{IN}-) + V_{REF})/H.$$

Thus, the output is equal to the difference of the V_{IN}'s and offset by V_{REF}, all gained up by the feedback divider ratio. The input impedance of the FB terminal (equal to R_{IN} of the input terminals) is in parallel with an R_G, and raises circuit gain slightly.

The EL4430 is stable for a gain of 1 (a direct connection between V_{OUT} and FB) or more and the EL4431 for gains of 2 or more. It is important to keep the feedback divider's impedance at the FB terminal low so that stray capacitance does not diminish the loop's phase margin. The pole caused by the parallel of resistors R_F and R_G and stray capacitance should be at least 200 MHz; typical strays of 3 pF thus require a feedback impedance of 270Ω or less. Two 510Ω resistors are acceptable for a gain of 2; 300Ω and 2700Ω make a good gain-of-10 divider. Alternatively, a small capacitor across R_F can be used to create more of a frequency-compensated divider. The value of the capacitor should scale with the parasitic capacitance at the FB terminal input. It is also practical to place small capacitors across both the feedback resistors (whose values maintain the desired gain) to swamp out parasitics. For instance, two 10 pF capacitors (for a gain of 2) across equal divider resistors will dominate parasitic effects and allow a higher divider resistance.

Input Connections

The input transistors can be driven from resistive and capacitive sources, but are capable of oscillation when presented with an inductive input. It takes about 80nH of series inductance to make the inputs actually oscillate, equivalent to 4″ of unshielded wiring or about 6″ of unterminated input transmission line. The oscillation has a characteristic frequency of 500 MHz. Often, placing one's finger (via a metal probe) or an oscilloscope probe on the input will kill the oscillation. Normal high-frequency construction obviates any such problems, where the input source is reasonably close to the input. If this is not possible, one can insert series resistors of approximately 51Ω to de-Q the inputs.

Signal Amplitudes

Signal input common-mode voltage must be between (V−)+3V and (V+)−3V to ensure linearity. Additionally, the differential voltage on any input stage must be limited to ±6V to prevent damage. The differential signal range is ±2V in the EL4430 and EL4431. The input range is substantially constant with temperature.

The Ground Pin

The ground pin draws only 6μA maximum DC current, and may be biased anywhere between (V−)+2.5V and (V+)−3.5V. The ground pin is connected to the IC's substrate and frequency compensation components. It serves as a shield within the IC and enhances CMRR over frequency, and if connected to a potential other than ground, it must be bypassed.

Applications Information

Power Supplies

The instrumentation amplifiers work well on any supplies from ±3V to ±15. The supplies may be of different voltages as long as the requirements of the Gnd pin are observed (see the Ground Pin section for a discussion). The supplies should be bypassed close to the device with short leads. 4.7μF tantalum capacitors are very good, and no smaller bypasses need be placed in parallel. Capacitors as low as 0.01μF can be used if small load currents flow.

Single-polarity supplies, such as +12V with +5V can be used, where the ground pin is connected to +5V and V- to ground. The inputs and outputs will have to have their levels shifted above ground to accommodate the lack of negative supply.

The dissipation of the amplifiers increases with power supply voltage, and this must be compatible with the package chosen. This is a close estimate for the dissipation of a circuit:

$$P_D = 2 \times V_S \times I_S, \max + (V_S - V_O) \times V_O/R_{PAR}$$

where I_S, max is the maximum supply current

V_S is the ± supply voltage (assumed equal)

V_O is the output voltage

R_{PAR} is the parallel of all resistors loading the output

For instance, the EL4431 draws a maximum of 16 mA and we might require a 2V peak output into 150Ω and a 270Ω + 270Ω feedback divider. The R_{PAR} is 117Ω. The dissipation with ±5V supplies is 201 mW. The maximum supply voltage that the device can run on for a given P_D and the other parameter is

$$V_S, \max = (P_D + V_O 2/R_{PAR})/(2I_S + V_O/R_{PAR})$$

The maximum dissipation a package can offer is

$$P_D, \max = (T_J, \max - T_A \max)/\theta_{JA}$$

where T_J, max is the maximum die junction temperature, 150°C for reliability, less to retain optimum electrical performance.

T_A, max is the ambient temperature, 70°C for commercial and 85°C for industrial range.

θ_{JA} is the thermal resistance of the mounted package, obtained from datasheet dissipation curves.

The more difficult case is the SO-8 package. With a maximum die temperature of 150°C and a maximum ambient temperature of 85°C, the 65°C temperature rise and package thermal resistance of 170°C/W gives a dissipation of 382 mW at 85°C. This allows a maximum supply voltage of ±8.5V for the EL4431 operated in our example. If an EL4430 were driving a light load ($R_{PAR} \rightarrow \infty$), it could operate on ±15V supplies at a 70°C maximum ambient.

Output Loading

The output stage of the instrumentation amplifiers is very powerful. It typically can source 80 mA and sink 120 mA. Of course, this is too much current to sustain and the part will eventually be destroyed by excessive dissipation or by metal traces on the die opening. The metal traces are completely reliable while delivering the 30 mA continuous output given in the Absolute Maximum Ratings table in this datasheet, or higher purely transient currents.

Gain or gain accuracy degrades only 10% from no load to 100Ω load. Heavy resistive loading will degrade frequency response and video distortion for loads <100Ω

Capacitive loads will cause peaking in the frequency response. If capacitive loads must be driven, a small-valued series resistor can be used to isolate it (12Ω to 51Ω should suffice). A 22Ω series resistor will limit peaking to 2.5 dB with even a 220 pF load.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4450C

Wideband Four-Quadrant Multiplier

Features

- Complete four-quandrant multiplier with output amp—requires no extra components
- Good linearity of 0.3%
- 90 MHz bandwidth for both X and Y inputs
- Operates on ±5V to ±15V supplies
- All inputs are differential
- 400V/μs slew rate

Applications

- Modulation/Demodulation
- RMS computation
- Real-time power computation
- Nonlinearity correction/ generation

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4450CN	−40°C to +85°C	14-Pin P-DIP	MDP0031
EL4450CM	−40°C to +85°C	14-Lead SO	MDP0027

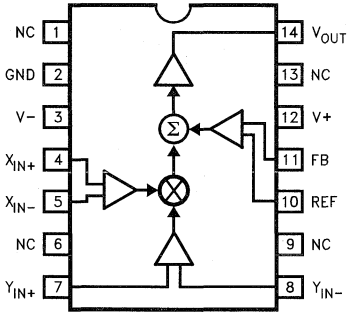
General Description

The EL4450C is a complete four-quadrant multiplier circuit. It offers wide bandwidth and good linearity while including a powerful output voltage amplifier, drawing modest supply current.

The EL4450C operates on ±5V supplies and has an analog input range of ±2V, making it ideal for video signal processing. AC characteristics do not vary over the ±5V to ±15V supply range.

The multiplier has an operational temperature range of −40°C to +85°C and are packaged in plastic 14-pin P-DIP and SO.

Connection Diagram



4450-1

EL4450C
Wideband Four-Quadrant Multiplier

Absolute Maximum Ratings (T_A = 25°C)

V+	Positive Supply Voltage	16.5V	I_{OUT}	Output Current	30 mA
V_S	V+ to V− Supply Voltage	33V	P_D	Maximum Power Dissipation	See Curves
V_{IN}	Voltage at any Input or Feedback	V+ to V−	T_A	Operating Temperature Range	−40°C to +85°C
ΔV_{IN}	Difference between Pairs of Inputs or Feedback	6V	T_S	Storage Temperature Range	−60°C to +150°C
I_{IN}	Current into any Input or Feedback Pin	4 mA			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open-Loop DC Electrical Characteristics Power Supplies at ±5V, T_A = 25°C, $V_{FB} = V_{OUT}$.

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{DIFF}	Differential Input Voltage—Clipping 0.2% nonlinearity	1.8	2.0 1.0		I V	V V
V_{CM}	Common-Mode Range of V_{DIFF} = 0, V_S = ±5V V_S = ±15V	±2.5 ±12.5	±2.8 ±12.8		I I	V V
V_{OS}	Input Offset Voltage		8	35	I	mV
I_B	Input Bias Current		9	20	I	µA
I_{OS}	Onput Offset Current between X_{IN}+ and X_{IN}−, Y_{IN}+ and Y_{IN}−, REF and FB		0.5	4	I	µA
Gain	Gain Factor of V_{OUT} = Gain × X_{IN}+ × Y_{IN}	0.45	0.5	0.55	I	V/V^2
NLx	Nonlinearity of X Input; X_{IN} between −1V and +1V		0.3	0.7	I	%
NLy	Nonlinearity of Y Input; Y_{IN} between −1V and +1V		0.2	0.35	I	%
R_{IN}	Input resistance, X_{IN}+ to X_{IN}−, Y_{IN}+ to Y_{IN}−, REF to FB		230 90		V	kΩ
CMRR	Common-Mode Rejection Ratio, X_{IN} and Y_{IN}	70	90		I	dB
PSRR	Power-Supply Rejection Ratio, FB	60	72		I	dB
V_O	Output Voltage Swing (V_{IN} = 0, V_{REF} Varied) V_S = ±5V V_S = ±15V	±2.5 ±12.5	±2.8 ±12.8		I	V
I_{SC}	Output Short-Circuit Current	40	85		I	mA
I_S	Supply Current, V_S = ±15V		15.4	18	I	mA

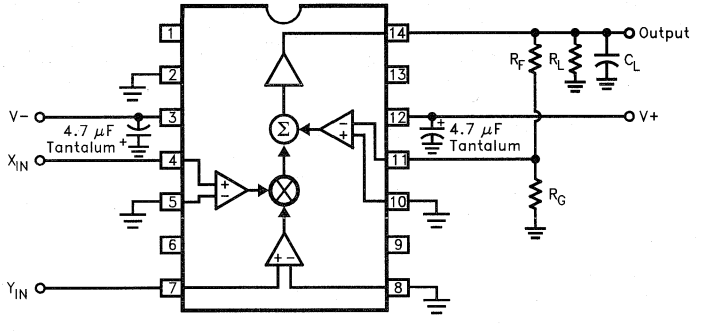
EL4450C
Wideband Four-Quadrant Multiplier

Closed-Loop AC Electrical Characteristics

Power Supplies at ±12V, T_A = 25°C, R_L = 500Ω, C_L = 15pF

Parameter	Description	Min	Typ	Max	Test Level	Units
BW, −3 dB	−3 dB Small-Signal Bandwidth, X or Y		90		V	MHz
BW, ±0.1 dB	0.1 dB Flatness Bandwidth		10		V	MHz
Peaking	Frequency Response Peaking		1.0		V	dB
SR	Slew Rate, V_{OUT} between −2V and +2V	300	400		I	V/µs
V_N	Input-Referred Noise Voltage Density		100		V	nV/√Hz

Test Circuit

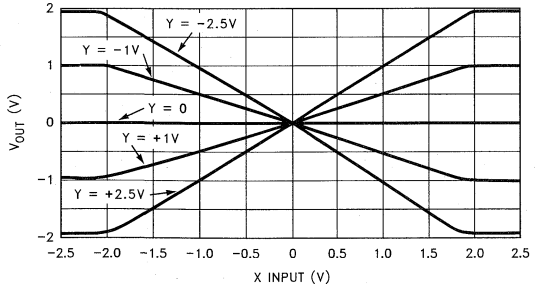


4450-2

Note: For typical performance curves, R_F = 0, R_G = ∞, V_S = ±5V, R_L = 500Ω, and C_L = 15 pF unless otherwise noted.

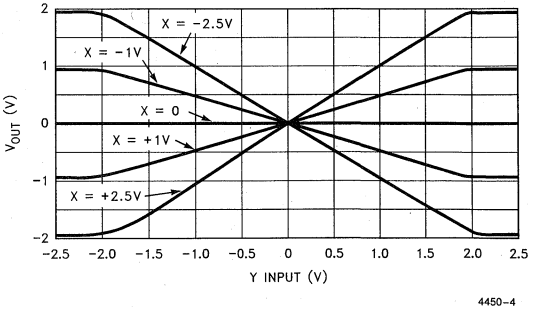
Typical Performance Curves

Transfer Function of X Input for Various Y Inputs



4450-3

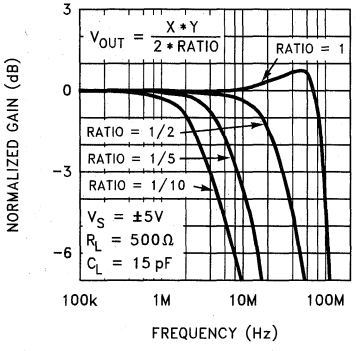
Transfer Function of Y Input for Various X Inputs



4450-4

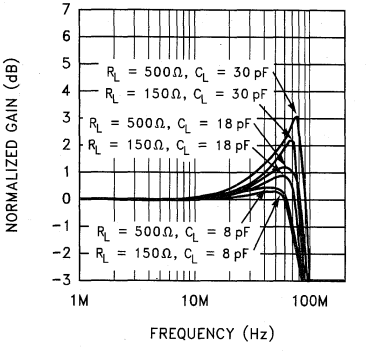
Typical Performance Curves — Contd.

Frequency Response for Various Feedback Divider Ratios



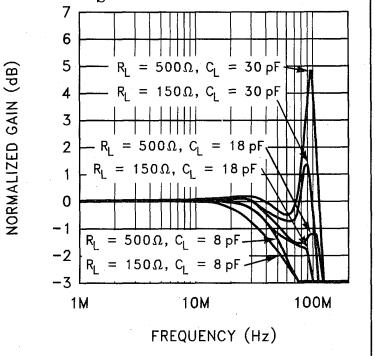
4450-5

Frequency Response for Various R_L, C_L V_S = ±5V



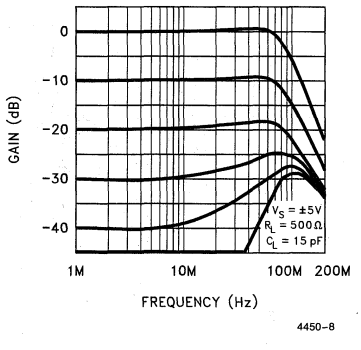
4450-6

Frequency Response for Various R_L, C_L V_S = ±15V



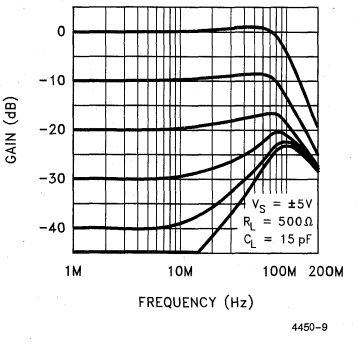
4450-7

X Input Frequency Response for Various Y DC Inputs



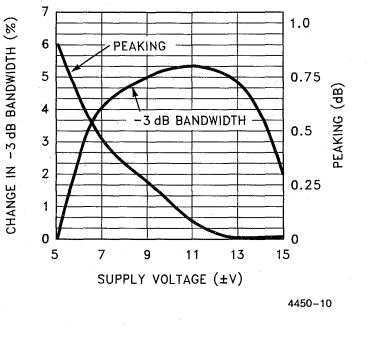
4450-8

Y Input Frequency Response for Various X DC Inputs



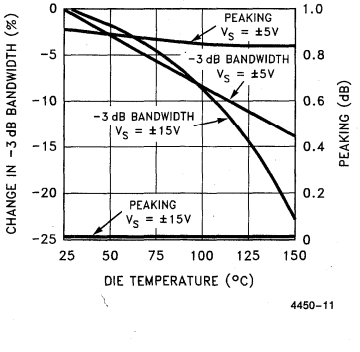
4450-9

−3 dB Bandwidth and Peaking vs Supply Voltage



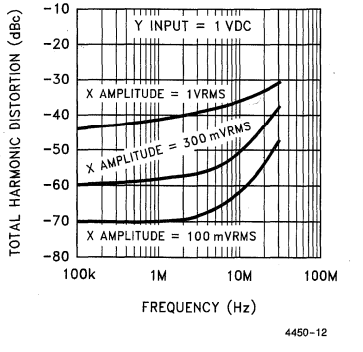
4450-10

Change in Bandwidth and Peaking vs Temperature



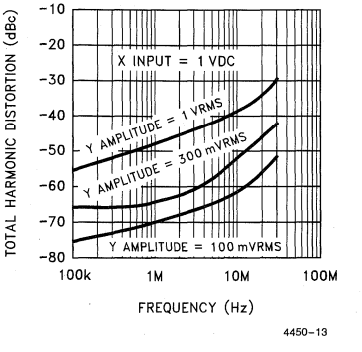
4450-11

Total Harmonic Distortion of X Input vs Frequency



4450-12

Total Harmonic Distortion of Y Input vs Frequency

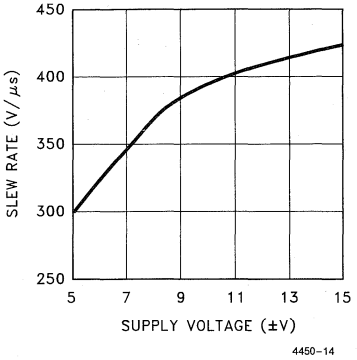


4450-13

EL4450C
Wideband Four-Quadrant Multiplier

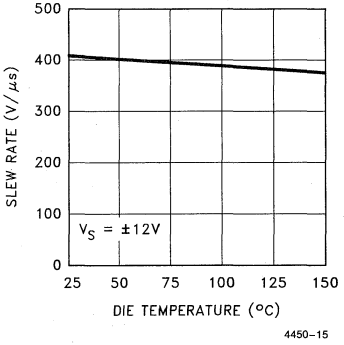
Typical Performance Curves — Contd.

Slew Rate vs Supply Voltage



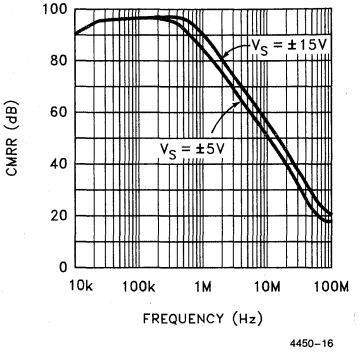
4450-14

Slew Rate vs Die Temperature



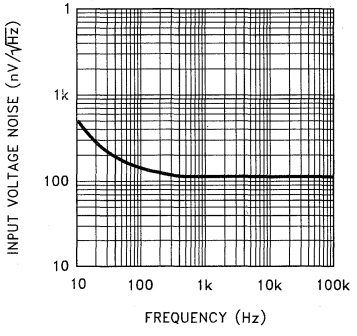
4450-15

CMRR vs Frequency



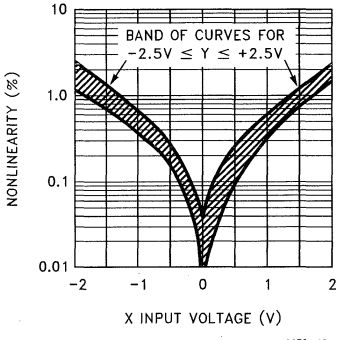
4450-16

Input Voltage Noise vs Frequency



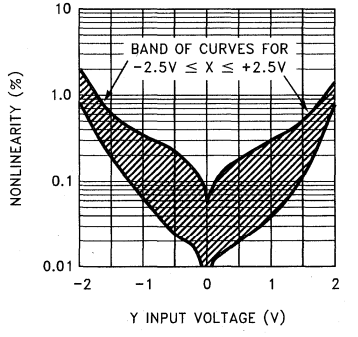
4450-17

Nonlinearity of X Input



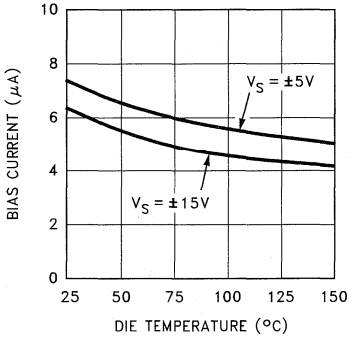
4450-18

Nonlinearity of Y Input



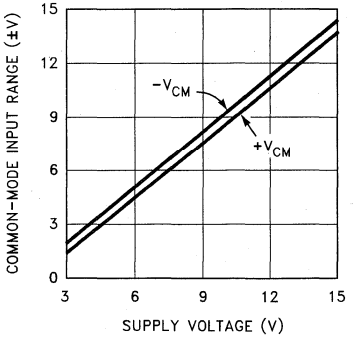
4450-19

Bias Current vs Die Temperature



4450-20

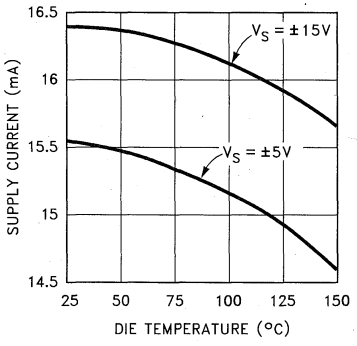
Common-Mode Input Range vs Supply Voltage



4450-21

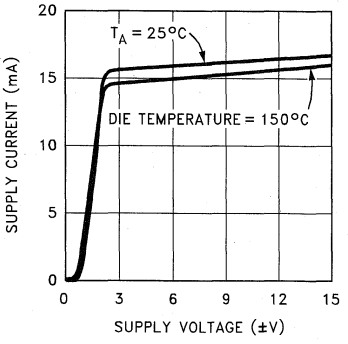
Typical Performance Curves — Contd.

Supply Current vs Die Temperature



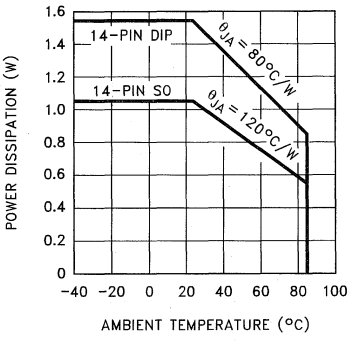
4450-22

Supply Current vs Supply Voltage



4450-23

14-Pin Package Power Dissipation vs Ambient Temperature



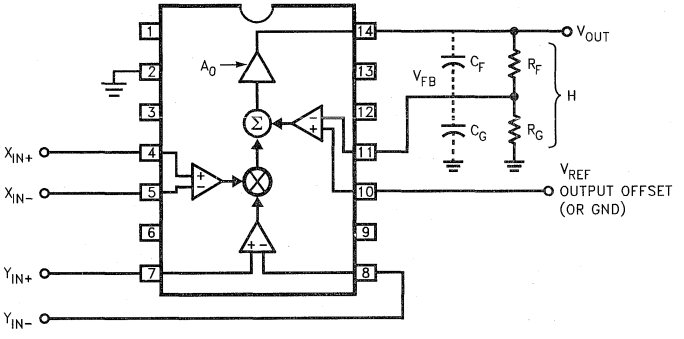
4450-24

3

EL4450C
Wideband Four-Quadrant Multiplier

Applications Information

The EL4450 is a complete four-quadrant multiplier with 90 MHz bandwidth. It has three sets of inputs; a differential multiplying X-input, a differential multiplying Y-input, and another differential input which is used to complete a feedback loop with the output. Here is a typical connection:



4450-25

The gain of the feedback divider is H, and $H = R_G/(R_G + R_F)$. The transfer function of the part is

$$V_{OUT} = A_O \times (½ \times ((V_{INX+} - V_{INX-})) \times ((V_{INY+} - V_{INY-})) + (V_{REF} - V_{FB})).$$

V_{FB} is connected to V_{OUT} through a feedback network, so $V_{REF} = H^*V_{OUT}$. A_O is the open-loop gain of the amplifier, and is about 600. The large value of A_O drives

$$(½ \times ((V_{INX+} - V_{INX-})) \times ((V_{INY+} - V_{INY-})) + (V_{REF} - V_{FB})) \rightarrow 0.$$

Rearranging and substituting for V_{REF}

$$V_{OUT} = (½ \times ((V_{INX+} - V_{INX-})) \times ((V_{INY+} - V_{INY-})) + V_{REF})/H, \text{ or}$$

$$V_{OUT} = (XY/2 + V_{REF})/H$$

Thus the output is equal to one-half the product of X and Y inputs and offset by V_{REF}, all gained up by the feedback divider ratio. The EL4450 is stable for a direct connection between V_{OUT} and FB, and the feedback divider may be used for higher output gain, although with the traditional loss of bandwidth.

It is important to keep the feedback divider's impedance at the FB terminal low so that stray capacitance does not diminish the loop's phase margin. The pole caused by the parallel impedance of the feedback resistors and stray capacitance should be at least 150 MHz; typical strays of 3 pF thus require a feedback impedance of 360Ω or less, Alternatively, a small capacitor across R_F can be used to create more of a frequency-compensated divider. The value of the capacitor should scale with the parasitic capacitance at the FB input. It is also practical to place small capacitors across both the feedback resistors (whose values maintain the desired gain) to swamp out parasitics. For instance, two 10 pF capacitors across equal divider resistors for a maximum gain of 1 will dominate parasitic effects and allow a higher divider resistance.

The REF pin can be used as the output's ground reference, or for DC offsetting of the output, or it can be used to sum in another signal.

Input Connections

The input transistors can be driven from resistive and capacitive sources, but are capable of oscillation when presented with an inductive input. It takes about 80 nH of series inductance to make the inputs actually oscillate, equivalent to four inches of unshielded wiring or about 6″ of unterminated input transmission line. The oscillation has a characteristic frequency of 500 MHz. Placing one's finger (via a metal probe) or an oscilloscope probe on the input will kill the oscillation. Normal high-frequency construction obviates any such problems, where the input source is reasonably close to the input. If this is not possible, one can insert series resistors of around to 51Ω to de-Q the inputs.

Signal Amplitudes

Signal input common-mode voltage must be between (V−) + 2.5V and (V+) −2.5V to ensure linearity. Additionally, the differential voltage on any input stage must be limited to ± 6V to prevent damage. The differential signal range is ± 2V in the EL4450C. The input range is substantially constant with temperature.

The Ground Pin

The ground pin draws only 6 μA maximum DC current, and may be biased anywhere between (V−) +2.5V and (V+) −3.5V. The ground pin is connected to the IC's substrate and frequency compensation components. It serves as a shield within the IC and enhances input stage CMRR over frequency, and if connected to a potential other than ground, it must be bypassed.

Power Supplies

The EL4450C works well on supplies from ± 3V to ± 15V. The supplies may be of different voltages as long as the requirements of the GND pin are observed (see the Ground Pin section for a discussion). The supplies should be bypassed close to the device with short leads. 4.7 μF tantalum capacitors are very good, and no smaller bypasses need be placed in parallel. Capacitors as low as 0.01 μF can be used if small load currents flow.

Single-polarity supplies, such as +12V with +5V can be used, where the ground pin is connected to +5V and V− to ground. The inputs and outputs will have to have their levels shifted above ground to accommodate the lack of negative supply.

The power dissipation of the EL4450C increases with power supply voltage, and this must be compatible with the package chosen. This is a close estimate for the dissipation of a circuit:

$$P_D = 2*I_{S,max}*V_S + (V_S - V_O)*V_O/R_{PAR}$$

where

$I_{S,max}$ is the maximum supply current
V_S is the ± supply voltage (assumed equal)
V_O is the output voltage
R_{PAR} is the parallel of all resistors loading the output

For instance, the EL4450C draws a maximum of 18 mA. With light loading, $R_{PAR} \rightarrow \infty$ and the dissipation with ±5V supplies is 180 mW. The maximum supply voltage that the device can run on for a given P_D and the other parameters is

$$V_{S,max} = (P_D + V_O^2/R_{PAR})/(2I_S + V_O/R_{PAR})$$

The maximum dissipation a package can offer is

$$P_{D,max} = (T_{J,max} - T_{A,max})/\theta_{JA}$$

Where $T_{J,max}$ is the maximum junction temperature, 150°C for reliability, less to retain optimum electrical performance

$T_{A,max}$ is the ambient temperature, 70°C for commercial and 85°C for industrial range

θ_{JA} is the thermal resistance of the mounted package, obtained from data sheet dissipation curves

The more difficult case is the SO-14 package. With a maximum junction temperature of 150°C and a maximum ambient temperature of 85°C, the 65°C temperature rise and package thermal resistance of 120°/W gives a dissipation of 542 mW at 85°C. This allows the full maximum operating supply voltage unloaded, but reduced if loaded significantly.

Output Loading

The output stage is very powerful. It typically can source 85 mA and sink 120 mA. Of course, this is too much current to sustain and the part will eventually be destroyed by excessive dissipation or by metal traces on the die opening. The metal traces are completely reliable while delivering the 30 mA continuous output given in the Absolute Maximum Ratings table in this data sheet, or higher purely transient currents.

Gain accuracy degrades only 0.2% from no load- to 100Ω load. Heavy resistive loading will degrade frequency response and video distortion for loads < 100Ω.

Capacitive loads will cause peaking in the frequency response. If a capacitive load must be driven, a small-valued series resistor can be used to isolate it. 12Ω to 51Ω should suffice. A 22Ω series resistor will limit peaking to 2.5 dB with even a 220 pF load.

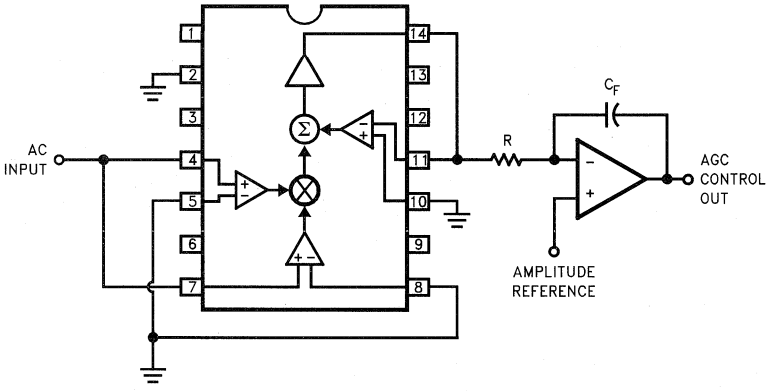
EL4450C
Wideband Four-Quadrant Multiplier

Mixer Applications

Because of its lower distortion levels, the Y input is the better choice for a mixer's signal port. The X input would receive oscillator amplitudes of about 1V RMS maximum. Carrier suppression is initially limited by the offset voltage of the Y input, 20 mV maximum, and is about 37 dB worst-case. Better suppression can be obtained by nulling the offset of the X input. Similarly, nulling the offset of the Y input will improve signal-port suppression. Driving an input differentially will also maximize feedthrough suppression at frequencies beyond 10 MHz.

AC Level Detectors

Square-law converters are commonly used to convert AC signals to DC voltages corresponding to the original amplitude in subsystems like automatic gain controls (AGC's) and amplitude-stabilized oscillators. Due to the controlled AC amplitudes, the inputs of the multiplier will see a relatively constant signal level. Best performance will be obtained for inputs between 200 mVRMS and 1 VRMS. The traditional use of the EL4450C as an AGC detector and control loop would be:



Traditional AGC Detector/DC Feedback Circuit

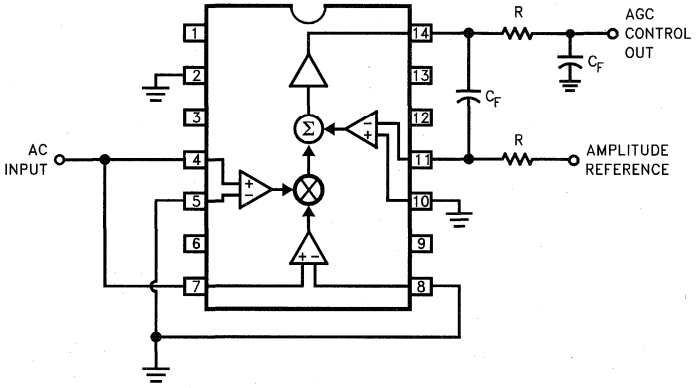
AC Level Detectors — Contd.

The EL4450C simply provides an output equal to the square of the input signal and an integrator filters out the AC component, while comparing the DC component to an amplitude reference. The integrator output is the DC control voltage to the variable-gain sections of the AGC (not shown). If a negative polarity of reference is required, one of the multiplier input terminal pairs is reversed, inverting the multiplier output. Input bias current will cause input voltage offsets due to source impedances; putting a compensating resistor in series with the grounded inputs of the EL4450C will reduce this offset greatly.

This control system will attempt to force

$V_{IN,RMS}^2/4 = V_{REF}$.

The extra op-amp can be eliminated by using this circuit:



4450-27

Simplified AGC Detector/DC Feedback Circuit

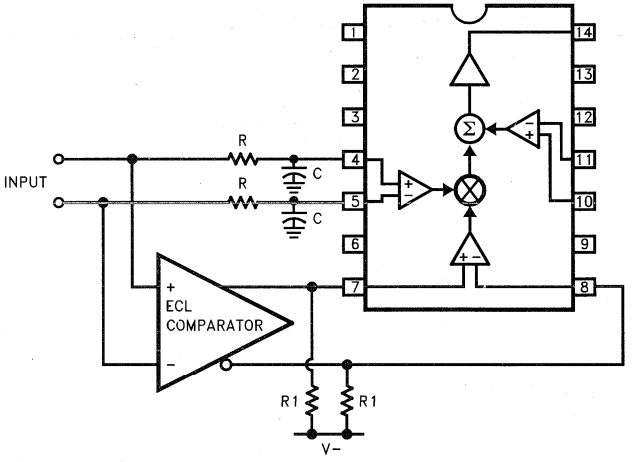
EL4450C
Wideband Four-Quadrant Multiplier

AC Level Detectors — Contd.

Here the internal op-amp of the EL4450C replaces the external amplifier. The feedback capacitor C_F does not provide a perfect integration action; a zero occurs at a frequency of $1/2\pi RC_F$. This is canceled by including another RC_F pair at the AGC control output. If the reference voltage must be negative, the resistor at pin 11 is connected to ground rather than the reference and pin 10 connected to the reference.

The amplitude reference will have to support some AC currents flowing through R. If this is a problem, several changes can be made to eliminate it. The reference is connected to pin 10 and the resistor R connected to pin 11 reconnected to ground, and one of the multiplier input connections are reversed.

Square-law detectors have a restricted input range, about 10:1, because the output rapidly disappears into the DC errors as signal amplitudes reduce. This circuit gives a multiplier output that is the absolute value of the input, thus increasing range to 100:1:



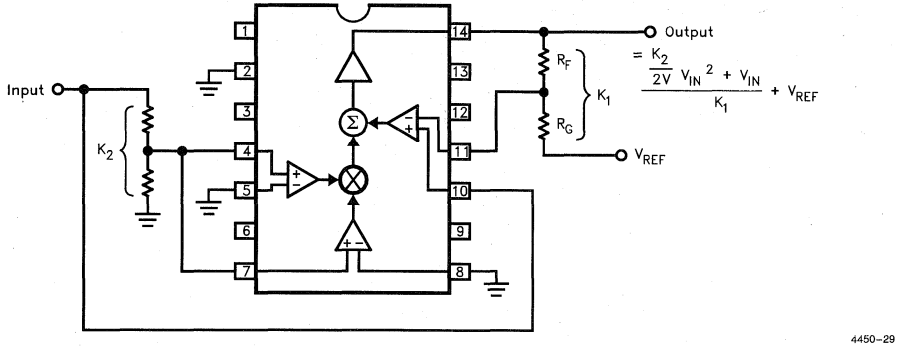
Absolute-Value Input Circuitry

AC Level Detectors — Contd.

An ECL comparator produces an output corresponding to the sign of the input, which when multiplied by the input produces an effective absolute-value function. The RC product connected to the X inputs simply emulates the time delay of the comparator to maintain circuit accuracy at higher frequencies.

Nonlinear Function Generation

The REF pin of the EL4450C can be used to sum in various quantities of polynominal function generators. For instance, this sum of REF allows a linear signal path which can have various amounts of squared signal added:

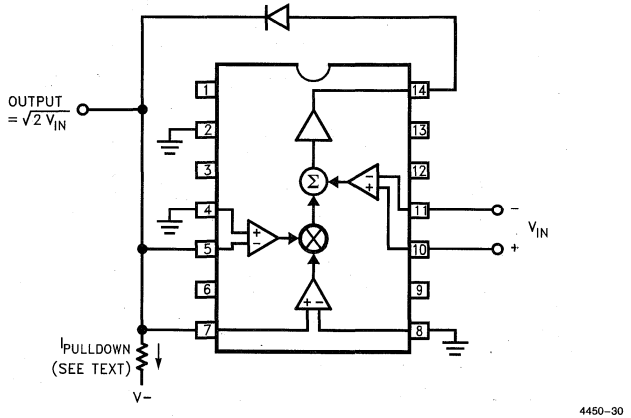


Polynomial Function Generator

The polarity of the squared signal can be reversed by swapping one of the X or Y input pairs.

The REF and FB pins also simplify feedback schemes that allow square-rooting:

The diode and $I_{pulldown}$ assure that the output will always produce the positive square-root of the input signal. $I_{pulldown}$ should be large enough to assure that the diode be forward-biased for any load current. In this configuration, the bandwidth of the circuit will reduce for smaller input signals.



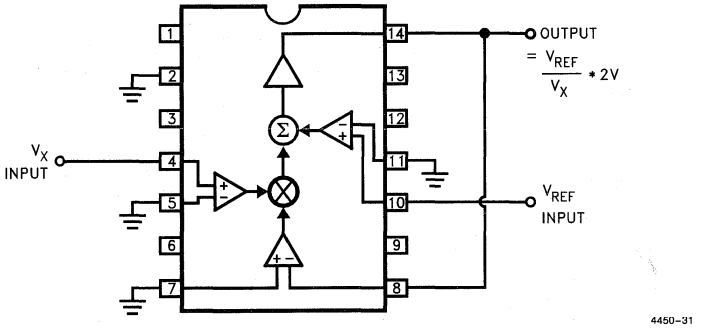
Square-Rooter

EL4450C
Wideband Four-Quadrant Multiplier

Nonlinear Function Generation — Contd.

The REF and FB terminals can also be used to implement division:

The output frequency response reduces for smaller values of V_X, but is not affected by V_{REF}.



Divider Connection

EL4451C

Wideband Variable-Gain Amplifier, Gain of 2

Features

- Complete variable-gain amplifier with output amplifier, requires no extra components
- Excellent linearity of 0.2%
- 70 MHz signal bandwidth
- Operates on ±5V to ±15V supplies
- All inputs are differential
- 400V/μs slew rate
- >70dB attenuation @ 4 MHz

Applications

- Leveling of varying inputs
- Variable filters
- Fading
- Text insertion into video

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4451CN	−40°C to +85°C	14-Pin P-DIP	MDP0031
EL4451CS	−40°C to +85°C	14-Lead SO	MDP0027

General Description

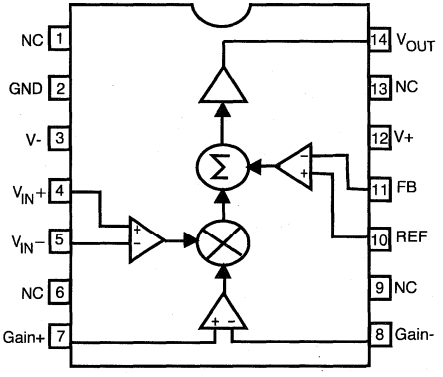
The EL4451C is a complete variable gain circuit. It offers wide bandwidth and excellent linearity while including a powerful output voltage amplifier, drawing modest supply current.

The EL4451C operates on ±5V to ±15V supplies and has an analog input range of ±2V, making it ideal for video signal processing. AC characteristics do not change appreciably over the ±5V to ±15V supply range.

The circuit has an operational temperature range of −40°C to +85°C and is packaged in plastic 14-pin DIP and 14-lead SO.

The EL4451C is fabricated with Elantec's proprietary complementary bipolar process which provides excellent signal symmetry and is free from latch up.

Connection Diagram



4451-1

EL4451C
Wideband Variable-Gain Amplifier, Gain of 2

Absolute Maximum Ratings (T_A = 25°C)

V+	Positive Supply Voltage	16.5V	I_{OUT}	Continuous Output Current	30mA
V_S	V+ to V− Supply Voltage	33V	P_D	Maximum Power Dissipation	See Curves
V_{IN}	Voltage at any Input or Feedback	V+ to V−	T_A	Operating Temperature Range	−40°C to +85°C
ΔV_{IN}	Difference between Pairs of Inputs or Feedback	6V	T_S	Storage Temperature Range	−60°C to +150°C
I_{IN}	Current into any Input, or Feedback Pin	4mA			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open-Loop DC Electrical Characteristics Power Supplies at ±5V, T_A = 25°C, R_L = 500Ω.

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{DIFF}	Signal input differential input voltage - Clipping 0.2% nonlinearity	1.8	2.0 1.3		I V	V V
V_{CM}	Common-mode range of V_{IN}; V_{DIFF} = 0, V_s = ±5V V_s = ±15V	±2.0	±2.8 ±12.8		I V	V V
V_{OS}	Input offset voltage		7	25	I	mV
V_{OS}, FB	Output offset voltage		8	25	I	mV
$V_{G,\,100\%}$	Extrapolated voltage for 100% gain	1.9	2.1	2.2	I	V
$V_{G,\,0\%}$	Extrapolated voltage for 0% gain	−0.16	−0.06	0.06	I	V
$V_{G,\,1V}$	Gain at V_{GAIN} = 1V	0.95	1.05	1.15	I	V/V
I_B	Input bias current (all inputs)	−20	−9	0	I	µA
I_{OS}	Input offset current between V_{IN} + and V_{IN} −, Gain+ and Gain−, FB and Ref		0.2	4	I	µA
NL	Nonlinearity, V_{IN} between −1V and +1V, V_G = 1V		0.2	0.5	I	%
Ft	Signal feedthrough, V_G = −1V		−100	−70	I	dB
R_{IN}, V_{IN}	Input resistance, V_{IN}	100	230		I	KΩ
R_{IN}, FB	Input resistance, FB	200	460		V	KΩ
R_{IN}, R_{GAIN}	Input resistance, gain input	50	100		I	KΩ

Open-Loop DC Electrical Characteristics — Contd.

Power Supplies at ±5V, T_A = 25°C, R_L = 500Ω.

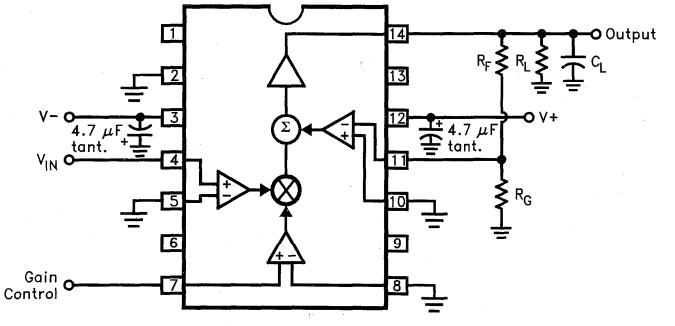
Parameter	Description	Min	Typ	Max	Test Level	Units
CMRR	Common-mode rejection ratio of V_{IN}	70	90		I	dB
PSRR	Power supply rejection ratio of $V_{OS, FB}$, V_S = ±5V to ±15V	50	60		I	dB
V_O	Output voltage swing V_S = ±5V (V_{IN} = 0, V_{REF} varied) V_S = ±15V	±2.5 ±12.5	±2.8 ±12.8		I	V
I_{SC}	Output short-circuit current	40	85		I	mA
I_S	Supply current, V_S = ±15V		15.5	18	I	mA

Closed-Loop AC Electrical Characteristics

Power supplies at ±12V, T_A = 25°C. R_L = 500Ω, C_L = 15pF, V_G = 1V

Parameter	Description	Min	Typ	Max	Test Level	Units
BW, −3dB	−3dB small-signal bandwidth, signal input		70		V	MHz
BW, ±0.1dB	0.1dB flatness bandwidth, signal input		10		V	MHz
Peaking	Frequency response peaking		0.6		V	dB
BW, gain	−3dB small-signal bandwidth, gain input		70		V	MHz
SR	Slew rate, V_{OUT} between −2V and +2V, R_F = R_G = 500Ω		400		V	V/µs
V_N	Input referred noise voltage density		110		V	nV/√Hz
dG	Differential gain error, Voffset between −0.7V and +0.7V		0.9		V	%
dθ	Differential phase error, Voffset between −0.7V and +0.7V		0. 2		V	°

Test Circuit



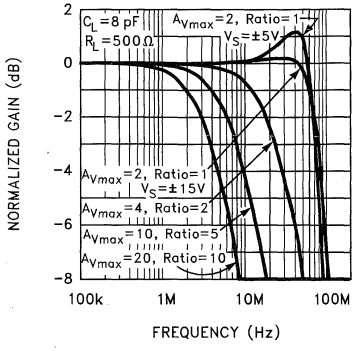
4451-3

Note: For typical performance curves, R_F = 0, R_G = ∞, V_{GAIN} = 1V, R_L = 500Ω, and C_L = 15 pF unless otherwise noted.

EL4451C
Wideband Variable-Gain Amplifier, Gain of 2

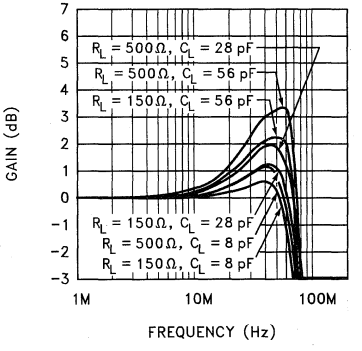
Typical Performance Curves

Frequency Response for Various Feedback Divider Ratios



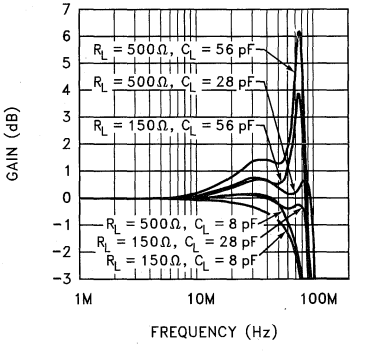
4451-4

Frequency Response for Various R_L, C_L V_S = ±5V



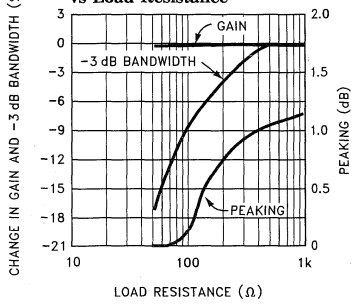
4451-5

Frequency Response for Various R_L, C_L V_S = ±15V



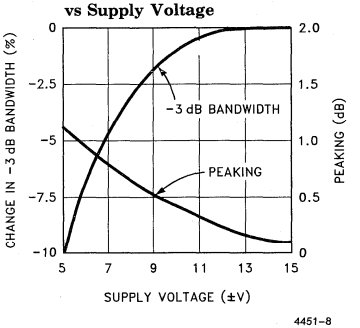
4451-6

Gain, −3 dB Bandwidth, and Peaking vs Load Resistance



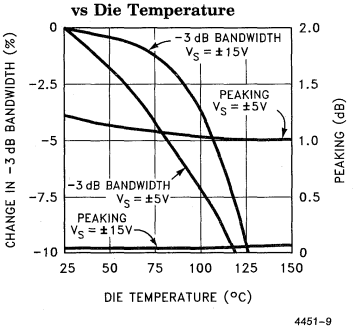
4451-7

−3 dB Bandwidth and Peaking vs Supply Voltage



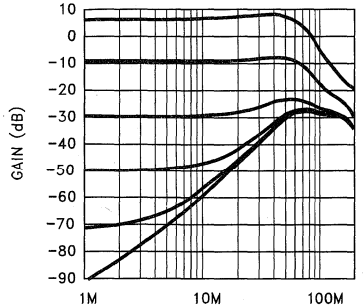
4451-8

−3 dB Bandwidth and Peaking vs Die Temperature



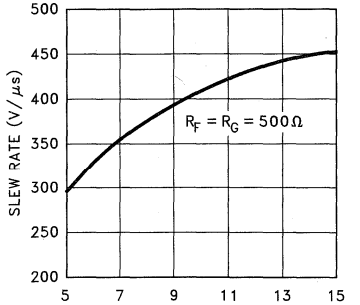
4451-9

Frequency Response for Various Gain Settings



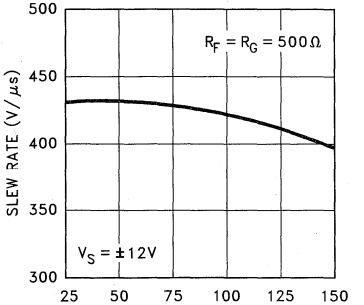
4451-10

Slew Rate vs Supply Voltage



4451-11

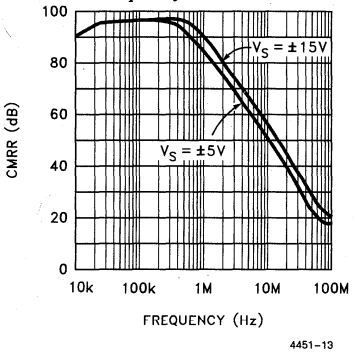
Slew Rate vs Die Temperature



4451-12

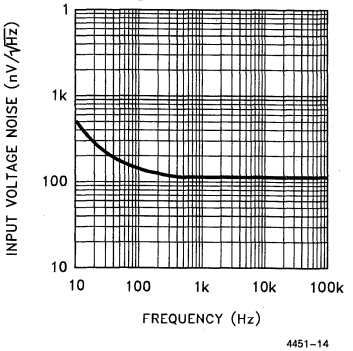
Typical Performance Curves — Contd.

Common-Mode Rejection Ratio vs Frequency



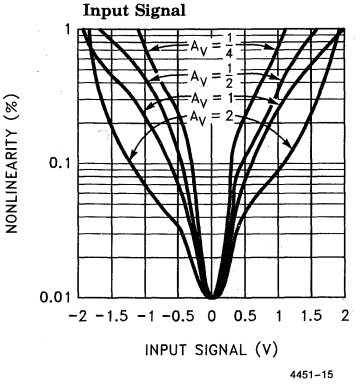
4451-13

Input Voltage Noise vs Frequency



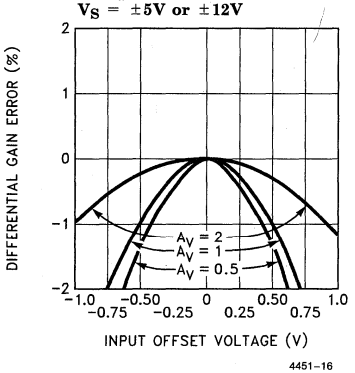
4451-14

Nonlinearity vs Input Signal



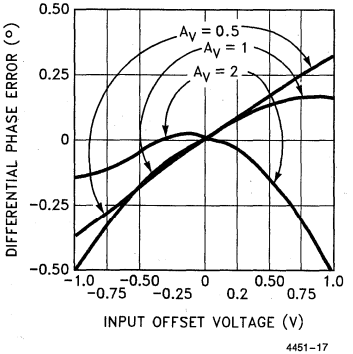
4451-15

Differential Gain Error vs Input Offset Voltage V_S = ±5V or ±12V



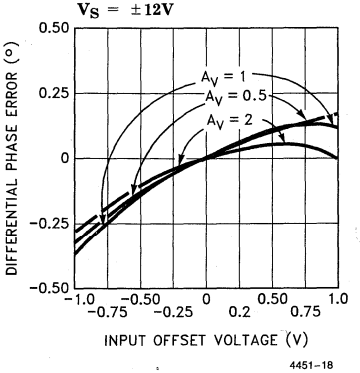
4451-16

Differential Phase Error vs Input Offset Voltage V_S = ±5V



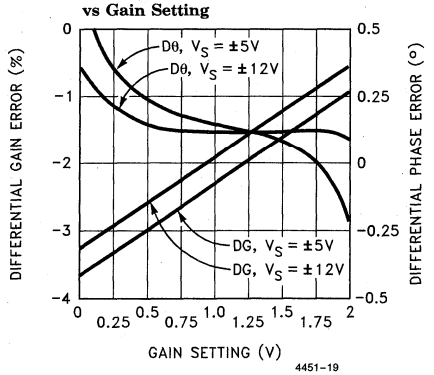
4451-17

Differential Phase Error vs Input Offset Voltage V_S = ±12V



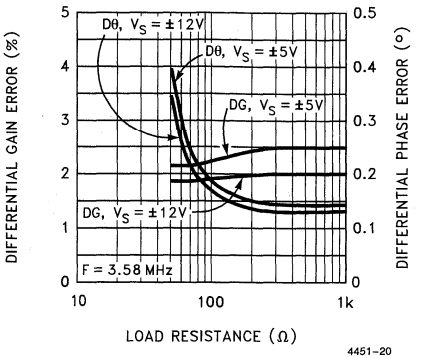
4451-18

Differential Gain and Phase Errors vs Gain Setting



4451-19

Differential Gain and Phase Errors vs Load Resistance

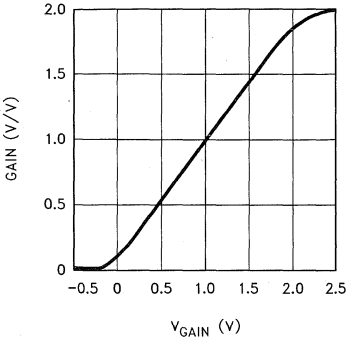


4451-20

EL4451C
Wideband Variable-Gain Amplifier, Gain of 2

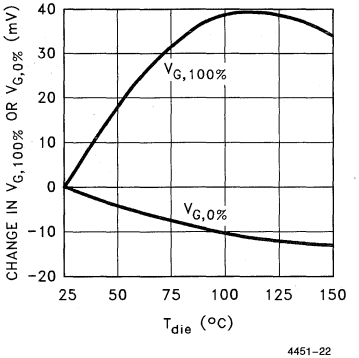
Typical Performance Curves — Contd.

Gain vs V_{GAIN}



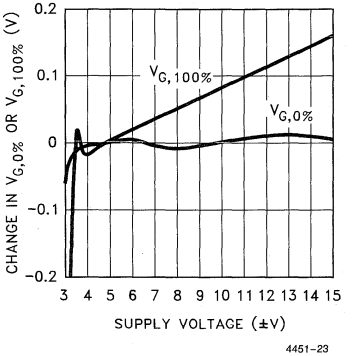
4451-21

Change in $V_{G,100\%}$ and $V_{G,0\%}$ vs Die Temperature



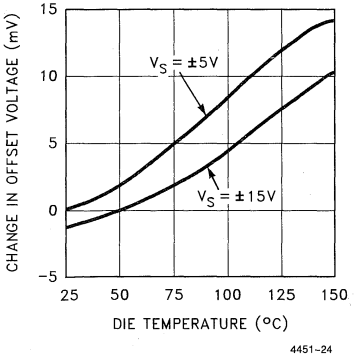
4451-22

$V_{G,0\%}$ and $V_{G,100\%}$ vs Supply Voltage



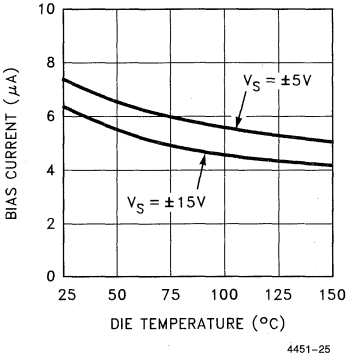
4451-23

Offset Voltage vs Die Temperature



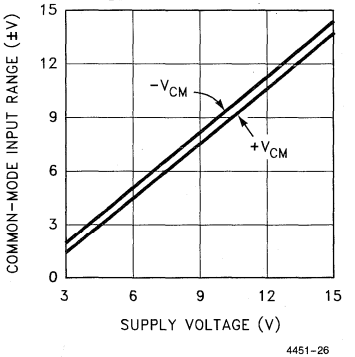
4451-24

Bias Current vs Die Temperature



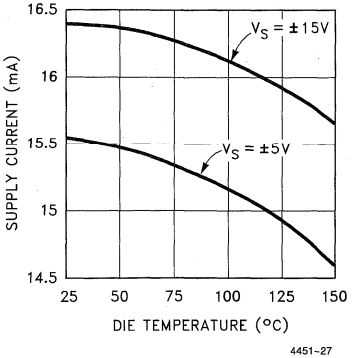
4451-25

Common Mode Input Range vs Supply Voltage



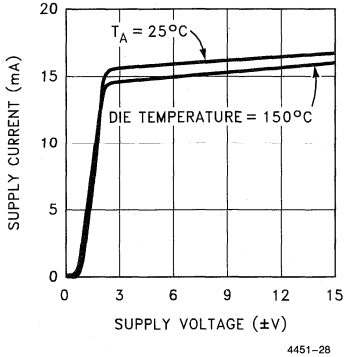
4451-26

Supply Current vs Die Temperature



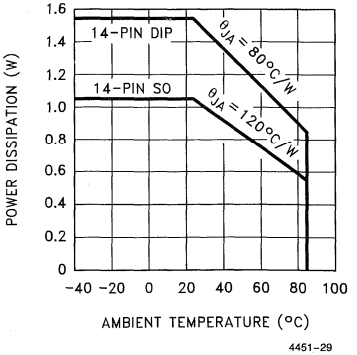
4451-27

Supply Current vs Supply Voltage



4451-28

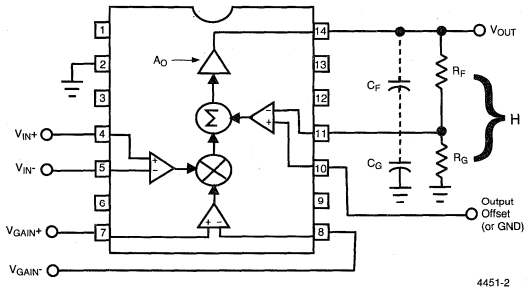
14-Pin Package Power Dissipation vs Ambient Temperature



4451-29

Applications Information

The EL4451 is a complete two-quadrant multiplier/gain control with 70 MHz bandwidth. It has three sets of inputs; a differential signal input V_{IN}, a differential gain-controlling input V_{GAIN}, and another differential input which is used to complete a feedback loop with the output. Here is a typical connection:



4451-2

The gain of the feedback divider is

$$H = \frac{R_G}{R_G + R_F}.$$

The transfer function of the part is

$V_{OUT} = A_O \times (((V_{IN}+) - (V_{IN}-)) \times ((V_{GAIN}+) - (V_{GAIN}-)) + (V_{REF} - V_{FB}))$.

V_{FB} is connected to V_{OUT} through a feedback network, so $V_{FB} = H \times V_{OUT}$. A_O is the open-loop gain of the amplifier, and is approximately 600. The large value of A_O drives

$((V_{IN}+) - (V_{IN}-)) \times ((V_{GAIN}+) - (V_{GAIN}-)) + (V_{REF} - V_{FB}) \rightarrow 0.$

Rearranging and substituting for V_{FB}

$V_{OUT} = (((V_{IN}+) - (V_{IN}-)) \times ((V_{GAIN}+) - (V_{GAIN})) + V_{REF})/H$, or

$V_{OUT} = (V_{IN} \times V_{GAIN} + V_{REF})/H$

Thus the output is equal to the difference of the V_{IN}'s times the difference of V_{GAIN}'s and offset by V_{REF}, all gained up by the feedback divider ratio. The EL4451 is stable for a direct connection between V_{OUT} and FB, and the divider may be used for higher output gain, although with the traditional loss of bandwidth.

It is important to keep the feedback divider's impedance at the FB terminal low so that stray capacitance does not diminish the loop's phase margin. The pole caused by the parallel impedance of the feedback resistors and stray capacitance should be at least 150 MHz; typical strays of 3 pF thus require a feedback impedance of 360Ω or less. Alternatively, a small capacitor across R_F can be used to create more of a frequency-compensated divider. The value of the capacitor should scale with the parasitic capacitance at the FB input. It is also practical to place small capacitors across both the feedback and the gain resistors (whose values maintain the desired gain) to swamp out parasitics. For instance, two 10pF capacitors across equal divider resistors for a maximum gain of 4 will dominate parasitic effects and allow a higher divider resistance.

The REF pin can be used as the output's ground reference, for DC offsetting of the output, or it can be used to sum in another signal.

Gain-Control Characteristics

The quantity V_{GAIN} in the above equations is bounded as $0 \leq V_{GAIN} \leq 2$, even though the externally applied voltages exceed this range. Actually, the gain transfer function around 0 and 2V is "soft"; that is, the gain does not clip abruptly below the 0%-V_{GAIN} voltage nor above the 100%-V_{GAIN} level. An overdrive of 0.3V must be applied to V_{GAIN} to obtain truly 0% or 100%. Because the 0%- or 100%- V_{GAIN} levels cannot be precisely determined, they are extrapolated from two points measured inside the slope of the gain transfer curve. Generally, an applied V_{GAIN} range of −0.5V to +2.5V will assure the full numerical span of $0 \leq V_{GAIN} \leq 2$.

The gain control has a small-signal bandwidth equal to the V_{IN} channel bandwidth, and overload recovery resolves in about 20 nsec.

Input Connections

The input transistors can be driven from resistive and capacitive sources, but are capable of oscillation when presented with an inductive input. It takes about 80nH of series inductance to make the inputs actually oscillate, equivalent to four inches of unshielded wiring or 6″ of unterminated input transmission line. The oscillation has a characteristic frequency of 500 MHz. Often placing one's finger (via a metal probe) or an oscilloscope probe on the input will kill the oscillation. Normal high-frequency construction obviates any such problems, where the input source is reasonably close to the input. If this is not possible, one can insert series resistors of around 51Ω to de-Q the inputs.

EL4451C
Wideband Variable-Gain Amplifier, Gain of 2

Applications Information — Contd.

Signal Amplitudes

Signal input common-mode voltage must be between (V−) + 3V and (V+) − 3V to ensure linearity. Additionally, the differential voltage on any input stage must be limited to ±6V to prevent damage. The differential signal range is ±2V in the EL4451. The input range is substantially constant with temperature.

The Ground Pin

The ground pin draws only 6μA maximum DC current, and may be biased anywhere between (V−) + 2.5V and (V+) − 3.5V. The ground pin is connected to the IC's substrate and frequency compensation components. It serves as a shield within the IC and enhances input stage CMRR and feedthrough over frequency, and if connected to a potential other than ground, it must be bypassed.

Power Supplies

The EL4451 works with any supplies from ±3V to ±15V. The supplies may be of different voltages as long as the requirements of the ground pin are observed (see the Ground Pin section). The supplies should be bypassed close to the device with short leads. 4.7μF tantalum capacitors are very good, and no smaller bypasses need be placed in parallel. Capacitors as small as 0.01μF can be used if small load currents flow.

Single-polarity supplies, such as +12V with +5V can be used, where the ground pin is connected to +5V and V− to ground. The inputs and outputs will have to have their levels shifted above ground to accommodate the lack of negative supply.

The power dissipation of the EL4451 increases with power supply voltage, and this must be compatible with the package chosen. This is a close estimate for the dissipation of a circuit:

$$P_D = 2 \times V_S \times I_{S,max} + (V_S - V_O) \times V_O/R_{PAR}$$

where I_S, max is the maximum supply current

V_S is the ± supply voltage (assumed equal)

V_O is the output voltage

R_{PAR} is the parallel of all resistors loading the output

For instance, the EL4451 draws a maximum of 18mA. With light loading, $R_{PAR} \rightarrow \infty$ and the dissipation with ±5V supplies is 180 mW. The maximum supply voltage that the device can run on for a given P_D and other parameters is

$$V_{S,max} = (P_D + V_O^2/R_{PAR}) / (2I_S + V_O/R_{PAR})$$

The maximum dissipation a package can offer is

$$P_{D,max} = (T_{J,max} - T_{A,max}) / \theta_{JA}$$

Where T_J, max is the maximum die temperature, 150°C for reliability, less to retain optimum electrical performance

T_A, max is the ambient temperature, 70°C for commercial and 85°C for industrial range

θ_{JA} is the thermal resistance of the mounted package, obtained from data sheet dissipation curves

The more difficult case is the SO-14 package. With a maximum die temperature of 150°C and a maximum ambient temperature of 85°C, the 65°C temperature rise and package thermal resistance of 120°C/W gives a dissipation of 542 mW at 85°C. This allows the full maximum operating supply voltage unloaded, but reduced if loaded.

Output Loading

The output stage of the EL4451 is very powerful. It typically can source 80mA and sink 120mA. Of course, this is too much current to sustain and the part will eventually be destroyed by excessive dissipation or by metal traces on the die opening. The metal traces are completely reliable while delivering the 30mA continuous output given in the Absolute Maximum Ratings table in this data sheet, or higher purely transient currents.

Gain changes only 0.2% from no load to 100Ω load. Heavy resistive loading will degrade frequency response and video distortion for loads <100Ω.

Capacitive loads will cause peaking in the frequency response. If capacitive loads must be driven, a small-valued series resistor can be used to isolate it. 12Ω to 51Ω should suffice. A 22Ω series resistor will limit peaking to 2.5 dB with even a 220pF load.

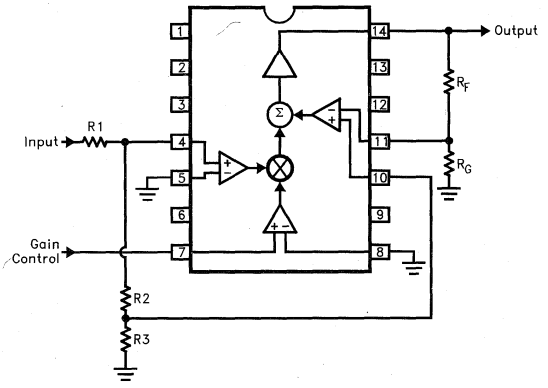
Applications Information — Contd.

Leveling Circuits

Often a variable-gain control is used to normalize an input signal to a standard amplitude from a modest range of possible input amplitude. A good example is in video systems, where an unterminated cable will yield a twice-sized standard video amplitude, and an erroneously twice-terminated cable gives a 2/3-sized input.

Here is a ±6 dB range preamplifier:

Linearized Leveling Amplifier



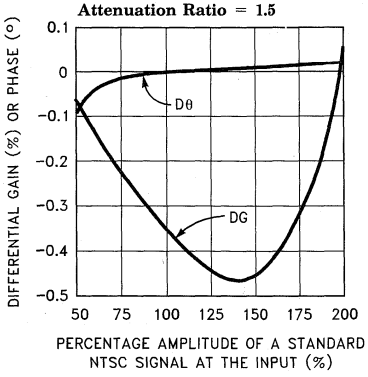
4451-30

In this arrangement, the EL4451 outputs a mixture of the signal routed through the multiplier and the REF terminal. The multiplier port produces the most distortion and needs to handle a fraction of an oversized video input, whereas the REF port is just like an op-amp input summing into the output. Thus, for oversized inputs the gain will be decreased and the majority of the signal is routed through the linear REF terminal. For undersized inputs, the gain is increased and the multiplier's contribution added to the output.

Here are some component values for two designs:

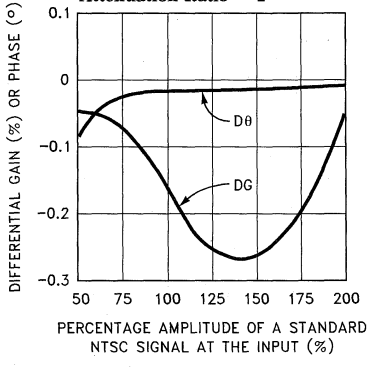
Attenuation Ratio	R_F	R_G	R_1	R_2	R_3	−3 dB Bandwidth
1.5	200Ω	400Ω	300Ω	100Ω	200Ω	47 MHz
2	400Ω	400Ω	500Ω	100Ω	200Ω	28 MHz

EL4451 Leveler Circuit
Attenuation Ratio = 1.5



4451-31

EL4451 Leveler Circuit
Attenuation Ratio = 2



4451-32

With the higher attenuation ratio, the multiplier sees a smaller input amplitude and distorts less, however the higher output gain reduces circuit bandwidth. As seen in the next curves, the peak differential gain error is 0.47% for the attenuation ratio of 1.5, but only 0.27% with the gain of 2 constants. To maintain bandwidth, an external op amp can be used instead of the R_F - R_G divider to boost the EL4451's output by the attenuation ratio.

Sinewave Oscillators

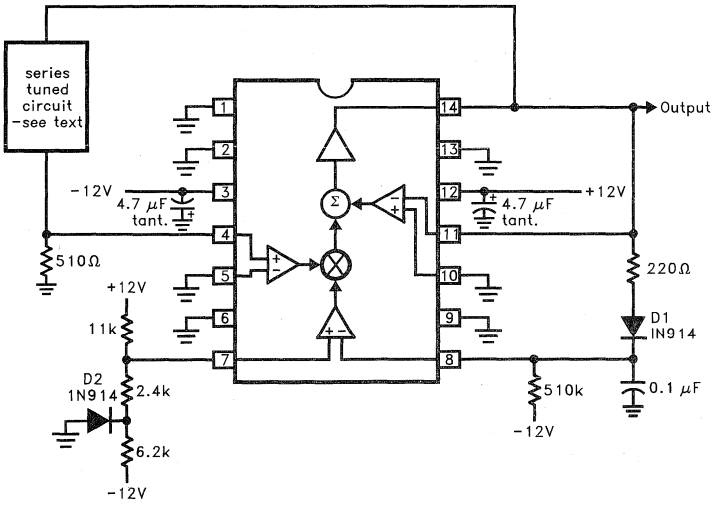
Generating a stable, low distortion sinewave has long been a difficult task. Because a linear oscillator's output tends to grow or diminish continuously, either a clipping circuit or automatic gain control (AGC) is needed. Clipping circuits generate severe distortion which needs subsequent filtering, and AGC's can be complicated.

EL4451C
Wideband Variable-Gain Amplifier, Gain of 2

Applications Information — Contd.

Here is the EL4451 used as an oscillator with simple AGC:

Low-Distortion Sinewave Oscillator



The oscillation frequency is set by the resonance of a series-tuned circuit, which may be an L-C combination or a crystal. At resonance, the series impedance of the tuned circuit drops and its phase lag is 0°, so the EL4451 needs a gain just over unity to sustain oscillation. The $V_{GAIN}-$ terminal is initially at $-0.7V$ and the $V_{GAIN}+$ terminal at about $+2.1V$, setting the maximum gain in the EL4451. At such high gain, the loop oscillates and output amplitude grows until D_1 rectifies more positive voltage at $V_{GAIN}-$, ultimately reducing gain until a stable 0.5Vrms output is produced.

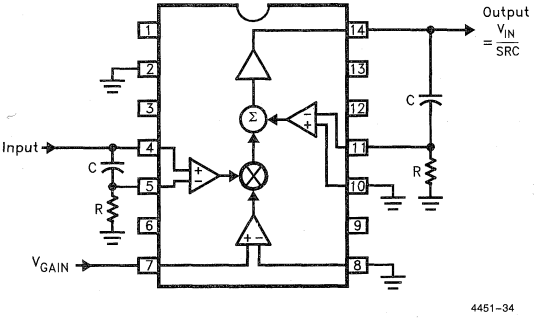
Using a 2 MHz crystal, output distortion was -53 dBc, or 0.22%. Sideband modulation was only 14 Hz wide at -90 dBc, limited by the filter of the spectrum analyzer used.

The circuit works up to 30 MHz. A parallel-tuned circuit can replace the 510Ω resistor and the 510Ω resistor moved in place of the series-tuned element to allow grounding of the tuned components.

Filters

The EL4451 can be connected to act as a voltage-variable integrator as shown:

EL4451 Connected As Variable Integrator

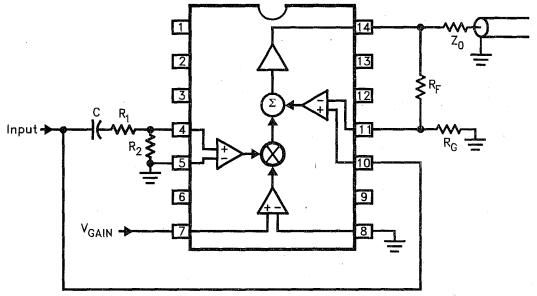


The input RC cancels a zero produced by the output op-amp feedback connection at $\omega = 1/RC$. With the input RC connected $V_{OUT}/V_{IN} = 1/sRC$; without it $V_{OUT}/V_{IN} = (1 + sRC)/sRC$. This variable integrator may be used in networks such as the Bi-quad. In some applications the input RC may be omitted. If a negative gain is required, the $V_{IN}+$ and $V_{IN}-$ terminals can be exchanged.

Applications Information — Contd.

A voltage-controlled equalizer and cable driver can be constructed so:

Equalization and Line Driver Amplifier



4451-35

The main signal path is via the REF pin. This ensures maximum signal linearity, while the multiplier input is used to allow a variable amount of frequency-shaped input from R_1, R_2, and C. For optimum linearity, the multiplier input is attenuated by R_1 and R_2. This may not be necessary, depending on input signal amplitude, and R_1 might be set to 0. $R_1$and R_2 should be set to provide sufficient peaking, depending on cable high-frequency losses, at maximum gain. R_F and R_G are chosen to provide the desired circuit gain, including backmatch resistor loss.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4452C

Wideband Variable-Gain Amplifier with Gain of 10

Features

- Complete variable-gain amplifier complete with output amplifier
- Compensated for Gain ≥ 10
- 50 MHz signal bandwidth
- 50 MHz gain-control bandwidth
- Low 29 nV/√Hz input noise
- Operates on ±5V to ±15V supplies
- All inputs are differential
- >70 dB attenuation @ 5 MHz

Applications

- AGC variable-gain amplifier
- IF amplifier
- Transducer amplifier

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4452CN	−40°C to +85°C	14-pin P-DIP	MDP0031
EL4452CS	−40°C to +85°C	14-lead SO	MDP0027

General Description

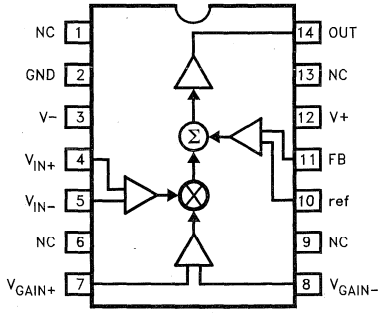
The EL4452 is a complete variable-gain circuit. It offers wide bandwidth and excellent linearity, while including a powerful output voltage amplifier, drawing modest current. The higher gain and lower input noise makes the EL4452 ideal for use in AGC systems.

The EL4452 operates on ±5V to ±15V and has an analog input range of ±0.5V. AC characteristics do not change appreciably over the supply range.

The circuit has an operational temperature of −40°C to +85°C and is packaged in 14-pin P-DIP and SO-14.

The EL4452 is fabricated with Elantec's proprietary complementary bipolar process which gives excellent signal symmetry and is very rugged.

Connection Diagram



EL4452C
Wideband Variable-Gain Amplifier with Gain of 10

Absolute Maximum Ratings (T_A = 25°C)

V+	Positive Supply Voltage	16.5V	I_{IN}	Current into any Input or Feedback Pin	4 mA
V_S	V+ to V− Supply Voltage	33V	I_{OUT}	Output Current	30 mA
V_{IN}	Voltage at any Input or Feedback	V+ to V−	P_D	Maximum Power Dissipation	See Curves
ΔV_{IN}	Difference between Pairs of Inputs or Feedback	6V	T_A	Operating Temperature Range	−40°C to +85°C
			T_S	Storage Temperature Range	−60°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open-Loop DC Electrical Characteristics

Power supplies at ±5V, T_A = 25°C, R_F = 910Ω, R_G = 100Ω, R_L = 500Ω

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{DIFF}	Signal Input Differential Input Voltage - Clipping	0.4	0.5		I	V
	0.6% Nonlinearity		0.4		V	V
V_{CM}	Common-Mode Range (All Inputs; V_{DIFF} = 0) V_S = ±5V	±2.0	±2.8		I	V
	V_S = ±15V	±12.0	±12.8		V	V
V_{OS}	Input Offset Voltage			10	I	mV
V_{OS}, FB	Output Offset Voltage			10	I	mV
V_G, 100%	Extrapolated Voltage for 100% Gain	1.8	2.1	2.2	I	V
V_G, 0%	Extrapolated Voltage for 0% Gain	−0.16	−0.06	0.04	I	V
V_G, 1V	Gain at V_{GAIN} = 1 (Rf = 910Ω, Rg = 100Ω)	4.9	5.35	5.9	I	V/V
I_B	Input Bias Current (All Inputs)	−20	−9	0	I	µA
I_{OS}	Input Offset Current Between V_{IN}+ and V_{IN}−, V_{GAIN}+ and V_{GAIN}−		0.5	4	I	µA
F_T	Signal Feedthrough, V_G = −1V		−100	−70	I	dB
R_{IN}, Signal	Input Resistance, Signal Input	25	60		I	kΩ
R_{IN}, Gain	Input Resistance, Gain Input	50	120		I	kΩ
R_{IN}, FB	Input Resistance, Feedback	25	60		V	kΩ
CMRR	Common-Mode Rejection Ratio, V_{IN}	70	90		I	dB

EL4452C
Wideband Variable-Gain Amplifier with Gain of 10

Open-Loop DC Electrical Characteristics — Contd.

Power supplies at ±5V, T_A = 25°C, R_F = 910Ω, R_G = 100Ω, R_L = 500Ω

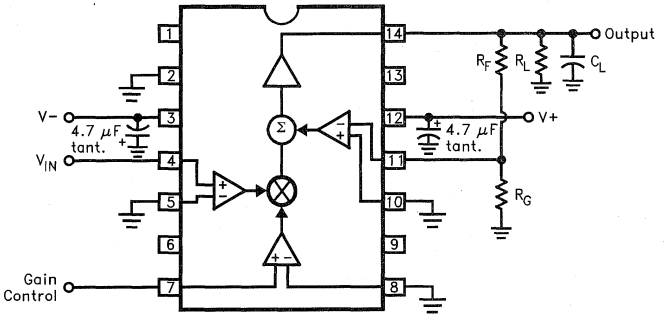
Parameter	Description		Min	Typ	Max	Test Level	Units
PSRR	Power-Supply Rejection Ratio, V_{OS}, FB; Supplies from ±5V to ±15V		65	83		I	dB
E_G	Gain Error, Excluding Feedback Resistors, V_{GAIN} = 2.5V		−7		+7	I	%
NL	Nonlinearity, V_{IN} from −0.25V to +0.25, V_{GAIN} = 1V			0.3	0.6	I	%
V_O	Output Voltage Swing	V_S = ±5V	±2.5	±2.8		I	V
	(V_{IN} = 0, V_{REF} Varied)	V_S = ±15V	±12.5	±12.8		I	V
I_{SC}	Output Short-Circuit Current		40	85		I	mA
I_S	Supply Current, V_S = ±15V			15.5	18	I	mA

Closed-Loop AC Electrical Characteristics

Power supplies at ±12V, T_A = 25°C, R_L = 500Ω, C_L = 15pF

Parameter	Description	Min	Typ	Max	Test Level	Units
BW, −3dB	−3dB Small-Signal Bandwidth, Signal Input		50		V	MHz
BW, ±0.1dB	0.1dB Flatness Bandwidth, Signal Input		10		V	MHz
Peaking	Frequency Response Peaking		0.1		V	dB
BW, Gain	−3dB Small-Signal Bandwidth, Gain Input		50		V	MHz
SR	Slew Rate, V_{OUT} between −2V and +2V	350	400	550	I	V/µs
V_N	Input-Referred Noise Voltage Density		29		V	nV/rt-Hz

Test Circuit

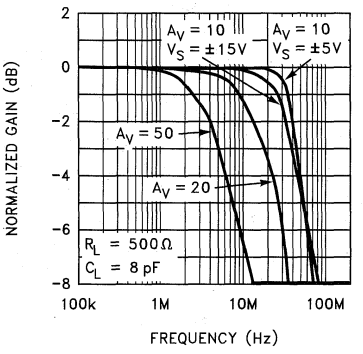


4452-2

Note: For typical performance curves, R_F = 910Ω, R_G = 100Ω, V_{GAIN} = 1V, R_L = 500Ω, and C_L = 15 pF unless otherwise noted.

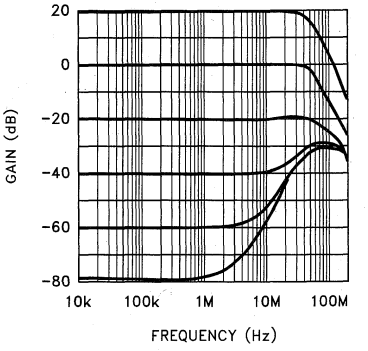
Typical Performance Curves

Frequency Response for Various Feedback Divider Ratios



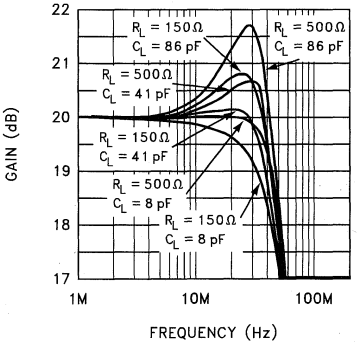
4452-3

Frequency Response for Various Gains



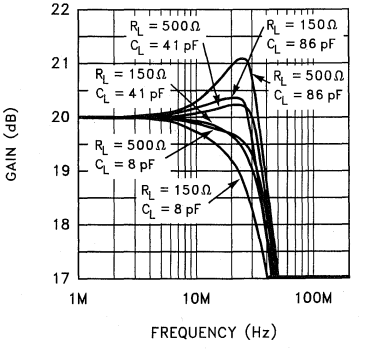
4452-4

Frequency Response for Various R_L, C_L, V_S = ±5V



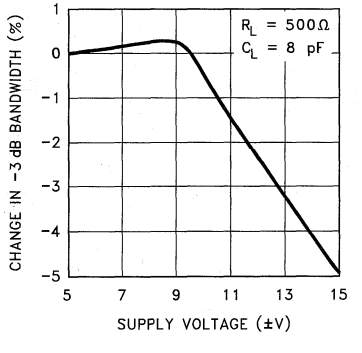
4452-5

Frequency Response for Various R_L, C_L, V_S = ±15V



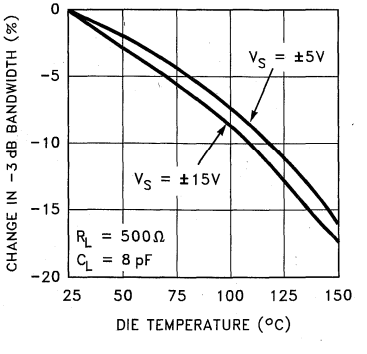
4452-6

−3 dB Bandwidth vs Supply Voltage



4452-7

−3 dB Bandwidth vs Die Temperature

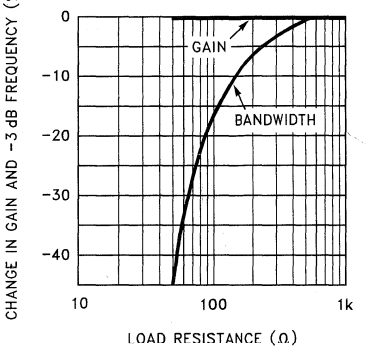


4452-8

EL4452C
Wideband Variable-Gain Amplifier with Gain of 10

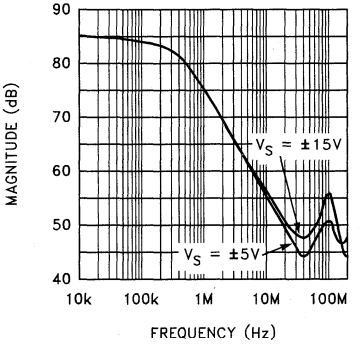
Typical Performance Curves — Contd.

Gain and −3 dB Bandwidth vs Load Resistance



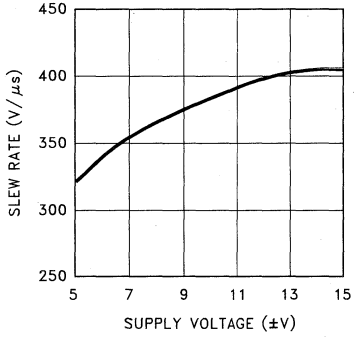
4452-9

Input Common-Mode Rejection Ratio vs Frequency



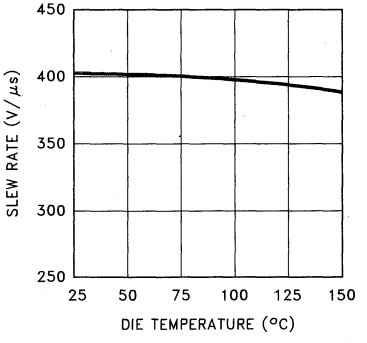
4452-10

Slew Rate vs Supply Voltage



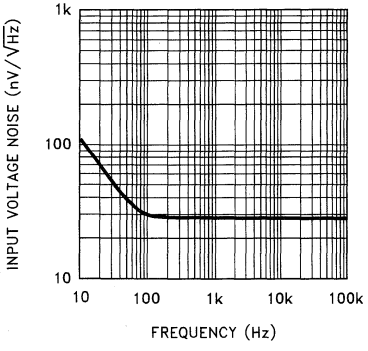
4452-11

Slew Rate vs Die Temperature



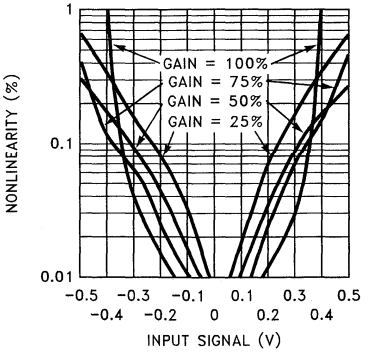
4452-12

Input Voltage Noise vs Frequency



4452-13

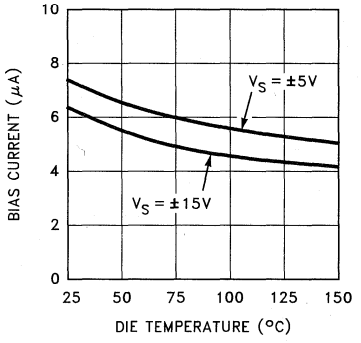
Nonlinearity vs Input Signal



4452-14

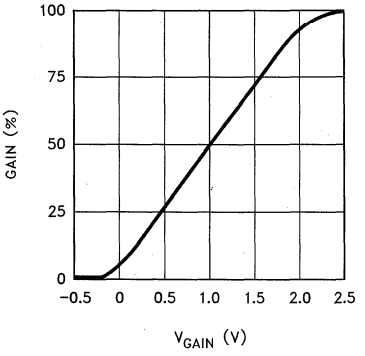
Typical Performance Curves — Contd.

Bias Current vs Die Temperature



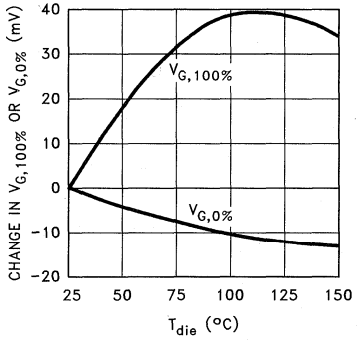
4452-15

Gain vs V_{GAIN}



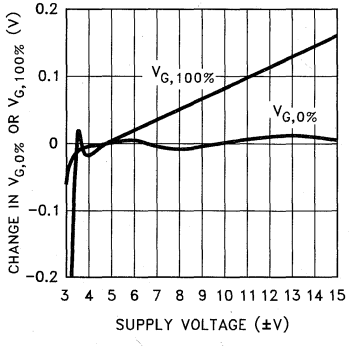
4452-16

Change in $V_{G,100\%}$ and $V_{G,0\%}$ vs Die Temperature



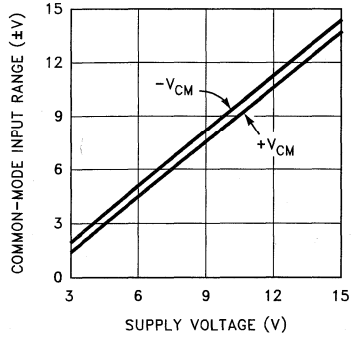
4452-17

$V_{G,0\%}$ and $V_{G,100\%}$ vs Supply Voltage



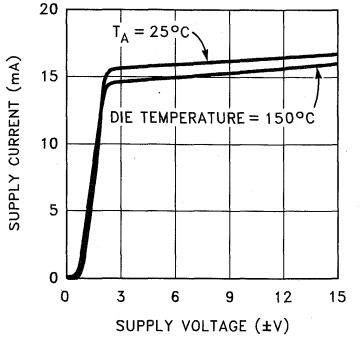
4452-18

Common Mode Input Range vs Supply Voltage



4452-19

Supply Current vs Supply Voltage

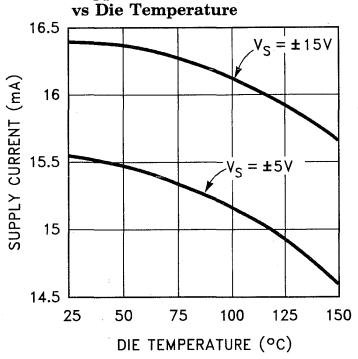


4452-20

EL4452C
Wideband Variable-Gain Amplifier with Gain of 10

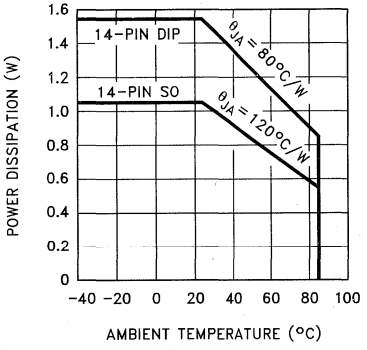
Typical Performance Curves — Contd.

Supply Current vs Die Temperature



4452-21

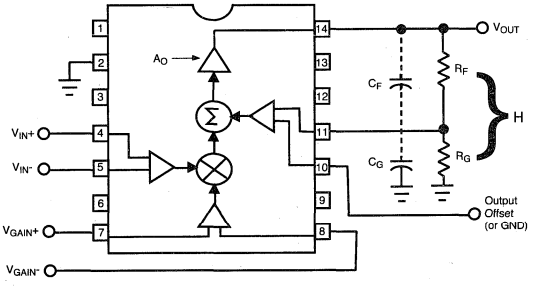
14-Pin Package Power Dissipation vs Ambient Temperature



4452-22

Applications Information

The EL4452 is a complete two-quadrant multiplier/gain control with 50 MHz bandwidth. It has three sets of inputs; a differential signal input V_{IN}, a differential gain-controlling input V_{GAIN}, and another differential input which is used to complete a feedback loop with the output. Here is a typical connection:



4451-23

The gain of the feedback divider is H. The transfer function of the part is

$V_{OUT} = A_O \times (((V_{IN}+) - (V_{IN}-)) \times ((V_{GAIN}+) - (V_{GAIN}-)) + (V_{REF} - V_{FB}))$.

V_{FB} is connected to V_{OUT} through a feedback network, so $V_{FB} = H \times V_{OUT}$. A_O is the open-loop gain of the amplifier, and is approximately 3300. The large value of A_O drives

$((V_{IN}+) - (V_{IN}-)) \times \frac{1}{2}((V_{GAIN}+) - (V_{GAIN}-)) + (V_{REF} - V_{FB}) \rightarrow 0$.

Rearranging and substituting for V_{FB}

$V_{OUT} = (((V_{IN}+) - (V_{IN}-)) \times \frac{1}{2}((V_{GAIN}+) - (V_{GAIN})) + V_{REF})/H$,

or

$V_{OUT} = (V_{IN} \times \frac{1}{2} V_{GAIN} + V_{REF})/H$

Applications Information — Contd.

Thus the output is equal to the difference of the V_{IN}'s times the difference of V_{GAIN}'s and offset by V_{REF}, all gained up by the feedback divider ratio. The EL4452 is stable for a divider ratio of $\frac{1}{10}$, and the divider may be set for higher output gain, although with the traditional loss of bandwidth.

It is important to keep the feedback divider's impedance at the FB terminal low so that stray capacitance does not diminish the loop's phase margin. The pole caused by the parallel impedance of the feedback resistors and stray capacitance should be at least 130 MHz; typical strays of 3 pF thus require a feedback impedance of 400Ω or less. Alternatively, a small capacitor across R_F can be used to create more of a frequency-compensated divider. The value of the capacitor should scale with the parasitic capacitance at the FB input. It is also practical to place small capacitors across both the feedback and the gain resistors (whose values maintain the desired gain) to swamp out parasitics. For instance, a 3 pF capacitor across R_F and 27 pF to ground will dominate parasitic effects in a $\frac{1}{10}$ divider and allow a higher divider resistance.

The REF pin can be used as the output's ground reference, for DC offsetting of the output, or it can be used to sum in another signal.

Gain-Control Characteristics

The quantity V_{GAIN} in the above equations is bounded as $0 \leq V_{GAIN} \leq 2$, even though the externally applied voltages exceed this range. Actually, the gain transfer function around 0 and 2V is "soft"; that is, the gain does not clip abruptly below the 0%-V_{GAIN} voltage nor above the 100%-V_{GAIN} level. An overdrive of 0.3V must be applied to V_{GAIN} to obtain truly 0% or 100%. Because the 0%- or 100%- V_{GAIN} levels cannot be precisely determined, they are extrapolated from two points measured inside the slope of the gain transfer curve. Generally, an applied V_{GAIN} range of −0.5V to +2.5V will assure the full numerical span of $0 \leq V_{GAIN} \leq 2$.

The gain control has a small-signal bandwidth equal to the V_{IN} channel bandwidth, and overload recovery resolves in about 20 nsec.

Input Connections

The input transistors can be driven from resistive and capacitive sources, but are capable of oscillation when presented with an inductive input. It takes about 80nH of series inductance to make the inputs actually oscillate, equivalent to four inches of unshielded wiring or 6″ of unterminated input transmission line. The oscillation has a characteristic frequency of 500 MHz. Often placing one's finger (via a metal probe) or an oscilloscope probe on the input will kill the oscillation. Normal high-frequency construction obviates any such problems, where the input source is reasonably close to the input. If this is not possible, one can insert series resistors of around 51Ω to de-Q the inputs.

Signal Amplitudes

Signal input common-mode voltage must be between (V−) + 2.5V and (V+) − 2.5V to ensure linearity. Additionally, the differential voltage on any input stage must be limited to ±6V to prevent damage. The differential signal range is ±0.5V in the EL4452. The input range is substantially constant with temperature.

The Ground Pin

The ground pin draws only 6 μA maximum DC current, and may be biased anywhere between (V−)+2.5V and (V+)−3.5V. The ground pin is connected to the IC's substrate and frequency compensation components. It serves as a shield within the IC and enhances input stage CMRR and feedthrough over frequency, and if connected to a potential other than ground, it must be bypassed.

Power Supplies

The EL4452 operates with power supplies from ±3V to ±15V. The supplies may be of different voltages as long as the requirements of the ground pin are observed (see the Ground Pin section). The supplies should be bypassed close to the device with short leads. 4.7 μF tantalum capacitors are very good, and no smaller bypasses need be placed in parallel. Capacitors as small as 0.01 μF can be used if small load currents flow.

Single-polarity supplies, such as +12V with +5V can be used, where the ground pin is connected to +5V and V− to ground. The inputs

EL4452C
Wideband Variable-Gain Amplifier with Gain of 10

Applications Information — Contd.

and outputs will have to have their levels shifted above ground to accommodate the lack of negative supply.

The power dissipation of the EL4452 increases with power supply voltage, and this must be compatible with the package chosen. This is a close estimate for the dissipation of a circuit:

$$P_D = 2 \times V_S \times I_S, \max + (V_S - V_O) \times V_O / R_{PAR}$$

where I_S, max is the maximum supply current

V_S is the ± supply voltage (assumed equal)

V_O is the output voltage

R_{PAR} is the parallel of all resistors loading the output

For instance, the EL4452 draws a maximum of 18mA. With light loading, $R_{PAR} \rightarrow \infty$ and the dissipation with ±5V supplies is 180 mW. The maximum supply voltage that the device can run on for a given P_D and other parameters is

$$V_S, \max = (P_D + V_O^2/R_{PAR})/(2I_S + V_O/R_{PAR})$$

The maximum dissipation a package can offer is

$$P_D, \max = (T_J, \max - T_A, \max) / \theta_{JA}$$

Where T_J, max is the maximum die temperature, 150°C for reliability, less to retain optimum electrical performance

T_A, max is the ambient temperature, 70°C for commercial and 85°C for industrial range

θ_{JA} is the thermal resistance of the mounted package, obtained from data sheet dissipation curves

The more difficult case is the SO-14 package. With a maximum die temperature of 150°C and a maximum ambient temperature of 85°C, the 65°C temperature rise and package thermal resistance of 120°C/W gives a dissipation of 542 mW at 85°C. This allows the full maximum operating supply voltage unloaded, but reduced if loaded.

Output Loading

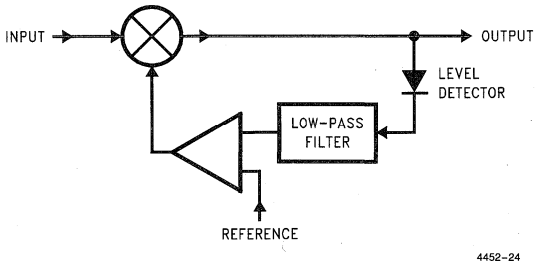
The output stage of the EL4452 is very powerful. It can typically source 80 mA and sink 120 mA. Of course, this is too much current to sustain and the part will eventually be destroyed by excessive dissipation or by metal traces on the die opening. The metal traces are completely reliable while delivering the 30 mA continuous output given in the Absolute Maximum Ratings table in this data sheet, or higher purely transient currents.

Gain changes only 0.2% from no load to a 100Ω load. Heavy resistive loading will degrade frequency response and distortion for loads <100Ω.

Capacitive loads will cause peaking in the frequency response. If capacitive loads must be driven, a small-valued series resistor can be used to isolate it. 12Ω to 51Ω should suffice. A 22Ω series resistor will limit peaking to 1 dB with even a 220 pF load.

AGC Circuits

The basic AGC (automatic gain control) loop is this:



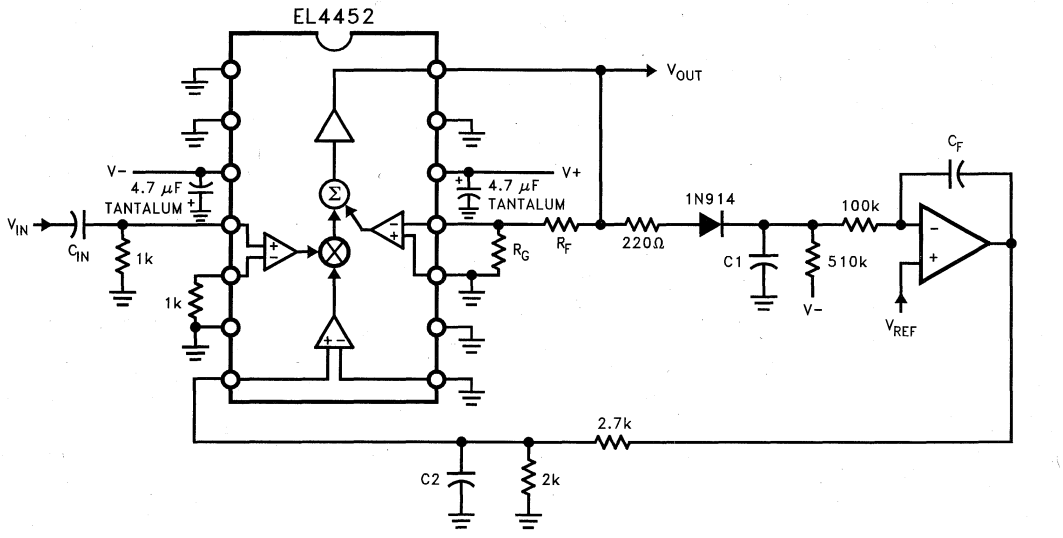
Basic AGC Loop

A multiplier scales the input signal and provides necessary gain and buffers the signal presented to the output load, a level detector (shown schematically here as a diode) converts some measure of the output signal amplitude to a DC level, a low-pass filter attenuates any signal ripple present on that DC level, and an amplifier compares that level to a reference and amplifies the error to create a gain-control voltage for the multiplier. The circuitry is a servo that attempts to keep the output amplitude constant by continuously adjusting the multiplier's gain control input.

Applications Information — Contd.

Most AGC's deal with repetitive input signals that are capacitively coupled. It is generally desirable to keep DC offsets from mixing with AC signals and fooling the level detector into maintaining the DC output offset level constant, rather than a smaller AC component. To that end, either the level detector is AC-coupled, or the reference voltage must be made greater than the maximum multiplier gain times the input offset. For instance, if the level detector output equaled the reference voltage at 1V of EL4452 output, the 8 mV of input offset would require a maximum gain of 125 through the EL4452. Bias current-induced offsets could increase this further.

Depending on the nature of the signal, different level detector strategies will be employed. If the system goal is to prevent overload of subsequent stages, peak detectors are preferred. Other strategies use an RMS detector to maintain constant output power. Here is a simple AGC using peak detection:



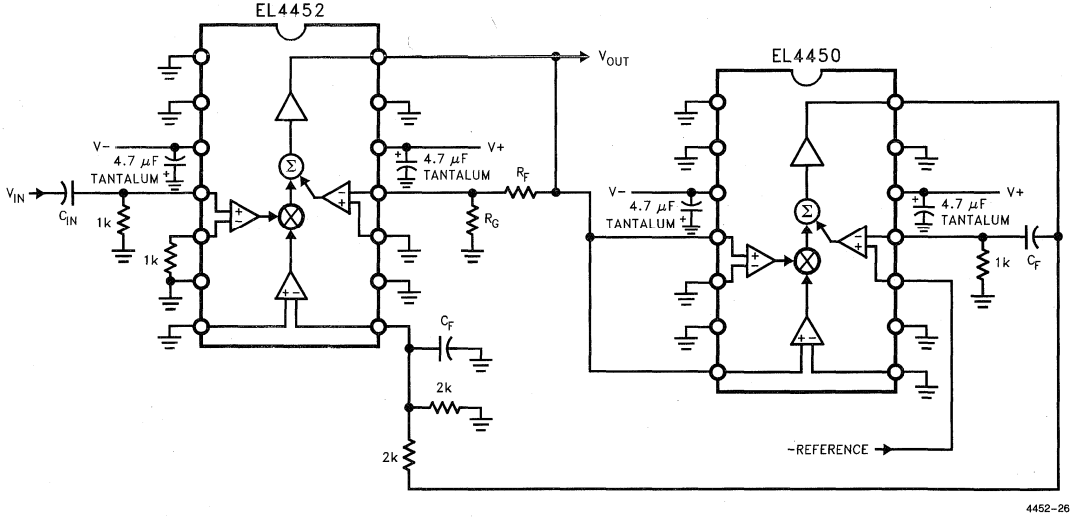
EL4452C
Wideband Variable-Gain Amplifier with Gain of 10

Applications Information — Contd.

The output of the EL4452 drives a diode detector which is compared to V_{REF} by an offset integrator. Its output feeds the gain-control input of the EL4452. The integrator's output is attenuated by the 2 kΩ and 2.7 kΩ resistors to prevent the op-amp from overloading the gain-control pin during zero input conditions. The 510 kΩ resistor provides a pull-down current to the peak level storage capacitor C1 to allow it to drift negative when output amplitude reduces. Thus the detector is of fast attack and slow decay design, able to reduce AGC gain rapidly when signal amplitude suddenly increases, and increases gain slowly when the input drops out momentarily. The value of C1 determines drop-out reaction rates, and the value of C_F affects overall loop time constant as well as the amount of ripple on the gain-control line. C2 can be used to reduce this ripple further, although it contributes to loop overshoot when input amplitude changes suddenly. The op-amp can be any inexpensive low-frequency type.

The major problem with diode detectors is their large and variable forward voltage. They require at least a 2 V_{P-P} peak output signal to function reliably, and the forward voltage should be compensated by including a negative V_D added to V_{REF}. Even this is only moderately successful. At the expense of bandwidth, op-amp circuits can greatly improve diode rectifiers (see "An Improved Peak Detector", an Elantec application note). Fortunately, the detector will see a constant amplitude of signal if the AGC is operating correctly.

A better-calibrated method is to use a four-quadrant multiplier as a square-law detector. Here is a circuit employing the EL4450:



Applications Information — Contd.

In this circuit, the EL4450 not only calculates the square of the input, but also provides the offset integrator function. The product of the two multiplier inputs adds to the −Reference input and are passed to the output amplifier, which through C_F behaves as a pseudo-integrator. The "integrator" gain does not pass through zero at high frequencies but has a zero at $1/(2\pi C_F \times 1\ k\Omega)$. This zero is cancelled by the pole caused by the second capacitor of value C_F connected at the EL4452 $-V_{GAIN}$ input. The −Reference can be exchanged for a positive reference by connecting it to the ground return of the 1 kΩ resistor at the FB terminal and grounding REF.

As a general consideration, the input signal applied to an EL4452 should be kept below about 250 mV peak for good linearity. If the AGC were designed to produce a 1V peak output, the input range would be 100 mV–250 mV peak when the EL4452 has a feedback network that establishes a maximum gain of 10. This is an input range of only 2.5:1 for precise output regulation. Raising the maximum gain to 25 allows a 40 mV–250 mV input range with the output still regulated, better than 6:1. Unfortunately, the bandwidth will be reduced. Bandwidth can be maintained by adding a high frequency op-amp cascaded with the output to make up gain beyond the 10 of the EL4452, current feedback devices being the most flexible. The op-amp's input should be capacitor coupled to prevent gained-up offsets from confusing the level detector during AGC control line variations.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4453C
Video Fader

Features

- Complete two-input fader with output amplifier—uses no extra components
- 80 MHz bandwidth
- Fast fade control speed
- Operates on ±5V to ±15V supplies
- >60 dB attenuation @ 5 MHz

Applications

- Mixing two inputs
- Picture-in-picture
- Text overlay onto video
- General gain control

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL4453CN	−40°C to +85°C	14-Pin P-DIP	MDP0031
EL4453CS	−40°C to +85°C	14-Lead SOIC	MDP0027

General Description

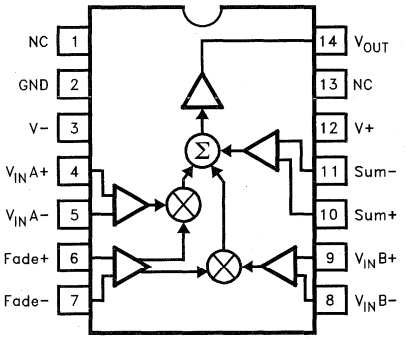
The EL4453C is a complete fader subsystem. It variably blends two inputs together for such applications as video picture-in-picture effects.

The EL4453C operates on ±5V to ±15V supplies and has an analog differential input range of ±2V. AC characteristics do not change appreciably over the supply range.

The circuit has an operational temperature of −40°C to +85°C and is packaged in 14-pin P-DIP and SO-14.

The EL4453C is fabricated with Elantec's proprietary complementary bipolar process which gives excellent signal symmetry and is free from latch up.

Connection Diagram



4453-1

Absolute Maximum Ratings $T_A = 25°C$

V+	Positive Supply Voltage	16.5V	I_{IN}	Current into any Input, or Feedback Pin	4 mA
V_S	V+ to V− Supply Voltage	33V	I_{OUT}	Output Current	30 mA
V_{IN}	Voltage at any Input or Feedback	V+ to V−	P_D	Maximum Power Dissipation	See Curves
ΔV_{IN}	Difference between Pairs		T_A	Operating Temperature Range	−40°C to +85°C
	of Inputs or Feedback	6V	T_S	Storage Temperature Range	−60°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25°C$ for information purposes only.

Open-Loop DC Electrical Characteristics

Power Supplies at ±5V, Sum+ = Sum− = 0, $T_A = 25°C$

Parameter	Description		Min	Typ	Max	Test Level	Units
V_{DIFF}	$V_{IN}A$, $V_{IN}B$, or Sum Differential Input Voltage—	Clipping	1.8	2.0		I	V
		0.2% Nonlinearity		0.7		V	V
V_{CM}	Common-Mode Range (All Inputs; $V_{DIFF} = 0$)	$V_S = \pm5V$	±2.5	±2.8		I	V
		$V_S = \pm15V$	±12.5	±12.8		I	V
V_{OS}	A or B Input Offset Voltage				25	I	mV
V_{FADE}, 100%	Extrapolated Voltage for 100% Gain for $V_{IN}A$		0.9	1.05	1.2	I	V
V_{FADE}, 0%	Extrapolated Voltage for 0% Gain for $V_{IN}A$		−1.2	−1.15	−0.9	I	V
I_B	Input Bias Current (All Inputs) with all $V_{IN} = 0$			9	20	I	µA
I_{OS}	Input Offset Current between $V_{IN}A+$ and $V_{IN}A-$, $V_{IN}B+$ and $V_{IN}B-$, Fade+ and Fade−, and Sum+ and Sum−			0.2	4	I	µA
F_T	$V_{IN}A$ Signal Feedthrough, $V_{FADE} = -1.5V$			−100	−60	I	dB
NL	A or B Input Nonlinearity, V_{IN} between +1V and −1V,	$V_{IN}A$ or $V_{IN}B$		0.2	0.5	I	%
		Sum Input		0.5		V	%
R_{IN}, Signal	Input Resistance, A, B, or Sum Input			230		V	kΩ
R_{IN}, Fade	Input Resistance, Fade Input			120		V	kΩ
CMRR	Common-Mode Rejection Ratio, $V_{IN}A$ or $V_{IN}B$		70	80		I	dB
PSRR	Power Supply Rejection Ratio		50	70		I	dB
E_G	Gain Error, $V_{FADE} = 1.5V$,	$V_{IN}A$ or $V_{IN}B$	−2		+2	I	%
		Sum Input	−4		+4	I	%
V_O	Output Voltage Swing	$V_S = \pm5V$	±2.5	±2.8		I	V
	($V_{IN} = 0$, V_{REF} Varied)	$V_S = \pm15V$	±12.5	±12.8		I	V
I_{SC}	Output Short-Circuit Current		40	85		I	mA
I_S	Supply Current, $V_S = \pm15V$			17	21	I	mA

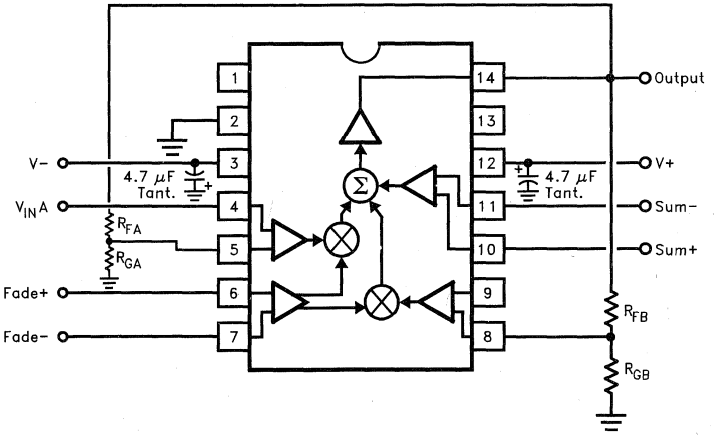
EL4453C
Video Fader

Closed-Loop AC Electrical Characteristics

Power supplies at ±12V, T_A = 25°C, R_L = 500Ω, C_L = 15 pF, V_{FADE} = 1.5V, Sum+ = Sum− = 0

Parameter	Description	Min	Typ	Max	Test Level	Units
BW, −3 dB	−3 dB Small-Signal Bandwidth, $V_{IN}A$ or $V_{IN}B$		80		V	MHz
BW, ±0.1 dB	0.1 dB Flatness Bandwidth, $V_{IN}A$ or $V_{IN}B$		9		V	MHz
Peaking	Frequency Response Peaking		1.0		V	dB
BW, Fade	−3 dB Small-Signal Bandwidth, Fade Input		80		V	MHz
SR	Slew Rate, V_{OUT} between −2V and +2V	TBD	380		I	V/µs
V_N	Input-Referred Noise Voltage Density		160		V	nV/Hz
F_T	Feedthrough of Faded-Out Channel, F = 3.58 MHz		−63		V	dB
dG	Differential Gain Error, V_{OFFSET} from 0 to ±0.714V, Fade at 100%					
	$V_{IN}A$ or $V_{IN}B$		0.05		V	%
	Sum Input		0.35		V	%
dθ	Differential Phase Error, V_{OFFSET} from 0 to ±0.71V, Fade at 100%					
	$V_{IN}A$ or $V_{IN}B$		0.05		V	(°)
	Sum Input		0.1		V	(°)

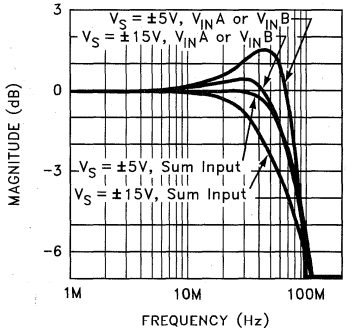
Test Circuit



Note: For typical performance curves Sum+ = Sum− = 0, R_F = 0Ω, R_G = ∞, V_{FADE} = +1.5V, and C_L = 15 pF, unless otherwise noted.

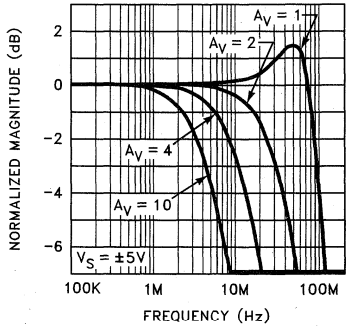
Typical Performance Curves

Frequency Response



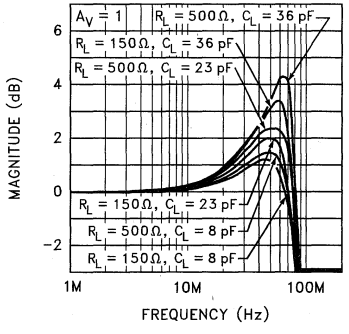
4453-3

Frequency Response vs Gain



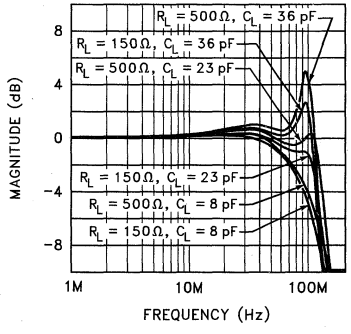
4453-4

Frequency Response for Various Loads, V_S = ±5V



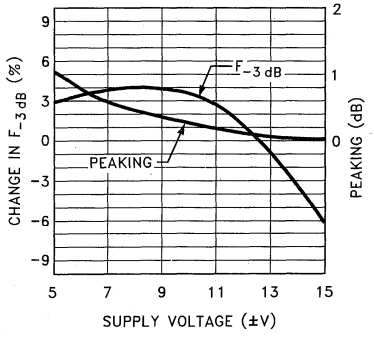
4453-6

Frequency Response for Various Loads, V_S = ±15V



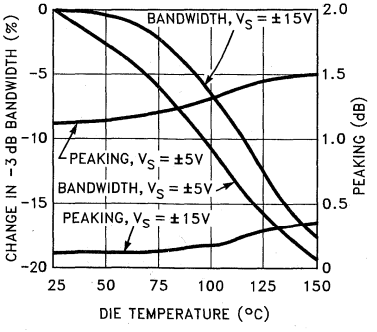
4453-7

−3 dB Bandwidth and Peaking vs Supply Voltage



4453-9

−3 dB Bandwidth and Peaking vs Die Temperature

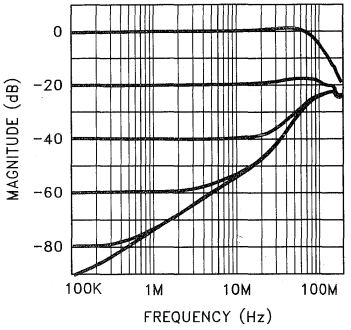


4453-10

EL4453C
Video Fader

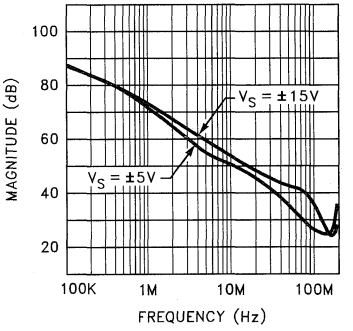
Typical Performance Curves — Contd.

Frequency Response for Different Gains, V_S = ±5V



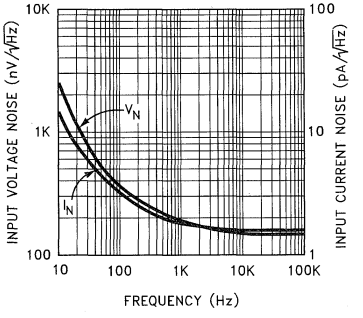
4453-5

Input Common-Mode Rejection Ratio vs Frequency



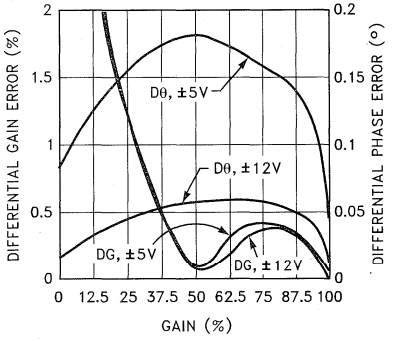
4453-8

Input Voltage and Current Noise vs Frequency



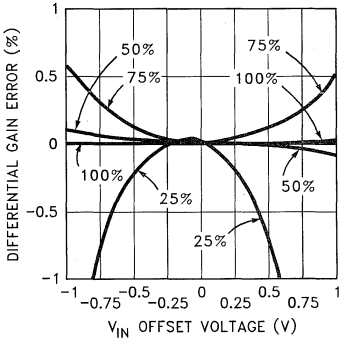
4453-11

V_{IN} Differential Gain and Phase Error vs Gain



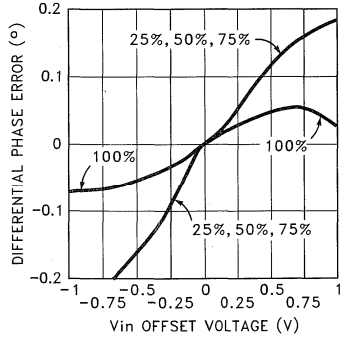
4453-14

V_{IN} Differential Gain Error vs Input Offset Voltage for Gain = 100%, 75%, 50% and 25%



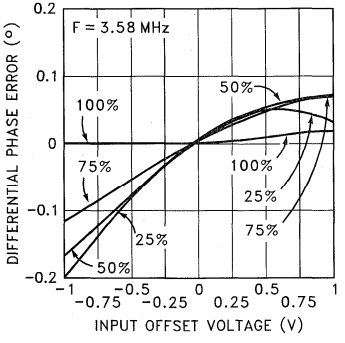
4453-15

V_{IN} Differential Phase Error vs Input Offset Voltage for Gain = 100%, 75%, 50% and 25%. V_S = ±5V



4453-16

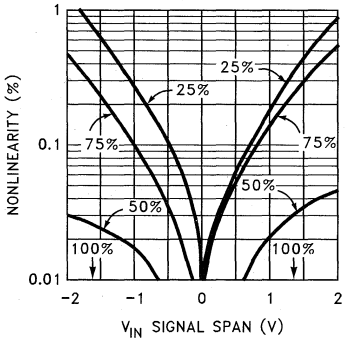
V_{IN} Differential Phase Error vs Input Offset Voltage for Gain = 100%, 75%, 50% and 25%. V_S = ±12V



4453-17

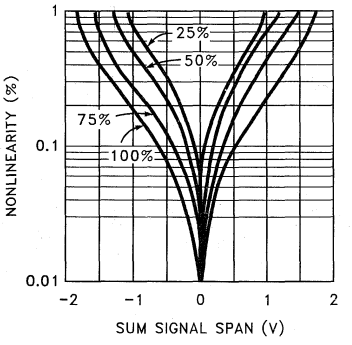
Typical Performance Curves — Contd.

Nonlinearity vs V_{IN} Signal Span



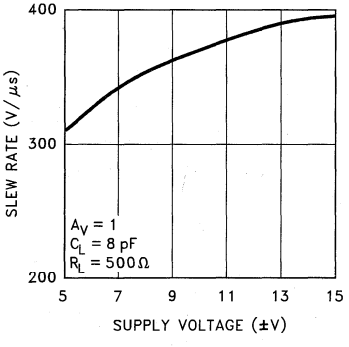
4453-12

Nonlinearity vs Sum Signal Span



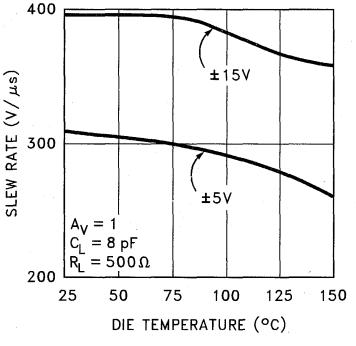
4453-13

Slew Rate vs Supply Voltage



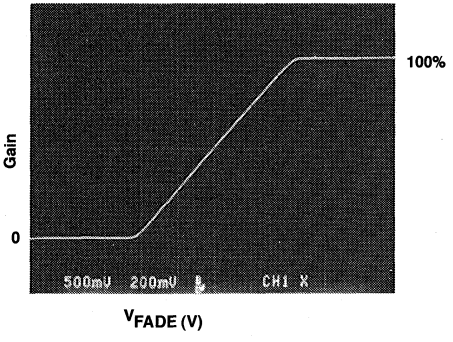
4453-18

Slew Rate vs Die Temperature



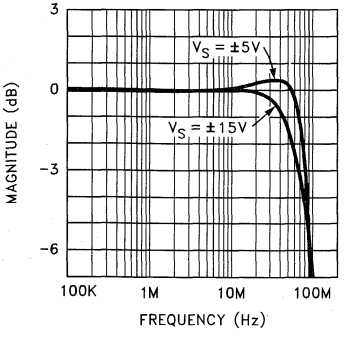
4453-19

V_{IN}A Gain vs V_{FADE}



4453-20

Frequency Response of Fade Input

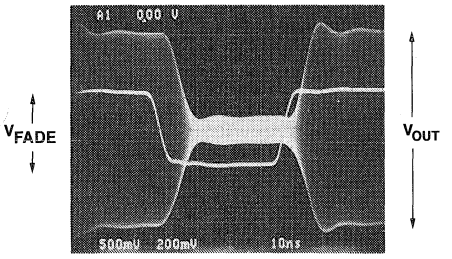


4453-21

EL4453C
Video Fader

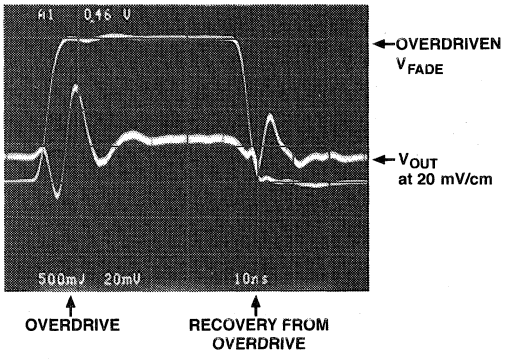
Typical Performance Curves — Contd.

Transient Response of Fade Input Constant Signal into $V_{IN}A$



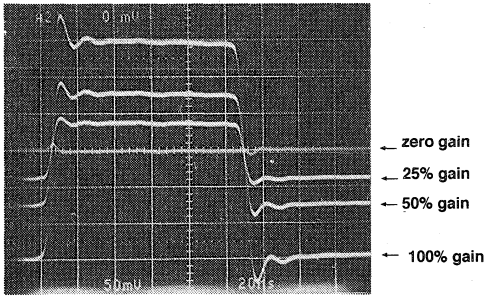
4453-22

Overdrive Recovery Glitch from V_{FADE}, No Input Signal



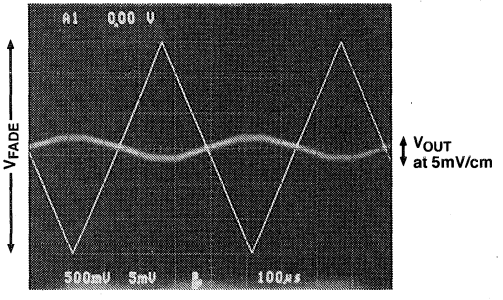
4453-23

$V_{IN}A$ Transient Response for Various Gains



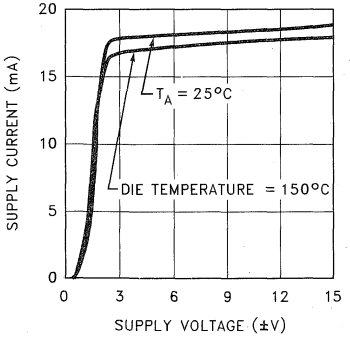
4453-24

Cross-Fade Balance with $V_{IN}A = V_{IN}B = 0$



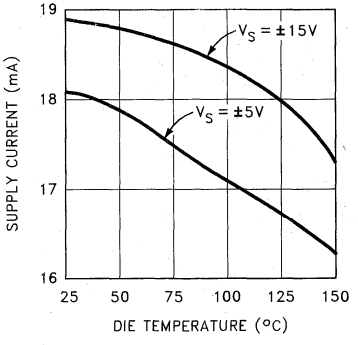
4453-25

Supply Current vs Supply Voltage



4453-26

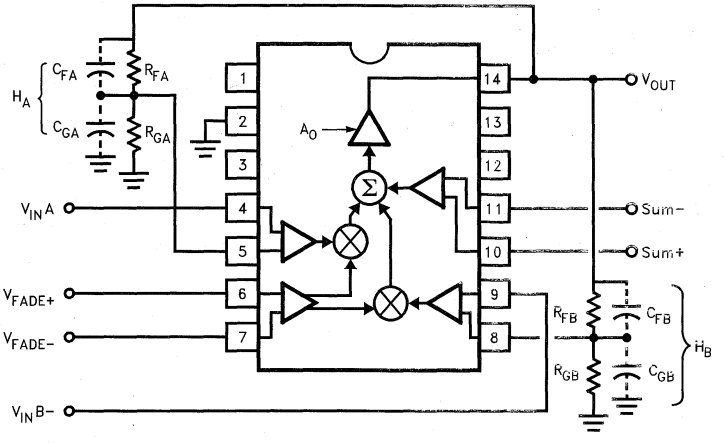
Supply Current vs Die Temperature



4453-27

Applications Information

The EL4453C is a complete two-quadrant fader/gain control with 80 MHz bandwidth. It has four sets of inputs; a differential signal input $V_{IN}A$, a differential signal input $V_{IN}B$, a differential fade-controlling input V_{FADE}, and another differential input Sum which can be used to add in a third input at full gain. This is the general connection of the EL4453C:



EL4453C
Video Fader

Applications Information — Contd.

The gain of the feedback dividers are H_A and H_B, and $0 \le H \le 1$. The transfer function of the part is

$$V_{OUT} = A_O \times [((V_{IN}A+) - H_A \times V_{OUT}) \times (1 + (V_{FADE}+) - (V_{FADE}-))/2 + ((V_{IN}B+) - H_B \times V_{OUT}) \times (1 - (V_{FADE}+) + (V_{FADE}-))/2 + (Sum+) - (Sum-))],$$

with $-1 \le (V_{FADE}+) - (V_{FADE}-) \le +1$ numerically.

A_O is the open-loop gain of the amplifier, and is about 600. The large value of A_O drives

$$((V_{IN}A+) - H_A \times V_{OUT}) \times (1 + (V_{FADE}+) - (V_{FADE}-))/2 + ((V_{IN}B+) - H_B \times V_{OUT}) \times (1 - (V_{FADE}+) + (V_{FADE}-))/2 + (Sum+) - (Sum-)) \rightarrow 0.$$

Rearranging and substituting

$$V_{OUT} = \frac{F \times V_{IN}A + \overline{F} \times V_{IN}B + Sum}{F \times H_A + \overline{F} \times H_B}$$

Where $F = (1 + (V_{FADE}+) - (V_{FADE}-))/2$,
$\overline{F} = (1 - (V_{FADE}+) + (V_{FADE}-))/2$, and
$Sum = (Sum+) - (Sum-)$

In the above equations, F represents the fade amount, with $F = 1$ giving 100% gain on $V_{IN}A$ but 0% for $V_{IN}B$; $F = 0$ giving 0% gain for $V_{IN}A$ but 100% to $V_{IN}B$. $\overline{F}$ is $1 - F$, the complement of the fade gain. When $F = 1$,

$$V_{OUT} = \frac{V_{IN}A + Sum}{H_A}$$

and the amplifier passes $V_{IN}A$ and Sum with a gain of $1/H_A$. Similarly, for $F = 0$

$$V_{OUT} = \frac{V_{IN}B + Sum}{H_B}$$

and the gains vary linearly between fade extremes.

The EL4453C is stable for a direct connection between V_{OUT} and $V_{IN}A-$ or $V_{IN}B-$, yielding a gain of +1. The feedback divider may be used for higher output gain, although with the traditional loss of bandwidth. It is important to keep the feedback dividers' impedances low so that stray capacitance does not diminish the feedback loop's phase margin. The pole caused by the parallel impedance of the feedback resistors and stray capacitance should be at least 150 MHz; typical strays of 3 pF thus require a feedback impedance of 360Ω or less. Alternatively, a small capacitor across R_F can be used to create more of a frequency-compensated divider. The value of the capacitor should scale with the parasitic capacitance at the FB input. It is also practical to place small capacitors across both the feedback resistors (whose values maintain the desired gain) to swamp out parasitics. For instance, two 10 pF capacitors across equal divider resistors for a gain of two will dominate parasitic effects and allow a higher divider resistance. Either input channel can be set up for inverting gain using traditional feedback resistor connections.

At 100% gain, an input stage operates just like an op-amp's input, and the gain error is very low, around −0.2%. Furthermore, nonlinearities are vastly improved since the gain core sees only small error signals, not full inputs. Unfortunately, distortions increase at lower fade gains for a given input channel.

The Sum pins can be used to inject an additional input signal, but it is not as linear as the V_{IN} paths. The gain error is also not as good as the main inputs, being about 1%. Both sum pins should be grounded if they are not to be used.

Fade-Control Characteristics

The quantity V_{FADE} in the above equations is bounded as $-1 \leq V_{FADE} \leq 1$, even though the externally applied voltages often exceed this range. Actually, the gain transfer function around $-1V$ and $+1V$ is "soft", that is, the gain does not clip abruptly below the 0%-V_{FADE} voltage or above the 100%-V_{FADE} level. An overdrive of 0.3V must be applied to V_{FADE} to obtain truly 0% or 100%. Because the 0% = or 100%-V_{FADE} levels cannot be precisely determined, they are extrapolated from two points measured inside the slope of the gain transfer curve. Generally, an applied V_{FADE} range of $-1.5V$ to $+1.5V$ will assure the full span of numerical $-1 \leq V_{FADE} \leq 1$ and $0 \leq F \leq 1$.

The fade control has a small-signal bandwidth equal to the V_{IN} channel bandwidth, and overload recovery resolves in about 20 ns.

Input Connections

The input transistors can be driven from resistive and capacitive sources, but are capable of oscillation when presented with an inductive input. It takes about 80 nH of series inductance to make the inputs actually oscillate, equivalent to four inches of unshielded wiring or about six inches of unterminated input transmission line. The oscillation has a characteristic frequency of 500 MHz. Often placing one's finger (via a metal probe) or an oscilloscope probe on the input will kill the oscillation. Normal high frequency construction obviates any such problems, where the input source is reasonably close to the fader input. If this is not possible, one can insert series resistors of around 51Ω to de-Q the inputs.

Signal Amplitudes

Signal input common-mode voltage must be between (V−) + 2.5V and (V+) − 2.5V to ensure linearity. Additionally, the differential voltage on any input stage must be limited to ±6V to prevent damage. The differential signal range is ±2V in the EL4453C. The input range is substantially constant with temperature.

The Ground Pin

The ground pin draws only 6 μA maximum DC current, and may be biased anywhere between (V−) +2.5V and (V+) − 3.5V. The ground pin is connected to the IC's substrate and frequency compensation components. It serves as a shield within the IC and enhances input stage CMRR and channel-to-channel isolation over frequency, and if connected to a potential other than ground, it must be bypassed.

Power Supplies

The EL4453C works well on any supplies from ±3V to ±15V. The supplies may be of different voltages as long as the requirements of the GND pin are observed (see the Ground Pin section for a discussion). The supplies should be bypassed close to the device with short leads. 4.7 μF tantalum capacitors are very good, and no smaller bypasses need be placed in parallel. Capacitors as small as 0.01 μF can be used if small load currents flow.

Singe-polarity supplies, such as +12V with +5V can be used, where the ground pin is connected to +5V and V− to ground. The inputs and outputs will have to have their levels shifted above ground to accommodate the lack of negative supply.

The dissipation of the fader increases with power supply voltage, and this must be compatible with the package chosen. This is a close estimate for the dissipation of a circuit:

$$P_D = 2 \times V_S, \max \times V_S + (V_S - V_O) \times V_O / R_{PAR}$$

where I_S, max is the maximum supply current
V_S is the ± supply voltage (assumed equal)
V_O is the output voltage
R_{PAR} is the parallel of all resistors loading the output

EL4453C
Video Fader

Power Supplies — Contd.

For instance, the EL4453C draws a maximum of 21 mA. With light loading, $R_{PAR} \rightarrow \infty$ and the dissipation with ±5V supplies is 210 mW. The maximum supply voltage that the device can run on for a given P_D and the other parameters is

$$V_S, max = (P_D + V_O^2/R_{PAR})/(2I_S + V_O/R_{PAR})$$

The maximum dissipation a package can offer is

$$P_D, max = (T_D, max - T_A, max)/\theta_{JA}$$

where T_D, max is the maximum die temperature, 150°C for reliability, less to retain optimum electrical performace

T_A, max is the ambient temperature, 70°C for commercial and 85°C for industrial range

θ_{JA} is the thermal resistance of the mounted package, obtained from datasheet dissipation curves

The more difficult case is the SO-14 package. With a maximum die temperature of 150°C and a maximum ambient temperature of 70°C, the 80°C temperature rise and package thermal resistance of 110°/W gives a dissipation of 636 mW at 85 °C. This allows ±15V operation over the commercial temperature range, but higher ambient temperature or output loading may require lower supply voltages.

Output Loading

The output stage of the EL4453C is very powerful. It typically can source 80 mA and sink 120 mA. Of course, this is too much current to sustain and the part will eventually be destroyed by excessive dissipation or by metal traces on the die opening. The metal traces are completely reliable while delivering the 30 mA continuous output given in the Absolute Maximum Ratings table in this data sheet, or higher purely transient currents.

Gain changes only 0.2% from no load to 100Ω load. Heavy resistive loading will degrade frequency response and video distortion for loads < 100Ω.

Capacitive loads will cause peaking in the frequency response. If capacitive loads must be driven, a small-valued series resistor can be used to isolate it. 12Ω to 51Ω should suffice. A 22Ω series resistor will limit peaking to 2.5 dB with even a 220 pF load.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4584C
Horizontal Genlock, 4 F_{SC}

Features

- 36 MHz, general purpose PLL
- 4 F_{SC} based timing (use the EL4585 for 8 F_{SC})
- Compatible w/EL4583 Sync Separator
- VCXO, Xtal, or LC tank oscillator
- <2 ns jitter (VCXO)
- User controlled PLL capture and lock
- Compatible with NTSC and PAL TV formats
- 8 pre-programmed TV scan rate clock divisors
- Selectable external divide for custom ratios
- Single 5V, low current operation

Applications

- Pixel Clock regeneration
- Video compression engine (MPEG) clock generator
- Video capture or digitization
- PIP (Picture in Picture) timing generator
- Text or graphics overlay timing

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4584CN	-40°C to +85°C	16-Pin DIP	MDP0031
EL4584CS	-40°C to +85°C	16-Lead SO	MDP0027

For 6Fsc and 8Fsc clock frequencies, see EL4585 datasheet.

General Description

The EL4584C is a PLL (Phase Lock Loop) sub system, designed for video applications but also suitable for general purpose use up to 36 MHz. In a video application this device generates a TTL/CMOS compatible Pixel Clock (Clk Out) which is a multiple of the TV Horizontal scan rate, and phase locked to it.

The reference signal is a horizontal sync signal, TTL/CMOS format, which can be easily derived from an analog composite video signal with the EL4583 Sync Separator. An input signal to "coast" is provided for applications were periodic disturbances are present in the reference video timing such as VTR head switching. The Lock detector output indicates correct lock.

The divider ratio is four ratios for NTSC and four similar ratios for the PAL video timing standards, by external selection of three control pins. These four ratios have been selected for common video applications including 4 F_{SC}, 3 F_{SC}, 13.5 MHz (CCIR 601 format) and square picture elements used in some workstation graphics. To generate 8 F_{SC}, 6 F_{SC}, 27 MHz (CCIR 601 format) etc. use the EL4585, which includes an additional divide by 2 stage.

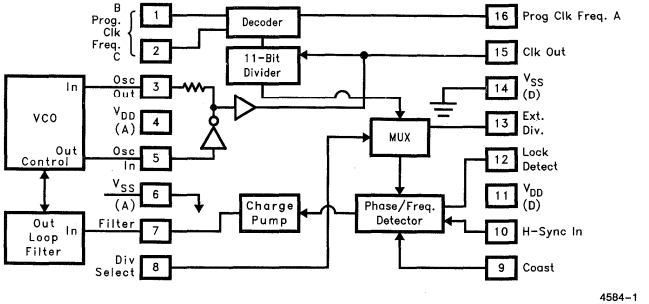
For applications where these frequencies are inappropriate or for general purpose PLL applications the internal divider can be bypassed and an external divider chain used.

FREQUENCIES and DIVISORS

Function	3Fsc	CCIR 601	Square	4Fsc
Divisor	851	864	944	1135
PAL Fosc (MHz)	13.301	13.5	14.75	17.734
Divisor	682	858	780	910
NTSC Fosc (MHz)	10.738	13.5	12.273	14.318

CCIR 601 Divisors yield 720 pixels in the portion of each line for NTSC and PAL.
Square pixels format gives 640 pixels for NTSC and 768 pixels for PAL in the active portion.
3Fsc numbers do not yield integer divisors.

Connection Diagram



EL4584C
Horizontal Genlock, 4 F_{SC}

Absolute Maximum Ratings (T_A = 25°C)

V_{CC} Supply	7V	Operating Junction Temp	125°C
Storage Temperature	−65°C to +150°C	Power Dissipation	400 mW
Lead Temperature	260°C	Oscillator Frequency	36 MHz
Pin Voltages	−0.5V to V_{CC}+0.5V		
Operating Ambient Temperature Range	−40°C to +85°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics (V_{DD} = 5V, T_A = 25°C unless otherwise noted)

Parameter	Conditions	Temp	Min	Typ	Max	Test Level	Units
I_{DD}	V_{DD} = 5V (Note 1)	25°C		2	4	I	mA
V_{IL} Input Low Voltage		25°C			1.5	I	V
V_{IH} Input High Voltage		25°C	3.5			I	V
I_{IL} Input Low Current	All inputs except COAST, V_{IN} = 1.5V	25°C	−100			I	nA
I_{IH} Input High Current	All inputs except COAST, V_{IN} = 3.5V	25°C			100	I	nA
I_{IL} Input Low Current	COAST pin, V_{IN} = 1.5V	25°C	100	60		I	μA
I_{IH} Input High Current	COAST pin, V_{IN} = 3.5V	25°C		60	100	I	μA
V_{OL} Output Low Voltage	Lock Det, I_{OL} = 1.6mA	25°C			0.4	I	V
V_{OH} Output High Voltage	Lock Det, I_{OH} = −1.6mA	25°C	2.4			I	V
V_{OL} Output Low Voltage	CLK, I_{OL} = 3.2mA	25°C			0.4	I	V
V_{OH} Output High Voltage	CLK, I_{OH} = −3.2mA	25°C	2.4			I	V
V_{OL} Output Low Voltage	OSC Out, I_{OL} = 200μA	25°C			0.4	I	V
V_{OH} Output High Voltage	OSC Out, I_{OH} = −200μA	25°C	2.4			I	V
I_{OL} Output Low Current	Filter Out, V_{OUT} = 2.5V	25°C	200	300		I	μA
I_{OH} Output High Current	Filter Out, V_{OUT} = 2.5V	25°C		−300	−200	I	μA
I_{OL}/I_{OH} Current Ratio	Filter Out, V_{OUT} = 2.5V	25°C	1.05	1.0	0.95	I	
I_{LEAK} Filter Out	Coast Mode, $V_{DD} > V_{OUT} > 0V$	25°C	−100	±1	100	I	nA

Note 1: All inputs to 0V, COAST floating.

AC Electrical Characteristics (V_{DD} = 5V, T_A = 25°C unless otherwise noted)

Parameter	Conditions	Temp	Min	Typ	Max	Test Level	Units
VCO Gain @ 20 MHz	Test Circuit 1	25°C		15.5		V	dB
H-sync S/N Ratio	V_{DD} = 5V (Note 2)	25°C	35			V	dB
Jitter	VCXO Oscillator	25°C		1		V	ns
Jitter	LC Oscillator (Typ)	25°C		10		V	ns

Note 2: Noisy video signal input to EL4583C, H-sync input to EL4584C. Test for positive signal lock.

Pin Description

Pin No.	Pin Name	Function
16,1,2	Prog A,B,C	Digital inputs to select ÷ N value for internal counter. See table below for values.
3	Osc/VCO Out	Output of internal inverter/oscillator. Connect to external crystal or LC tank VCO circuit.
4	V_{DD} (A)	Analog positive supply for oscillator, PLL circuits.
5	Osc/VCO In	Input from external VCO.
6	V_{SS} (A)	Analog ground for oscillator, PLL circuits.
7	Filter	Charge pump output. If the H-sync phase is leading or H-sync frequency > CLK ÷ N, current is pumped into the filter capacitor to increase VCO frequency. If H-sync phase is lagging or frequency < CLK ÷ N, current is pumped out of the filter capacitor to decrease VCO frequency. During coast mode or when locked, filter goes to a high impedance state.
8	Div Select	Divide select input. When high, the internal divider is enabled and EXT DIV becomes a test pin, outputting CLK ÷ N. When low, the internal divider is disabled and EXT DIV is an input from an external ÷ N.
9	Coast	Tri-state logic input. Low(<⅓*V_{CC}) = normal mode, Hi Z(or ⅓ to ⅔*V_{CC}) = fast lock mode, High(>⅔*V_{CC}) = coast mode.
10	H-sync In	Horizontal sync pulse (CMOS level) input.
11	V_{DD} (D)	Positive supply for digital, I/O circuits.
12	Lock Det	Lock Detect output. Low level when PLL is locked. Pulses high when out of lock.
13	Ext Div	External Divide input when DIV SEL is low, internal ÷N output when DIV SEL is high.
14	V_{SS} (D)	Ground for digital, I/O circuits.
15	CLK Out	Buffered output of the VCO.

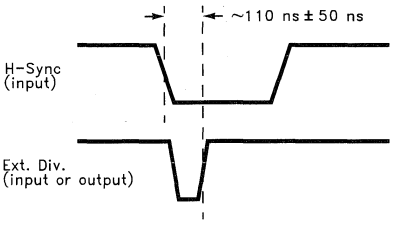
VCO Divisors Table 1

Prog A Pin 16	Prog B Pin 1	Prog C Pin 2	Div Value N
0	0	0	851
0	0	1	864
0	1	0	944
0	1	1	1135
1	0	0	682
1	0	1	858
1	1	0	780
1	1	1	910

EL4584C
Horizontal Genlock, 4 F_{SC}

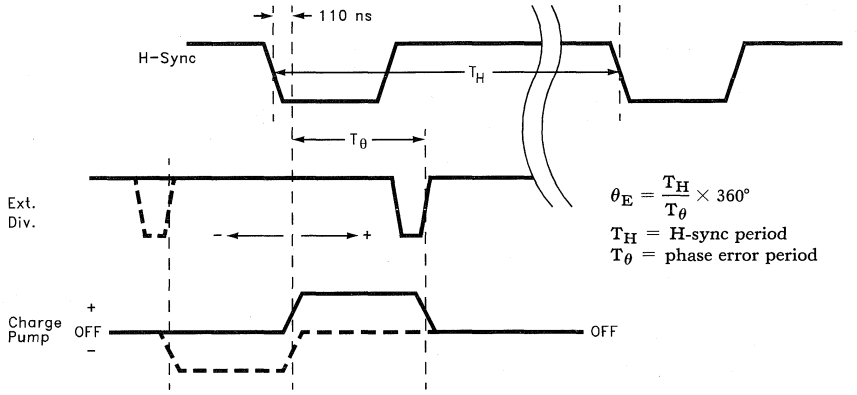
Timing Diagrams

PLL Locked Condition (Phase Error = 0)



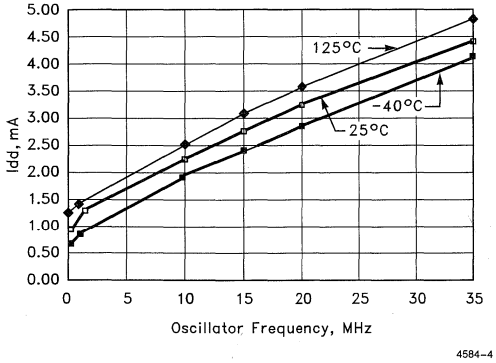
Falling edge of H-sync + 110 ns locks to rising edge of Ext Div signal.

Out of Lock Condition

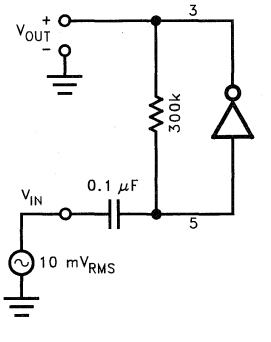


Typical Performance Curves

Idd vs Fosc

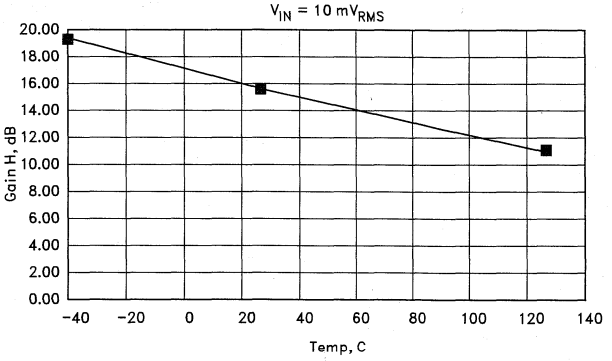


Test Circuit 1



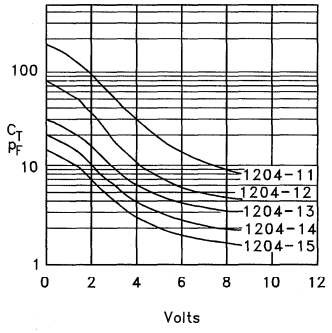
Typical Performance Curves — Contd.

4584 OSC Gain @ 20 MHz vs Temp



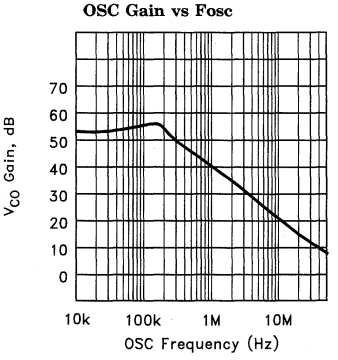
4584-6

Typical Varactor



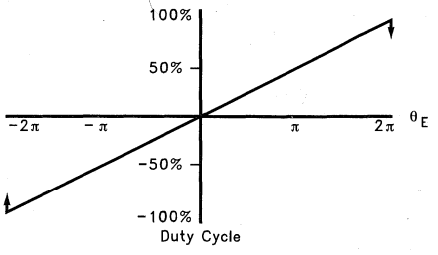
4584-7

OSC Gain vs Fosc



4584-8

Charge Pump Duty Cycle vs θ_E



4584-9

EL4584C
Horizontal Genlock, 4 F_{SC}

Description Of Operation

The horizontal sync signal (CMOS level, falling leading edge) is input to H-sync input (pin 10). This signal is delayed about 110 ns, the falling edge of which becomes the reference to which the clock output will be locked. (See timing diagrams.) The clock is generated by the signal on pin 5, OSC in. There are 2 general types of VCO that can be used with the EL4584C, LC and crystal controlled. Additionally, each type can be either built up using discrete components, including a varactor as the frequency controlling element, or complete, self contained modules can be purchased with everything inside a metal can. The modules are very forgiving of PCB layout, but cost more than discrete solutions. The VCO or VCXO is used to generate the clock. An LC tank resonator has greater "pull" than a crystal controlled circuit, but will also be more likely to drift over time, and thus will generate more jitter. The "pullability" of the circuit refers to the ability to "pull" the frequency of oscillation away from its center frequency by modulating the voltage on the control pin of a VCO module or varactor, and is a function of the slope and range of the capacitance-voltage curve of the varactor or VCO module used. The VCO signal is sent to a divide by N counter, and to the CLK out pin. The divisor N is determined by the state of pins 1,2, and 16 and is described in table 1 above. The divided signal is sent, along with the delayed H-sync input, to the phase/frequency detector, which compares the two signals for phase and frequency differences. Any phase difference is converted to a current at the charge pump output FILTER (pin 7). A VCO with positive frequency deviation with control voltage must be used. Varactors have negative capacitance slope with voltage, resulting in positive frequency deviation with control voltage for the oscillators in figures 10 and 11 below.

VCO

The VCO should be tuned so its frequency of oscillation is very close to the required clock output frequency when the voltage on the varactor is 2.5 volts. VCXO and VCO modules are already tuned to the desired frequency, so this step is not necessary if using one of these units. The range of the FILTER (pin 7) is 0 to 5 volts and it can source or sink a maximum of about 300 μA, so all frequency control must be accomplished with variable capacitance from the varactor within this range. Crystal oscillators are more stable than LC oscillators, which translates into lower jitter, but LC oscillators can be pulled from their mid-point values further, resulting in a greater capture and locking range. If the incoming horizontal sync signal is known to be very stable, then a crystal oscillator circuit can be used. If the h-sync signal experiences frequency variations of greater than about 300 ppm, an LC oscillator should be considered, as crystal oscillators are very difficult to pull this far. When H-SYNC input frequency is greater than CLK frequency $\div$ N, filter output (pin 7) sources current into the filter capacitor, increasing the voltage across the varactor, which lowers its capacitance, thus tending to increase VCO frequency. Conversely, filter output pulls current from the filter capacitor when H-SYNC frequency is less than CLK $\div$ N, forcing the VCO frequency lower.

Loop Filter

The loop filter controls how fast the VCO will respond to a change in filter output stimulus. Its components should be chosen so that fast lock can be achieved, yet with a minimum of VCO "hunting", preferably in one to two oscillations of filter output, assuming the VCO frequency starts within capture range. If the filter is underdamped, the VCO will over and under-shoot the desired operating point many times before a stable lock takes place. It is possible to under-damp the filter so much that the loop itself oscillates, and VCO lock is never achieved. If the filter is over-damped, the VCO response time will be excessive and many cycles will be required for a lock condition. Over-damping is also characterized by an easily unlocked system because the filter can't respond fast enough to perturbations in VCO frequency. A severely over damped system will seem to endlessly oscillate, like a very large mass at the end of a long pendulum. Due to parasitic effects of PCB traces and component variables, it will take some trial and error experimentation to determine the best values to use for any given situation. Use the component tables as a starting point, but be aware that deviation from these values is not out of the ordinary.

Description of Operation — Contd.

External Divide

DIV SEL (pin 8) controls the use of the internal divider. When high, the internal divider is enabled and EXT DIV (pin 13) outputs the CLK out divided by N. This is the signal to which the horizontal sync input will lock. When divide select is low, the internal divider output is disabled, and external divide becomes an input from an external divider, so that a divisor other than one of the 8 pre-programmed internal divisors can be used.

Normal Mode

Normal mode is enabled by pulling COAST (pin 9) low (below $\frac{1}{3}*V_{CC}$). If H-sync and CLK ÷ N have any phase or frequency difference, an error signal is generated and sent to the charge pump. The charge pump will either force current into or out of the filter capacitor in an attempt to modulate the VCO frequency. Modulation will continue until the phase and frequency of CLK ÷ N exactly match the H-sync input. When the phase and frequency match (with some offset in phase that is a function of the VCO characteristics), the error signal goes to zero, lock detect no longer pulses high, and the charge pump enters a high impedance state. The clock is now locked to the H-sync input. As long as phase and frequency differences remain small, the PLL can adjust the VCO to remain locked and lock detect remains low. Once locked, the phase/frequency detector becomes a phase only detector so that missing sync pulses will not disturb the VCO output. If H-sync disappears completely, filter output goes into a high impedance state, which is functionally equivalent to coast mode.

Fast Lock Mode

Fast Lock mode is enabled by either allowing coast to float, or pulling it to mid supply (between $\frac{1}{3}$ and $\frac{2}{3}*V_{CC}$). In this mode, lock is achieved much faster than in normal mode, but the clock divisor is modified on the fly to achieve this. If the phase detector detects an error of enough magnitude, the clock is either inhibited or reset to attempt a "fast" lock of the signals. Forcing the clock to be synchronized to the H-sync input this way allows a lock in approximately 2 H-cycles, but the clock spacing will not be regular during this time. Once the near lock condition is attained, filter output should be very close to its lock-on value and placing the device into normal mode should result in a normal lock very quickly. Fast Lock mode is intended to be used where H-sync becomes irregular, until a stable signal is again obtained.

Coast Mode

Coast mode is enabled by pulling COAST (pin 9) high (above $\frac{2}{3}*V_{CC}$). In coast mode the internal phase detector is disabled and filter out remains in high impedance mode to keep filter out voltage and VCO frequency as constant a possible. VCO frequency will drift as charge leaks from the filter capacitor, and the voltage changes the VCO operating point. Coast mode is intended to be used when noise or signal degradation result in loss of horizontal sync for many cycles. The phase detector will not attempt to adjust to the resultant loss of signal so that when horizontal sync returns, sync lock can be re-established quickly. However, if much VCO drift has occurred, it may take as long to re-lock as when restarting.

Lock Detect

Lock detect (pin 12) will go low when lock is established. Any DC current path from FILTER out will skew EXT DIV relative to H-SYNC in, tending to offset or add to the 110 ns internal delay, depending on which way the extra current is flowing. This offset is called static phase error, and is always present in any PLL system. If, when the part stabilizes in a locked mode, lock detect is not low, adding or subtracting from the series resistor will change this static phase error to allow LDET to go low while in lock. The goal is to put the rising edge of EXT DIV in sync with the falling edge of H-SYNC + 110 ns. (See timing diagrams.) Increasing R_2 increases phase error, while decreasing R_2 decreases phase error. (Phase error is positive when EXT DIV lags H-SYNC.) The resistance needed will depend on VCO design or VCXO module selection.

EL4584C
Horizontal Genlock, 4 F_{SC}

Applications Information

Choosing External Components

1. To choose LC VCO components, first pick the desired operating frequency. For our example we will use 14.31818 MHz, with an H-sync frequency of 15.734 kHz.
2. Choose a reasonable inductor value (10–20μH works well). We choose 15 μH.
3. Calculate C_T needed to produce F_{OSC}.

$$F_{OSC} = \frac{1}{2\pi\sqrt{LC_T}}$$

$$C_T = \frac{1}{4\pi^2F^2L} = \frac{1}{4\pi^2(14.318e6)^2(15e-6)} = 8.2\text{ pF}$$

4. From the varactor data sheet find C_V @ 2.5V, the desired lock voltage. $C_V = 23$ pF for our SMV1204-12, for example.
5. C_2 should be about $10C_V$, so we choose $C_2 = 220$ pF for our example.
6. Calculate C_1. Since

$$C_T = \frac{C_1C_2C_V}{(C_1C_2) + (C_1C_V) + (C_2C_V)},$$

then

$$C_1 = \frac{C_2C_TC_V}{(C_2C_V) - (C_2C_T) - (C_TC_V)}.$$

For our example, $C_1 = 14$ pF. (A trim cap may be used for fine tuning.) Examples for each frequency using the internal divider follow.

Typical LC VCO

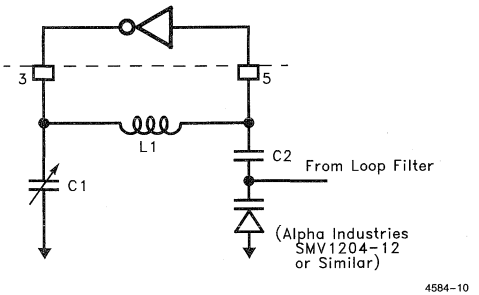


Figure 10

LC VCO Component Values (Approximate)

Frequency (MHz)	L1 (μH)	C1 (pF)	C2 (pF)
13.301	15	18	220
13.5	15	17	220
14.75	12	18	220
17.734	12	10	220
10.738	22	20	220
12.273	18	17	220
14.318	15	14	220

Note: Use shielded inductors for optimum performance.

Typical Xtal VCO

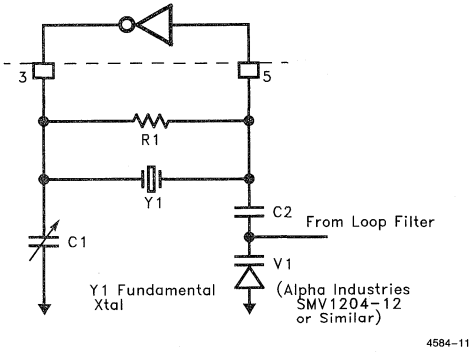


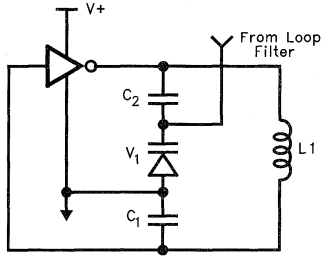
Figure 11

Xtal VCO Component Values (Approximate)

Frequency (MHz)	R1 (kΩ)	C1 (pF)	C2 (uF)
13.301	300	15	.001
13.5	300	15	.001
14.75	300	15	.001
17.734	300	15	.001
10.738	300	15	.001
12.273	300	15	.001
14.318	300	15	.001

The above oscillators are arranged as Colpitts oscillators, and the structure is redrawn here to emphasize the split capacitance used in a Colpitts oscillator. It should be noted that this oscillator configuration is just one of literally hundreds possible, and the configuration shown here does not necessarily represent the best solution for all applications. Crystal manufacturers are very informative sources on the design and use of oscillators in a wide variety of applications, and the reader is encouraged to become familiar with them.

Colpitts Oscillator



4584-12

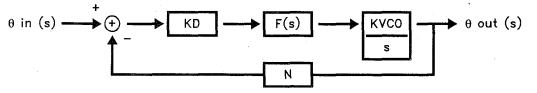
C_1 is to adjust the center frequency, C_2 DC isolates the control from the oscillator, and V1 is the primary control device. C_2 should be much larger than C_V so that V_1 has maximum modulation capability. The frequency of oscillation is given by:

$$F = \frac{1}{2\pi\sqrt{LC_T}}$$

$$C_T = \frac{C_1C_2C_V}{(C_1C_2) + (C_1C_V) + (C_2C_V)}$$

Choosing Loop Filter Components

The PLL, VCO, and loop filter can be described as:



4584-13

Where:

K_d = phase detector gain in A/rad

F(s) = loop filter impedance in V/A

K_{VCO} = VCO gain in rad/s/V

N = internal or external divisor

It can be shown that for the loop filter shown below:

$$C_3 = \frac{K_dK_{VCO}}{N\omega_n^2}, C_4 = \frac{C_3}{10}, R_3 = \frac{2N\zeta\omega_n}{K_dK_{VCO}}$$

Where ω_n = loop filter bandwidth, and ζ = loop filter damping factor.

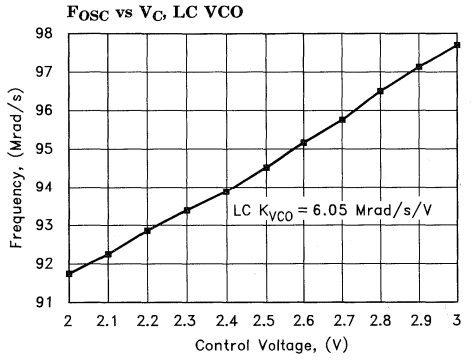
1. K_d = 300 μA/2πrad = 4.77e-5A/rad for the EL4584C.
2. The loop bandwidth should be about H-sync frequency/20, and the damping ratio should be 1 for optimum performance. For our example, ω_n = 15.734 kHz/20 = 787 Hz ≈ 5000 rad/S.
3. N = 910 from table 1.

$$N = \frac{\text{VCOfrequency}}{\text{H-SYNCfrequency}} = \frac{14.31818M}{15.73426k} = 910$$

4. K_{VCO} represents how much the VCO frequency changes for each volt applied at the control pin. It is assumed (but probably isn't) linear about the lock point (2.5V). Its value depends on the VCO configuration and the varactor

EL4584C
Horizontal Genlock, 4 F_{SC}

transfer function $C_v = F(V_C)$, where V_C is the reverse bias control voltage, and C_V is varactor capacitance. Since $F(V_C)$ is nonlinear, it is probably best to build the VCO and measure K_{VCO} about 2.5V. The results of one such measurement are shown below. The slope of the curve is determined by linear regression techniques and equals K_{VCO}. For our example, K_{VCO} = 6.05 Mrad/S/V.



4584-14

5. Now we can solve for C_3, C_4, and R_3.

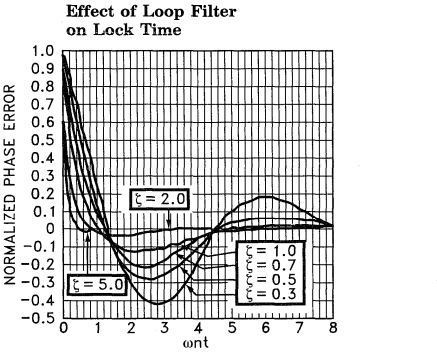
$$C_3 = \frac{K_d K_{VCO}}{N\omega^2_n} = \frac{(4.77e-5)(6.05e6)}{(910)(5000)^2} = 0.01\ \mu F$$

$$C_4 = \frac{C_3}{10} = 0.001\ \mu F$$

$$R_3 = \frac{2N\zeta\omega_n}{K_d K_{VCO}} = \frac{(2)(910)(1)(5000)}{(4.77e-5)(6.05e6)} = 31.5\ k\Omega$$

We choose R_3 = 30 kΩ for convenience.

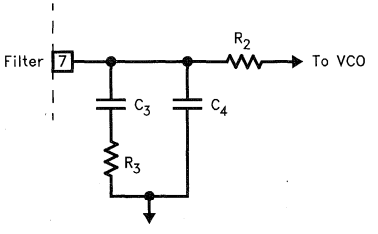
6. Notice R_2 has little effect on the loop filter design. R_2 should be large, around 100k, and can be adjusted to compensate for any static phase error T_θ at lock, but if made too large, will slow loop response. If R_2 is made smaller, T_θ (see timing diagrams) increases, and if R_2 increases, T_θ decreases. For LDET to be low at lock, $|T_\theta| < 50$ ns. C_4 is used mainly to attenuate high frequency noise from the charge pump. The effect these components have on time to lock is illustrated below.



4584-15

Let $T = R_3C_3$. As T increases, damping increases, but so does lock time. Decreasing T decreases damping and speeds up loop response, but increases overshoot and thus increases the number of hunting oscillations before lock. Critical damping ($\zeta = 1$) occurs at minimum lock time. Because decreased damping also decreases loop stability, it is sometimes desirable to design slightly overdamped ($\zeta > 1$), trading lock time for increased stability.

Typical Loop Filter



4584-16

LC Loop Filter Components (Approximate)

Frequency (MHz)	R2 (kΩ)	R3 (kΩ)	C3 (μF)	C4 (μF)
13.301	100	30	0.01	0.001
13.5	100	30	0.01	0.001
14.75	100	33	0.01	0.001
17.734	100	39	0.01	0.001
10.738	100	22	0.01	0.001
12.273	100	27	0.01	0.001
14.318	100	30	0.01	0.001

Xtal Loop Filter Components (Approximate)

Frequency (MHz)	R2 (kΩ)	R3 (MΩ)	C3 (pF)	C4 (pF)
13.301	100	4.3	68	6.8
13.5	100	4.3	68	6.8
14.75	100	4.3	68	6.8
17.734	100	4.3	68	6.8
10.738	100	4.3	68	6.8
12.273	100	4.3	68	6.8
14.318	100	4.3	68	6.8

PCB Layout Considerations

It is highly recommended that power and ground planes be used in layout. The oscillator and filter sections constitute a feedback loop and thus care must be taken to avoid any feedback signal influencing the oscillator except at the control input. The entire oscillator/filter section should be surrounded by copper ground to prevent unwanted influences from nearby signals. Use separate paths for analog and digital supplies, keeping the analog (oscillator section) as short and free from spurious signals as possible. Careful attention must be paid to correct bypassing. Keep lead lengths short and place bypass caps as close to the supply pins as possible. If laying out a PCB to use discrete components for the VCO section, care must be taken to avoid parasitic capacitance at the OSC pins 3 and 5, and FILTER out (pin 7). Remove ground and power plane copper above and below these traces to avoid making a capacitive connection to them. It is also recommended to enclose the oscillator section within a shielded cage to reduce external influences on the VCO, as they tend to be very sensitive to "hand-waving" influences, the LC variety being more sensitive than crystal controlled oscillators. In general, the higher the operating frequency, the more important these considerations are. Self contained VCXO or VCO modules are already mounted in a shielding cage and therefore do not require as much consideration in layout. Many crystal manufacturers publish informative literature regarding use and layout of oscillators which should be helpful.

Component Sources

Inductors

- Dale Electronics
  E. Highway 50
  PO Box 180
  Yankton, SD 57078-0180
  (605) 665-9301

Crystals, VCXO, VCO Modules

- Connor-Winfield
  2111 Comprehensive Drive
  Aurora, IL 60606
  (708) 851-4722

- Piezo Systems
  100 K Street
  PO Box 619
  Carlisle, PA 17013
  (717) 249-2151

EL4584C
Horizontal Genlock, 4 F_{SC}

Component Sources — Contd.

- Reeves-Hoffman
  400 West North Street
  Carlisle, PA 17013
  (717) 243-5929

- SaRonix
  151 Laura Lane
  Palo Alto, CA 94043
  (415) 856-6900

- Standard Crystal
  9940 Baldwin Place
  El Monte, CA 91731
  (818) 443-2121

Varactors

- Alpha Industries
  20 Sylvan Road
  Woburn, MA 01801
  (617) 935-5150

- Motorola Semiconductor Products
  2100 E. Elliot
  Tempe, AZ 85284
  (602) 244-6900

Note: These sources are provided for information purposes only. No endorsement of these companies is implied by this listing.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4585C
Horizontal Genlock, 8 F_{SC}

Features

- 36 MHz, general purpose PLL
- 8 F_{SC} timing. (Use the EL4584 for 4 F_{SC})
- Compatible with EL4583C Sync Separator
- VCXO, Xtal, or LC tank oscillator
- <2nS jitter (VCXO)
- User-controlled PLL capture and lock
- Compatible with NTSC and PAL TV formats
- 8 pre-programmed popular TV scan rate clock divisors
- Single 5V, low current operation

Applications

- Pixel Clock regeneration
- Video compression engine (MPEG) clock generator
- Video Capture or digitization
- PIP (Picture In Picture) timing generator
- Text or Graphics overlay timing

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4585CN	−40°C to +85°C	16-Pin DIP	MDP0031
EL4585CS	−40°C to +85°C	16-Lead SO	MDP0027

For 3Fsc and 4Fsc clock frequency operation, see EL4584 datasheet.

General Description

The EL4585C is a PLL (Phase Lock Loop) sub system, designed for video applications, but also suitable for general purpose use up to 36 MHz. In a video application this device generates a TTL/CMOS compatible Pixel Clock (Clk Out) which is a multiple of the TV Horizontal scan rate, and phase locked to it.

The reference signal is a horizontal sync signal, TTL/CMOS format, which can be easily derived from an analog composite video signal with the EL4583 Sync Separator. An input signal to "coast" is provided for applications where periodic disturbances are present in the reference video timing such as VTR head switching. The Lock detector output indicates correct lock.

The divider ratio is four ratios for NTSC and four similar ratios for the PAL video timing standards, by external selection of three control pins. These four ratios have been selected for common video applications including 8 F_{SC}, 6 F_{SC}, 27 MHz (CCIR 601 format) and square picture elements used in some workstation graphics. To generate 4 F_{SC}, 3 F_{SC}, 13.5 MHz (CCIR 601 format) etc., use the EL4584, which does not have the additional divide by 2 stage of the EL4585.

For applications where these frequencies are inappropriate or for general purpose PLL applications the internal divider can be by passed and an external divider chain used.

FREQUENCIES and DIVISORS

Function	6Fsc	CCIR 601	Square	8Fsc
Divisor*	851	864	944	1135
PAL Fosc (MHz)	26.602	27.0	29.5	35.468
Divisor*	682	858	780	910
NTSC Fosc (MHz)	21.476	27.0	24.546	28.636

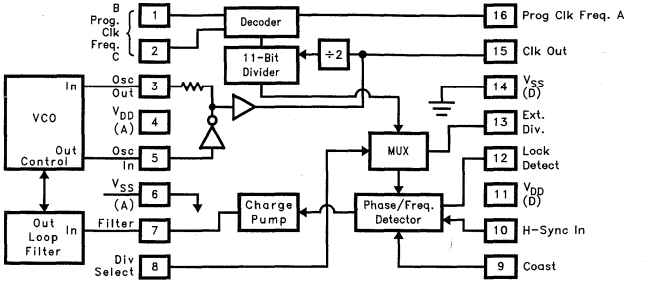
CCIR 601 divisors yield 720 pixels in the active portion of each line for NTSC and PAL.

Square pixels format gives 640 pixels for NTSC and 768 pixels for PAL.

6Fsc frequencies do not yield integer divisors.

*Divisor does not include ÷ 2 block.

Connection Diagram



4585-1

EL4585C
Horizontal Genlock, 8 F_{SC}

Absolute Maximum Ratings (T_A = 25°C)

V_{CC} Supply	7V	Operating Junction Temp	125°C
Storage Temperature	−65°C to +150°C	Power Dissipation	400mW
Lead Temperature	260°C	Oscillator Frequency	36MHz
Pin Voltages	−0.5V to V_{CC} +0.5V		
Operating Ambient Temperature Range	−40°C to +85°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics (V_{DD} = 5V, T_A = 25°C unless otherwise noted)

Parameter	Conditions	Temp	Min	Typ	Max	Test Level	Units
I_{DD}	V_{DD} = 5V (Note 1)	25°C		2	4	I	mA
V_{IL} Input Low Voltage		25°C			1.5	I	V
V_{IH} Input High Voltage		25°C	3.5			I	V
I_{IL} Input Low Current	All inputs except COAST, V_{in} = 1.5V	25°C	−100			I	nA
I_{IH} Input High Current	All inputs except COAST, V_{in} = 3.5V	25°C			100	I	nA
I_{IL} Input Low Current	COAST pin, V_{in} = 1.5V	25°C	−100	−60		I	µA
I_{IH} Input High Current	COAST pin, V_{in} = 3.5V	25°C		60	100	I	µA
V_{OL} Output Low Voltage	Lock Det, I_{OL} = 1.6mA	25°C			0.4	I	V
V_{OH} Output High Voltage	Lock Det, I_{OH} = −1.6mA	25°C	2.4			I	V
V_{OL} Output Low Voltage	CLK, I_{OL} = 3.2mA	25°C			0.4	I	V
V_{OH} Output High Voltage	CLK, I_{OH} = −3.2mA	25°C	2.4			I	V
V_{OL} Output Low Voltage	OSC Out, I_{OL} = 200µA	25°C			0.4	I	V
V_{OH} Output High Voltage	OSC Out, I_{OH} = −200µA	25°C	2.4			I	V
I_{OL} Output Low Current	Filter Out, V_{OUT} = 2.5V	25°C	200	300		I	µA
I_{OH} Output High Current	Filter Out, V_{OUT} = 2.5V	25°C		−300	−200	I	µA
I_{OL}/I_{OH} Current Ratio	Filter Out, V_{OUT} = 2.5V	25°C	1.05	1.0	0.95	I	
I_{LEAK} Filter Out	Coast Mode, $V_{DD} > V_{OUT} > 0V$	25°C	−100	±1	100	I	nA

Note 1: All inputs to 0V, COAST floating.

AC Electrical Characteristics (V_{DD} = 5V, T_A = 25°C unless otherwise noted)

Parameter	Conditions	Temp	Min	Typ	Max	Test Level	Units
VCO Gain @ 20 MHz	Test circuit 1	25°C		15.5		V	dB
H-sync S/N Ratio	V_{DD} = 5V (Note 2)	25°C	35			V	dB
Jitter	VCXO Oscillator	25°C		1		V	ns
Jitter	LC Oscillator (Typ)	25°C		10		V	ns

Note 2: Noisy video signal input to EL4583C, H-sync input to EL4585C. Test for positive signal lock.

Pin Description

Pin No.	Pin Name	Function
16,1,2	Prog A,B,C	Digital inputs to select ÷ N value for internal counter. See table below for values.
3	Osc/VCO Out	Output of internal inverter/oscillator. Connect to external crystal or LC tank VCO circuit.
4	V_{DD} (A)	Analog positive supply for oscillator, PLL circuits.
5	Osc/VCO In	Input from external VCO.
6	V_{SS} (A)	Analog ground for oscillator, PLL circuits.
7	Filter	Charge pump output. If the H-sync phase is leading or H-sync frequency > CLK÷2N, current is pumped into the filter capacitor to increase VCO frequency. If H-sync phase is lagging or frequency < CLK÷2N, current is pumped out of the filter capacitor to decrease VCO frequency. During coast mode or when locked, filter goes to a high impedance state.
8	Div Select	Divide select input. When high, the internal divider is enabled and EXT DIV becomes a test pin, outputting CLK÷2N. When low, the internal divider is disabled and EXT DIV is an input from an external ÷N.
9	Coast	Tri-state logic input. Low(< $\frac{1}{3}$*V_{CC}) = normal mode, Hi Z(or $\frac{1}{3}$ to $\frac{2}{3}$*V_{CC}) = fast lock mode, High(> $\frac{2}{3}$*V_{CC}) = coast mode.
10	H-sync In	Horizontal sync pulse (CMOS level) input.
11	V_{DD} (D)	Positive supply for digital, I/O circuits.
12	Lock Det	Lock Detect output. Low level when PLL is locked. Pulses high when out of lock.
13	Ext Div	External Divide input when DIV SEL is low, internal ÷ 2N output when DIV SEL is high.
14	V_{SS} (D)	Ground for digital, I/O circuits.
15	CLK Out	Buffered output of the VCO.

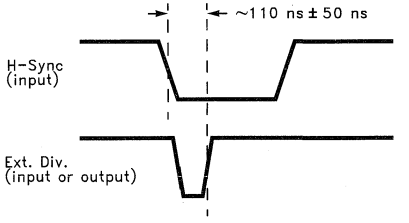
Table 5: VCO Divisors

Prog A Pin 16	Prog B Pin 1	Prog C Pin 2	Div Value N
0	0	0	851
0	0	1	864
0	1	0	944
0	1	1	1135
1	0	0	682
1	0	1	858
1	1	0	780
1	1	1	910

EL4585C
Horizontal Genlock, 8 F_{SC}

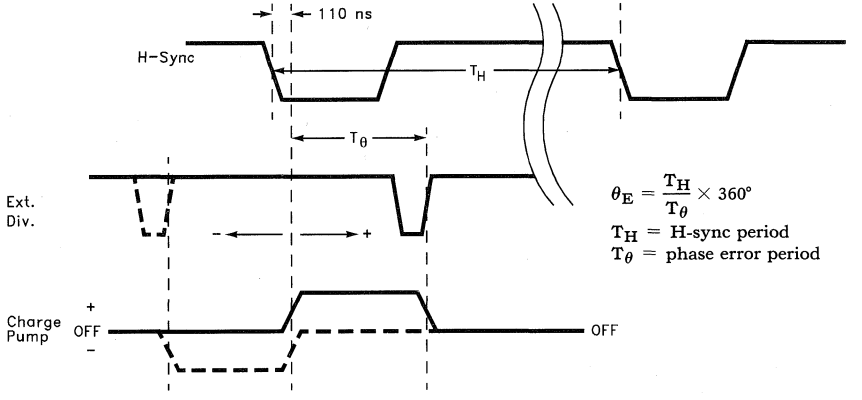
Timing Diagrams

PLL Locked Condition (Phase Error = 0)



4585-2

Out of Lock Condition



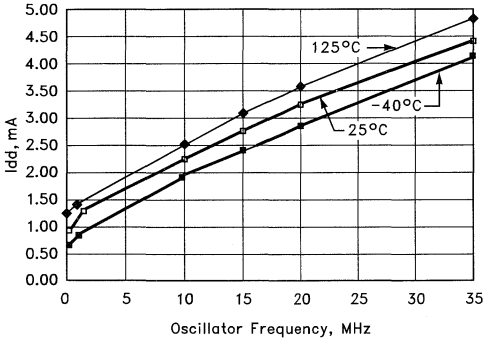
$$\theta_E = \frac{T_H}{T_\theta} \times 360°$$

T_H = H-sync period
T_θ = phase error period

4585-3

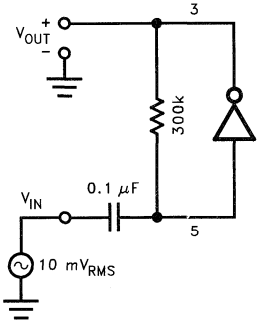
Typical Performance Curves

Idd vs Fosc



4585-4

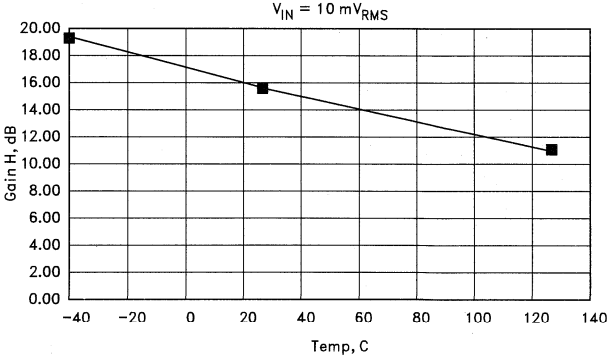
Test Circuit 1



4585-5

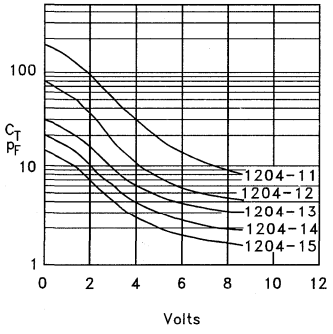
Typical Performance Curves — Contd.

OSC Gain @ 20 MHz vs Temp



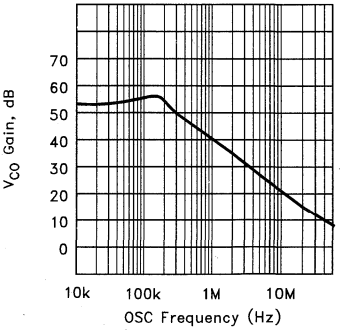
4585-6

Typical Varactor



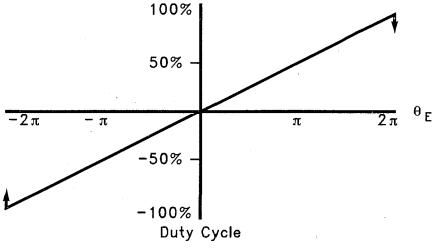
4585-7

OSC Gain vs Fosc



4585-8

Charge Pump Duty Cycle Vs θ_E



4585-9

EL4585C
Horizontal Genlock, 8 F_{SC}

Description Of Operation

The horizontal sync signal (CMOS level, falling leading edge) is input to H-SYNC input (pin 10). This signal is delayed about 110nS, the falling edge of which becomes the reference to which the clock output will be locked. (See timing diagrams.) The clock is generated by the signal on pin 5, OSC in. There are 2 general types of VCO that can be used with the EL4585C, LC and crystal controlled. Additionally, each type can be either built up using discrete components, including a varactor as the frequency controlling element, or complete, self contained modules can be purchased with everything inside a metal can. These modules are very forgiving of PCB layout, but cost more than discrete solutions. The VCO or VCXO is used to regulate the clock. An LC tank resonator has greater "pull" than a crystal controlled circuit, but will also be more likely to drift over time, and thus will generate more jitter. The "pullability" of the circuit refers to the ability to pull the frequency of oscillation away from its center frequency by modulating the voltage on the control pin of the VCO module or varactor, and is a function of the slope and range of the capacitance-voltage curve of the varactor or VCO module used. The VCO signal is sent to the CLK out pin, divided by two, then sent to the divide by N counter. The divisor N is determined by the state of pins 1, 2, and 16 and is described in table 5 above. The divided signal is sent, along with the delayed H-sync input, to the phase/frequency detector, which compares the two signals for phase and frequency differences. Any phase difference is converted to a current at the charge pump output, FILTER (pin 7). A VCO with a positive frequency deviation with control voltage must be used. Varactors have negative capacitance slope with voltage, resulting in positive frequency deviation with increasing control voltage for the oscillators in figures 10 and 11 below.

VCO

The VCO should be tuned so that its frequency of oscillation is very close to the required clock output frequency when the voltage on the varactor is 2.5 volts. VCXO and VCO modules are already tuned to the desired frequency, so this step is not necessary if using one of these units. The output range of the FILTER (pin 7) is 0 to 5 volts, and it can source or sink a maximum of about 300μA, so all frequency control must be accomplished with variable capacitance from the varactor within this range. Crystal oscillators are more stable than LC oscillators, which translates into lower jitter, but LC oscillators can be pulled from their mid-point values further, resulting in a greater capture and locking range. If the incoming horizontal sync signal is known to be very stable, then a crystal oscillator circuit can be used. If the H-sync signal experiences frequency variations of greater than about 300ppm, an LC oscillator should be considered, as crystal oscillators are very difficult to pull this far. When H-sync input frequency is greater than CLK frequency $\div$ 2N, FILTER output (pin 7) sources current into the filter capacitor, increasing the voltage across the varactor, thus tending to increase VCO frequency. Conversely, filter output pulls current from the filter capacitor when H-sync frequency is less than CLK $\div$ 2N, forcing the VCO frequency lower.

Loop Filter

The loop filter controls how fast the VCO will respond to a change in phase comparator output stimulus. Its components should be chosen so that fast lock can be achieved, yet with a minimum of VCO "hunting", preferably in one to two oscillations of filter output, assuming the VCO frequency starts within capture range. If the filter is under-damped, the VCO will over and under-shoot the desired operating point many times before a stable lock takes place. It is possible to under-damp the filter so much that the loop itself oscillates, and VCO lock is never achieved. If the filter is over-damped, the VCO response time will be excessive and many cycles will be required for a lock condition. Over-damping is also characterized by an easily unlocked system because the filter can't respond fast enough to perturbations in VCO frequency. A severely over damped system will seem to endlessly oscillate, like a very large mass at the end of a long pendulum. Due to parasitic effects of PCB traces and component variables, it will take some trial and error experimentation to determine the best values to use for any given situation. Use the component tables as a starting point, but be aware that deviations from these values are not out of the ordinary.

Description Of Operation — Contd.

External Divide

DIV SEL (pin 8) controls the use of the internal divider. When high, the internal divider is enabled and EXT DIV (pin 13) outputs the CLK out divided by 2N. This is the signal to which the horizontal sync input will lock. When divide select is low, the internal divider output is disabled, and external divide becomes an input from an external divider, so that a divisor other than one of the 8 pre-programmed internal divisors can be used.

Normal Mode

Normal mode is enabled by pulling COAST (pin 9) low (below $\frac{1}{3}$*Vcc). If H-SYNC and CLK ÷ 2N have any phase or frequency difference, an error signal is generated and sent to the charge pump. The charge pump will either force current into or out of the filter capacitor in an attempt to modulate the VCO frequency. Modulation will continue until the phase and frequency of CLK ÷ 2N exactly match the H-sync input. When the phase and frequency match (with some offset in phase that is a function of the VCO characteristics), the error signal goes to zero, lock detect no longer pulses high, and the charge pump enters a high impedance state. The clock is now locked to the H-sync input. As long as phase and frequency differences remain small, the PLL can adjust the VCO to remain locked and lock detect remains low. Once locked, the phase/frequency detector becomes a phase only detector so that missing sync pulses will not disturb the VCO output. If H-sync disappears completely, filter output goes into a high impedance state, which is functionally equivalent to coast mode.

Fast Lock Mode

Fast Lock mode is enabled by either allowing coast to float, or pulling it to mid supply (between $\frac{1}{3}$ and $\frac{2}{3}$*Vcc). In this mode, lock is achieved much faster than in normal mode, but the clock divisor is modified on the fly to achieve this. If the phase detector detects an error of enough magnitude, the clock is either inhibited or reset to attempt a "fast lock" of the signals. Forcing the clock to be synchronized to the H-sync input this way allows a lock in approximately 2 H-cycles, but the clock spacing will not be regular during this time. Once the near lock condition is attained, filter output should be very close to its lock-on value, and placing the device into normal mode should result in a normal lock very quickly. Fast lock mode is intended to be used where H-sync becomes irregular, until a stable signal is again obtained.

Coast Mode

Coast mode is enabled by pulling COAST (pin 9) high (above $\frac{2}{3}$*Vcc). In coast mode the internal phase detector is disabled and filter out remains in high impedance mode to keep filter out voltage and VCO frequency as constant a possible. VCO frequency will drift as charge leaks from the filter capacitor, and the voltage changes the VCO operating point. Coast mode is intended to be used when noise or signal degradation result in loss of horizontal sync for many cycles. The phase detector will not attempt to adjust to the resultant loss of signal so that when horizontal sync returns, sync lock can be re-established quickly. However, if much VCO drift has occurred, it may take as long to re-lock as when restarting.

Lock Detect

Lock detect (pin 12) will go low when lock is established. Any DC current path from FILTER out will skew EXT DIV relative to H-SYNC in, tending to offset or add to the 110nS internal delay, depending on which way the extra current is flowing. This offset is called static phase error, and is always present in any PLL system. If, when the part stabilizes in a locked mode, lock detect is not low, adding or subtracting from the series resistor will change this static phase error to allow LDET to go low while in lock. The goal is to put the rising edge of EXT DIV in sync with the falling edge of H-SYNC + 110nS. (See timing diagrams.) Increasing R_2 increases phase error, while decreasing R_2 decreases phase error. (Phase error is positive when EXT DIV lags H-SYNC.) The resistance needed will depend on VCO design or VCXO module selection.

EL4585C
Horizontal Genlock, 8 F_{SC}

Applications Information

Choosing External Components

1. To choose LC VCO components, first pick the desired operating frequency. For our example we will use 28.636MHz, with an H-sync frequency of 15.734kHz.
2. Choose a reasonable inductor value (1-5μH works well). We choose 3.3μH.
3. Calculate C_T needed to produce F_{OSC}.

$$F_{OSC} = \frac{1}{2\pi\sqrt{LC_T}}$$

$$C_T = \frac{1}{4\pi^2F^2L} = \frac{1}{4\pi^2(28.636e6)^2(3.3e-6)} = 9.4pF$$

4. From the varactor data sheet find C_V @ 2.5V, the desired lock voltage. $C_V = 23pF$ for our SMV1204-12 for example.
5. C_2 should be about $10C_V$, so we choose $C_2 = 220pF$ for our example.
6. Calculate C_1. Since

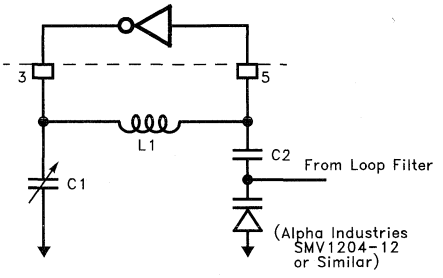
$$C_T = \frac{C_1C_2C_V}{(C_1C_2) + (C_1C_V) + (C_2C_V)},$$

then

$$C_1 = \frac{C_2C_TC_V}{(C_2C_v) - (C_2C_T) - (C_TC_V)}.$$

For our example, $C_1 = 17pF$. (A trim cap may be used for fine tuning.) Examples for each frequency using the internal divider follow.

Typical LC VCO



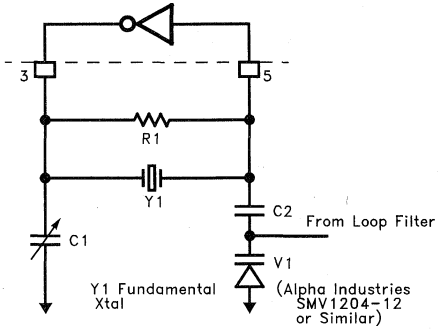
4585-10

LC VCO Component Values (Approximate)

Frequency (MHz)	L1 (μH)	C1 (pF)	C2 (pF)
26.602	3.3	22	220
27.0	3.3	21	220
29.5	2.7	22	220
35.468	2.2	16	220
21.476	4.7	26	220
24.546	3.9	22	220
28.636	3.3	17	220

Note: Use shielded inductors for optimum performance.

Typical Xtal VCO



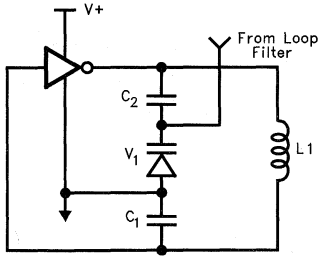
4585-11

Xtal VCO Component Values (Approximate)

Frequency (MHz)	R1 (kΩ)	C1 (pF)	C2 (μF)
26.602	300	15	.001
27.0	300	15	.001
29.5	300	15	.001
35.468	300	15	.001
21.476	300	15	.001
24.546	300	15	.001
28.636	300	15	.001

The above oscillators are arranged as Colpitts oscillators, and the structure is redrawn here to emphasize the split capacitance used in a Colpitts oscillator. It should be noted that this oscillator configuration is just one of literally hundreds possible, and the configuration shown here does not necessarily represent the best solution for all applications. Crystal manufacturers are very informative sources on the design and use of oscillators in a wide variety of applications, and the reader is encouraged to become familiar with them.

Colpitts Oscillator



4585-12

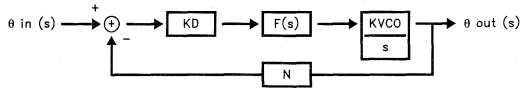
C_1 is to adjust the center frequency, C_2 DC isolates the control from the oscillator, and V1 is the primary control device. C_2 should be much larger than C_V so that V_1 has maximum modulation capability. The frequency of oscillation is given by:

$$F = \frac{1}{2\pi\sqrt{LC_T}}$$

$$C_T = \frac{C_1C_2C_V}{(C_1C_2) + (C_1C_V) + (C_2C_V)}$$

Choosing Loop Filter Components

The PLL, VCO, and loop filter can be described as:



4585-13

Where:

K_d = phase detector gain in A/rad

F(s) = loop filter impedance in V/A

K_{VCO} = VCO gain in rad/s/V

N = Total internal or external divisor (see 3 below)

It can be shown that for the loop filter shown below:

$$C_3 = \frac{K_dK_{VCO}}{N\omega_n^2},\ C_4 = \frac{C_3}{10},\ R_3 = \frac{2N\zeta\omega_n}{K_dK_{VCO}}$$

Where ω_n = loop filter bandwidth, and ζ = loop filter damping factor.

1. K_d = 300μA/2πrad = 4.77e-5A/rad for the EL4585C.
2. The loop bandwidth should be about H-sync frequency/20, and the damping ratio should be 1 for optimum performance. For our example, ω_n = 15.734kHz/20 = 787 Hz ≈ 5000 rad/S.
3. N = 910x2 = 1820 from table 1.

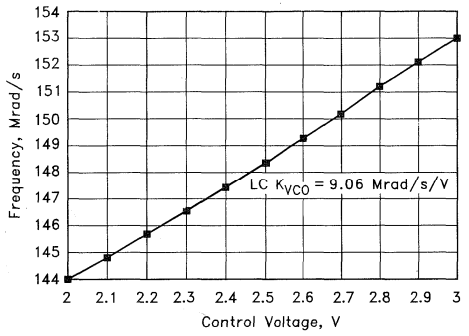
$$N = \frac{F_{VCO}}{F_{Hsync}} = \frac{28.636M}{15.73426k} = 1820 = 910x2$$

4. K_{VCO} represents how much the VCO frequency changes for each volt applied at the control pin. It is assumed (but probably isn't) linear about the lock point (2.5V). Its value depends on the VCO configuration and the varactor

EL4585C
Horizontal Genlock, 8 F_{SC}

transfer function $C_v = F(V_C)$, where V_C is the reverse bias control voltage, and C_V is varactor capacitance. Since $F(V_C)$ is nonlinear, it is probably best to build the VCO and measure K_{VCO} about 2.5V. The results of one such measurement are shown below. The slope of the curve is determined by linear regression techniques and equals K_{VCO}. For our example, $K_{VCO} = 9.06$ Mrad/s/V.

F_{OSC} vs V_C, LC VCO



4585-14

5. Now we can solve for C_3, C_4, and R_3.

$$C_3 = \frac{K_d K_{VCO}}{N\omega_n^2} = \frac{(4.77e-5)(9.06e6)}{(1820)(5000)^2} = 0.01\mu F$$

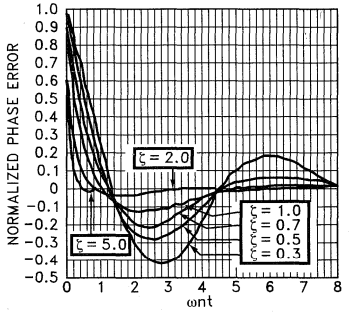
$$C_4 = \frac{C_3}{10} = 0.001\mu F$$

$$R_3 = \frac{2N\zeta\omega_n}{K_d K_{VCO}} = \frac{(2)(1820)(1)(5000)}{(4.77e-5)(9.06e6)} = 42.1k\Omega$$

We choose $R_3 = 43k\Omega$ for convenience.

6. Notice R_2 has little effect on the loop filter design. R_2 should be large, around 100k, and can be adjusted to compensate for any static phase error T_θ at lock, but if made too large, will slow loop response. If R_2 is made smaller, T_θ (see timing diagrams) increases, and if R_2 increases, T_θ decreases. For LDET to be low at lock, $|T_\theta| < 50$nS. C_4 is used mainly to attenuate high frequency noise from the charge pump. The effect these components have on time to lock is illustrated below.

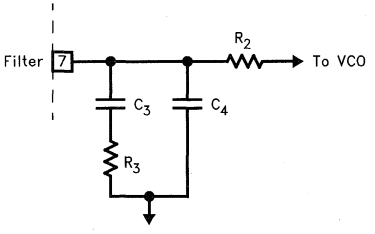
Effect of Loop Filter on Lock Time



4585-15

Let $T = R_3C_3$. As T increases, damping increases, but so does lock time. Decreasing T decreases damping and speeds up loop response, but increases overshoot and thus increases the number of hunting oscillations before lock. Critical damping ($\zeta = 1$) occurs at minimum lock time. Because decreased damping also decreases loop stability, it is sometimes desirable to design slightly overdamped ($\zeta > 1$), trading lock time for increased stability.

Typical Loop Filter



4585-16

LC Loop Filter Components (Approximate)

Frequency (MHz)	R2 (kΩ)	R3 (kΩ)	C3 (μF)	C4 (μF)
26.602	100	39	0.01	0.001
27.0	100	39	0.01	0.001
29.5	100	43	0.01	0.001
35.468	100	51	0.01	0.001
21.476	100	30	0.01	0.001
24.546	100	36	0.01	0.001
28.636	100	43	0.01	0.001

Xtal Loop Filter Components (Approximate)

Frequency (MHz)	R2 (kΩ)	R3 (MΩ)	C3 (pF)	C4 (pF)
26.602	100	4.3	68	6.8
27.0	100	4.3	68	6.8
29.5	100	4.3	68	6.8
35.468	100	4.3	68	6.8
21.476	100	4.3	68	6.8
24.546	100	4.3	68	6.8
28.636	100	4.3	68	6.8

PCB Layout Considerations

It is highly recommended that power and ground planes be used in layout. The oscillator and filter sections constitute a feedback loop and thus care must be taken to avoid any feedback signal influencing the oscillator except at the control input. The entire oscillator/filter section should be surrounded by copper ground to prevent unwanted influences from nearby signals. Use separate paths for analog and digital supplies, keeping the analog (oscillator section) as short and free from spurious signals as possible. Careful attention must be paid to correct bypassing. Keep lead lengths short and place bypass caps as close to the supply pins as possible. If laying out a PCB to use discrete components for the VCO section, care must be taken to avoid parasitic capacitance at the OSC pins 3 and 5, and FILTER out (pin 7). Remove ground and power plane copper above and below these traces to avoid making a capacitive connection to them. It is also recommended to enclose the oscillator section within a shielded cage to reduce external influences on the VCO, as they tend to be very sensitive to "hand waving" influences, the LC variety being more sensitive than crystal controlled oscillators. In general, the higher the operating frequency, the more important these considerations are. Self contained VCXO or VCO modules are already mounted in a shielding cage and therefore do not require as much consideration in layout. Many crystal manufacturers publish informative literature regarding use and layout of oscillators which should be helpful.

EL4585C
Horizontal Genlock, 8 F_{SC}

Component Sources

Inductors

- Dale Electronics
  E. Highway 50
  PO Box 180
  Yankton, SD 57078-0180
  (605) 665-9301

Crystals, VCXO, VCO Modules

- Connor-Winfield
  2111 Comprehensive Drive
  Aurora, IL 60606
  (708) 851-4722

- Piezo Systems
  100 K Street
  PO Box 619
  Carlisle, PA 17013
  (717) 249-2151

- Reeves-Hoffman
  400 West North Street
  Carlisle, PA 17013
  (717) 243-5929

- SaRonix
  151 Laura Lane
  Palo Alto, CA 94043
  (415) 856-6900

- Standard Crystal
  9940 Baldwin Place
  El Monte, CA 91731
  (818) 443-2121

Varactors

- Alpha Industries
  20 Sylvan Road
  Woburn, MA 01801
  (617) 935-5150

- Motorola Semiconductor Products
  2100 E. Elliot
  Tempe, AZ 85284
  (602) 244-6900

Note: These sources are provided for information purposes only. No endorsement of these companies is implied by this listing.

Communications

élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL1501C—SLIDE*

Differential Line Driver/Receiver

Features

- Complete ADSL differential driver and receiver
- 45 V_{p-p} differential output drive into 200Ω
- −60 dB typical output distortion at full output at 2 MHz
- −73 dB typical receive distortion at 15 V_{p-p} levels at 2 MHz
- Drives 8 single-ended video loads, or 4 S-VHS loads, or 4 differential video loads
- Power surface-mount package

Applications

- ADSL line interface
- HDSL line driver
- Video distribution amplifier
- Video twisted-pair line driver

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL1501CM	−40°C to +85°C	20-Lead SO	MDP0027

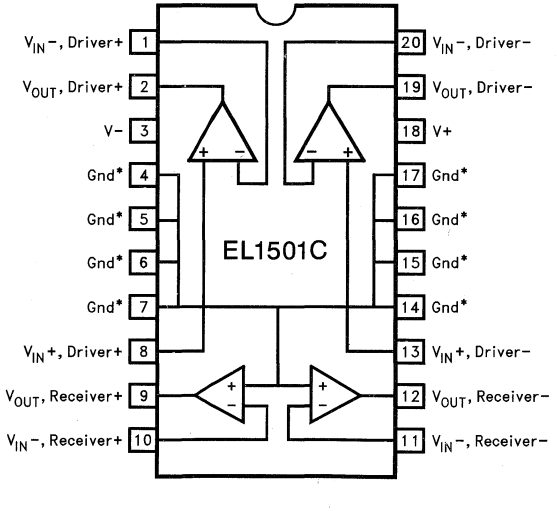
General Description

The EL1501C contains two wideband high-voltage drivers and two receive amplifiers. It is designed to drive 45 V_{p-p} signals at 2 MHz into a 200Ω load differentially with very low distortion. The receive amplifiers also provide very low distortion and noise, and with external resistors can be wired as a hybrid coupler.

All amplifiers are of the current-feedback type, giving high slewrates while consuming moderate power. They retain frequency response over a wide range of externally set gains.

The EL1501C operates on ±5V to ±15V supplies, and retains its bandwidths and linearities over the supply range.

Eight center package pins are used as ground connections and heat spreaders, allowing a dissipation of 2W at the maximum ambient temperature of 85°C.



1501-1

*Subscriber Line Interface Device

EL1501C—SLIDE*
Differential Line Driver/Receiver

Absolute Maximum Ratings (T_A = 25°C)

V_S	V+ to V− Supply Voltage	33V	I_{OUT}, rec	Output Current from Receiver (Static)	15 mA
V+	V+ Voltage to Ground	−0.3V to +33V	P_D	Maximum Power Dissipation	See Curves
V−	V− Voltage to Ground	−33V to 0.3V	T_A	Operating Temperature Range	−40°C to +85°C
V_{IN}+	Driver V_{IN}+ Voltage	V− to V+	T_S	Storage Temperature Range	−60°C to +150°C
I_{IN}	Current into any Input	8 mA			
I_{OUT}, driver	Output Current from Driver (Static)	75 mA			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open-Loop DC Electrical Characteristics

Power supplies at ±15V, R_F for both drivers and receivers is 1 kΩ, R_L for driver is 75Ω, R_L for receiver is 200Ω. T_A = 25°C. Amplifiers tested separately.

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}, driver	Driver Input Offset Voltage	−30		30	I	mV
ΔV_{OS}, drivers	Driver-to-Driver V_{OS} Mismatch	−10		10	I	mV
I_B+, driver	Non-Inverting Driver Input Bias Current	−10		10	I	µA
I_B−, driver	Inverting Driver Input Bias Current	−40		40	I	µA
ΔI_B−, drivers	Driver-to-Driver I_B− Mismatch	−36		36	I	µA
R_{OL}, drivers	Driver Transimpedance, V_{OUT} from −12V to +12V	0.4	1.6		I	MΩ
V_{OUT}, driver	Driver Loaded Output Swing	±12.0	±13		I	V
V_{OS}, receiver	Receiver Input Offset Voltage	−30		30	I	mV
ΔV_{OS}, receivers	Receiver-to-Receiver V_{OS} Mismatch	−10		10	I	mV
I_B−, receiver	Receiver Inverting Input Bias Current	−15		15	I	µA
ΔI_B−, receiver	Receiver-to-Receiver I_B− Mismatch	−16		16	I	µA
R_{OL}, receiver	Receiver Transimpedance, V_{OUT} from −4V to +4V	2	6		I	MΩ
V_{OUT}, receiver	Receiver Loaded Output Swing	±6.25	±10		I	V
I_S	All Outputs at 0V	30	36	45	I	mA

Closed-Loop AC Electrical Characteristics

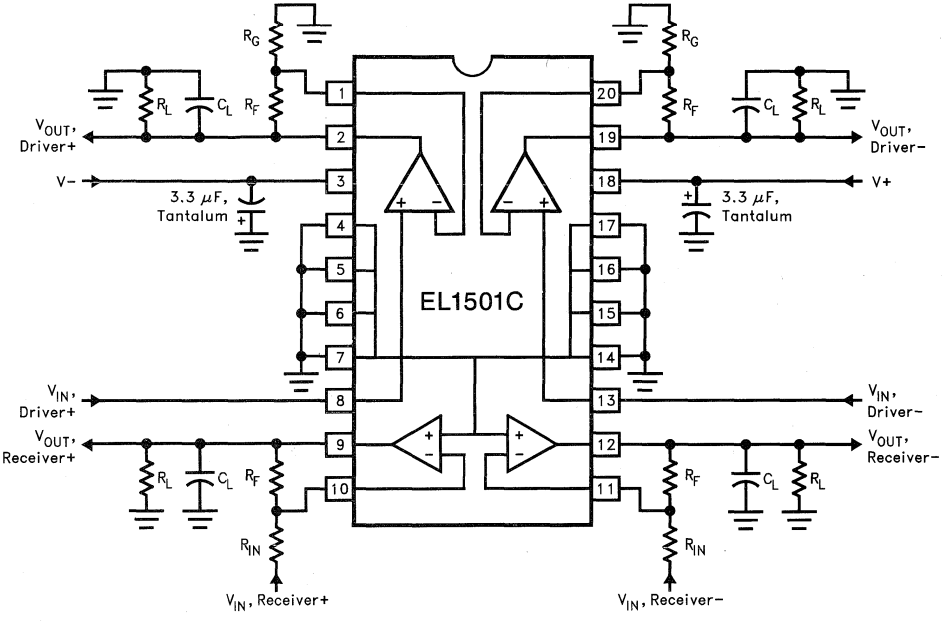
Power supplies at ±15V, R_F for both drivers and receivers is 510Ω, R_L for drivers is 75Ω, R_L for receivers is 200Ω. C_L = 15 pF. Driver gain is +10 and receiver gain is −1. T_A = 25°C. Amplifiers tested separately.

Parameter	Description	Min	Typ	Max	Test Level	Units
BW, driver	−3 dB Bandwidth of Driver Amplifiers		63		V	MHz
HD, driver	Total Harmonic Distortion of Driver					
	f = 2 MHz, Supplies at ±15V, 22.5 V_{p-p} Output		−60		V	dBc
	f = 2 MHz, Supplies at ±9V, 10.5 V_{p-p} Output		−66		V	dBc
	f = 300 kHz, Supplies at ±5V, 6 V_{p-p} Output		−71		V	dBc
dG, driver	Driver Differential Gain Error, Standard NTSC Test					
	A_V = +2, V_S = ±12V, R_L = 37.5Ω		0.17		V	%
dθ, driver	Driver Differential Phase Error, Standard NTSC Test					
	A_V = +2, V_S = ±12V, R_L = 37.5Ω		0.06		V	°
SR, driver	Driver Slewrate, V_{OUT} from −10V to +10V Measured at ±5V	TBD	1000		I	V/μsec
e_N, driver	Driver Input Noise Voltage		3.3		V	nV/√Hz
i_N, driver	Driver −Input Noise Current		18		V	pA/√Hz
BW, receiver	−3 dB Bandwidth of Receive Amplifiers		80		V	MHz
HD, receiver	Total Harmonic Distortion of Receive Amplifiers					
	f = 2 MHz, Supplies at ±15V, 11.25 V_{p-p} Output		−72		V	dBc
	f = 2 MHz, Supplies at ±9V, 5.25 V_{p-p} Output		−71		V	dBc
	f = 300 kHz, Supplies at ±5V, 3 V_{p-p} Output		−73		V	dBc
SR, receiver	Receiver Slewrate, V_{OUT} from −4V to +4V Measured at ±2.5V	TBD	600		I	V/μsec
e_N, receiver	Receiver Input Noise Voltage		3		V	nV/√Hz
i_N, receiver	Receiver −Input Noise Current		12		V	pA/√Hz

4

EL1501C—SLIDE*
Differential Line Driver/Receiver

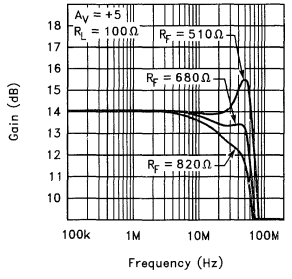
Test Circuit



1501-2

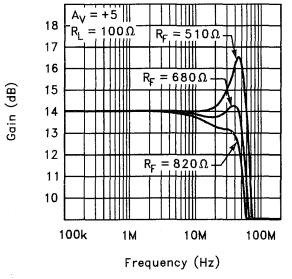
Typical Performance Curves

Driver Frequency Response vs R_F at ±15V Supplies



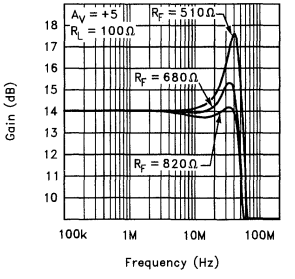
1501-3

Driver Frequency Response vs R_F at ±9V Supplies



1501-4

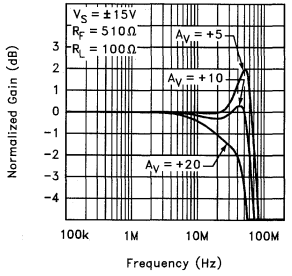
Driver Frequency Response vs R_F at ±5V Supplies



1501-5

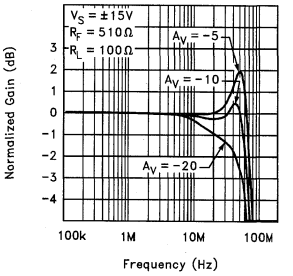
Typical Performance Curves — Contd.

Driver Frequency Response vs Gain (Non-Inverting)



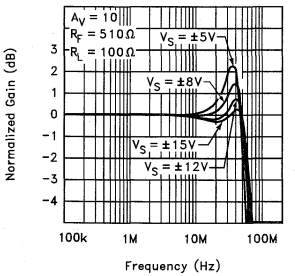
1501-6

Driver Frequency Response vs Gain (Inverting)



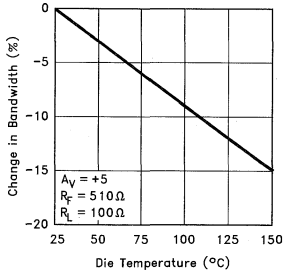
1501-7

Driver Frequency Response vs ± Supply Voltage



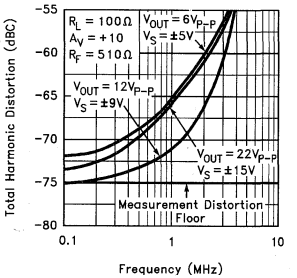
1501-8

Driver Bandwidth vs Temperature



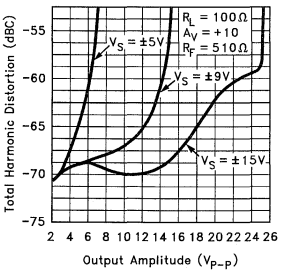
1501-9

Driver Harmonic Distortion vs Frequency (Single Amplifier)



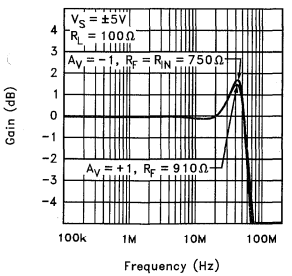
1501-10

Driver Harmonic Distortion vs Output Amplitude at 2 MHz (Single Amplifier)



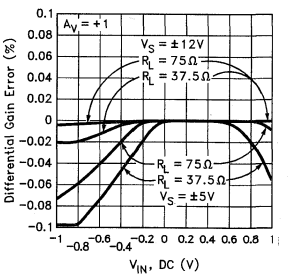
1501-11

Driver Frequency Responses Equalized for Gains of +1 and −1



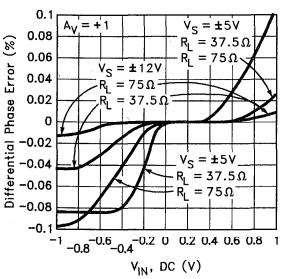
1501-12

Driver Differential Gain Error vs DC Input Offset Gain = +1



1501-13

Driver Differential Phase Error vs DC Input Offset Gain = +1

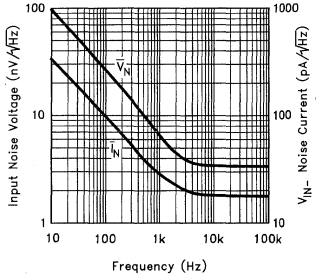


1501-14

EL1501C—SLIDE*
Differential Line Driver/Receiver

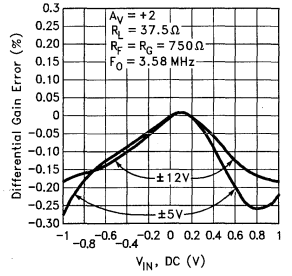
Typical Performance Curves — Contd.

Driver Input Noise Voltage and Current over Frequency



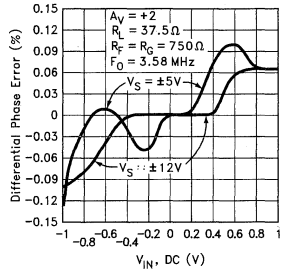
1501-15

Driver Differential Gain Error vs DC Input Voltage—Driving Four Video Loads; Gain = +2



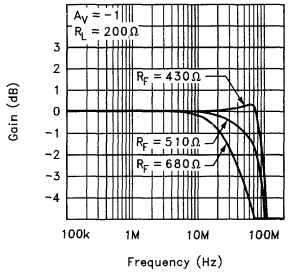
1501-16

Driver Differential Phase Error vs DC Input Voltage—Driving Four Video Loads; Gain = +2



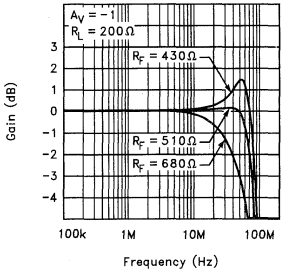
1501-17

Receive Amplifier Frequency Response at V_S = ±15V



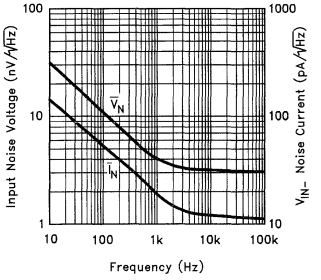
1501-18

Receive Amplifier Frequency Response at V_S = ±5V



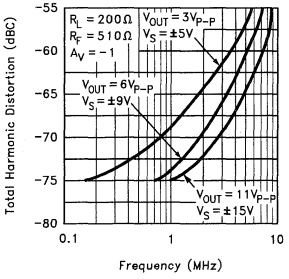
1501-19

Receive Amplifier Input Voltage and Current Noise over Frequency



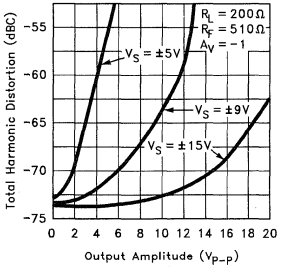
1501-20

Receive Amplifier Harmonic Distortion vs Frequency (Single Amplifier)



1501-21

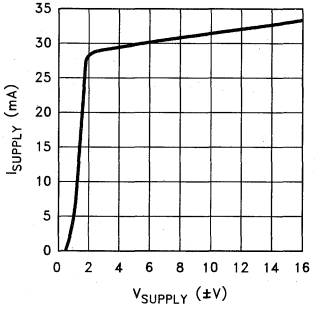
Receive Amplifier Harmonic Distortion vs Output Amplitude at 2 MHz (Single Amplifier)



1501-22

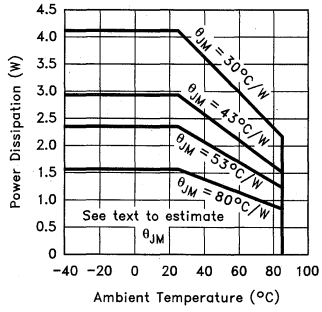
Typical Performance Curves — Contd.

Total Supply Current vs Supply Voltage (All Amplifiers)



1501-23

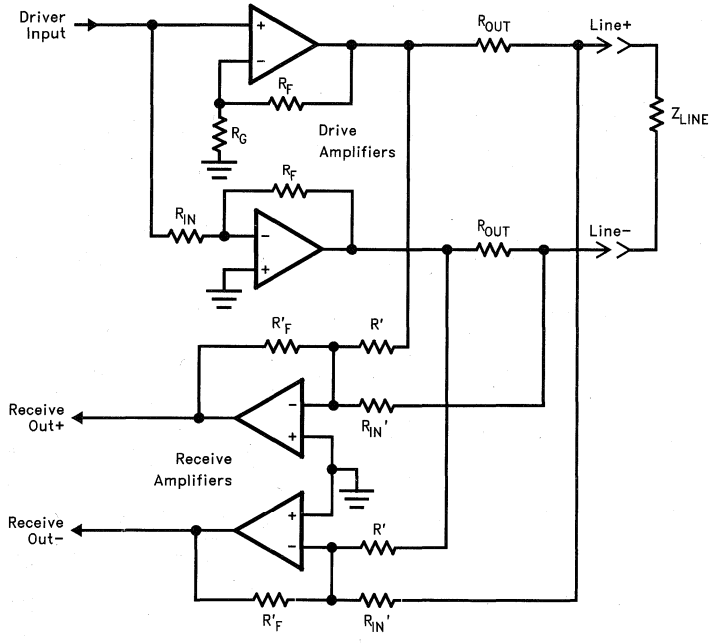
Power Dissipation vs Ambient Temperature for Various Mounted θ_{JM}'s



1501-24

Applications Information

The EL1501C consists of two power line drivers and two receiver amplifiers that can be connected for full duplex differential line transmission and reception. The amplifiers are designed to be used with signals up to 4 MHz and produce low distortion levels. Here is a typical interface circuit:



1501-25

Typical Line Interface Connections

EL1501C—SLIDE*
Differential Line Driver/Receiver

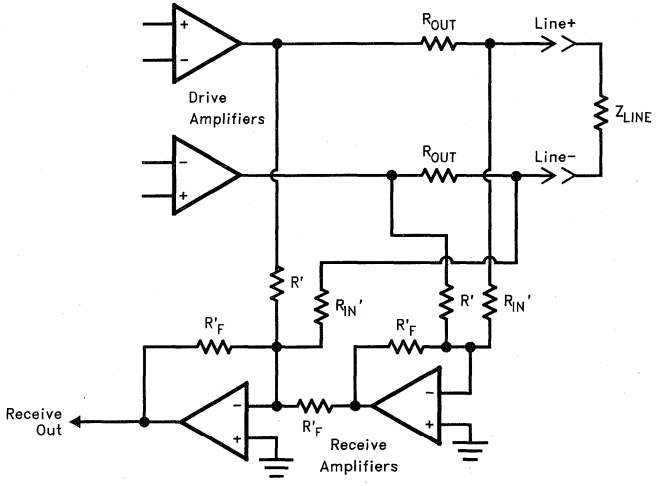
Applications Information — Contd.

The drive amplifiers are wired one in positive gain and the other in negative gain configurations to generate a differential output for a single-ended input. The drivers will exhibit very similar frequency responses for gains of three or greater and thus generate very small common-mode outputs over frequency, but for low gains the two drivers R_F's need to be adjusted to give similar frequency responses. The positive-gain driver will generally exhibit more bandwidth and peaking than the negative-gain driver. The Typical Performance Curves section of this data sheet has a plot of driver responses matched at gains of +1 and −1 using feedback resistors of 910Ω and 750Ω, respectively.

The receiver amplifiers are wired as a hybrid coupler in the circuit. They reject the drivers' output signal (to the matching accuracy of the line impedance and resistors) while passing the signal coming from the line. Their outputs are still differential signals and can be converted to single-ended form by using a wideband instrumentation amplifier such as the EL4430. In a simplistic analysis we set $R_{OUT} = Z_{LINE}/2$ and $R' = 2*R_{IN}'$. Signals coming in from the line convert to currents through the R_{IN}'s and pass through the receive amplifiers. Driver outputs pass through the R′ resistors and produce signal currents, but they are cancelled by opposite-polarity currents through the R_{IN}' resistors.

The actual value of R_{OUT} is increased from $Z_{LINE}/2$ to make its value in parallel R_{IN}' equal $Z_{LINE}/2$ and better match the line. For proper hybrid balance, R′ is increased to compensate for R_{OUT}'s adjustment. For $Z_{LINE} = 130\Omega$ and $R_{IN}' = 510\Omega$, we set $R_{OUT} = 74.5\Omega$ and $R' = 1.17\ k\Omega$.

For operating frequencies below 1 MHz, or in cases where the hybrid rejection of the drive signal is not very critical, the receive amplifiers can be wired to provide a single-ended hybrid coupler output:



1501-27

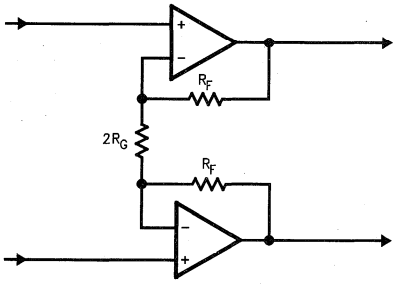
Receive Amplifiers Providing Hybrid and Differential Conversion

Applications Information — Contd.

Common-mode rejection is as good as resistor and line impedance match, as before, but there is a 4 ns time mismatch due to cascading the receive amplifiers. Thus, rejection of common-mode interference will degrade above 1 MHz.

If the receiver amplifiers are not used, their −inputs and outputs may simply be left open. This will reduce power consumption by 2 mA per amplifier.

If a differential signal is available to the drive amplifiers, they may be wired so:



1501-26

Drivers Wired for Differential Input

Each amplifier has identical positive gain connections, and optimum common-mode rejection occurs. Further, DC input errors are duplicated and create common-mode rather than differential line errors.

Input Connections

The receiver amplifiers are not sensitive to source impedances, since they are wired for inverting gain. The drivers are somewhat sensitive to source impedance, however. In particular, they do not like being driven by inductive sources. More than 100 nH of source impedance can cause ringing or even oscillations. This inductance is equivalent to about 4″ of unshielded wiring, or 6″ of unterminated transmission line. Normal high-frequency construction obviates any such problem.

Resistive sources greater than 2 kΩ will cause the driver to exhibit increased harmonic distortion. Most amplifier output stages are much lower in impedance and give no problem.

Power Supplies

The EL1501C works well over the ±5V to ±15V supply range. Frequency response varies only slightly, and output drive capability is constant. The major supply voltage issue is power dissipation. The internal dissipation P_D for an EL1501C running on supply voltages of $\pm V_S$ and delivering a DC output voltage V_O into a load of R_L is

$$P_D = 2 \times V_S \times I_S + \Sigma (V_S - V_O) \times V_O / R_L,$$

where the Σ indicates that all four amplifiers can produce dissipation by each driving a load. If outputs are sinusoidal signals of V_O volts per amplifier peak-to-peak rather than DC the dissipation is

$$P_D = 2 \times V_S \times I_S + \sum \frac{\sqrt{\frac{V_S^2 \times V_O^2}{8} - \frac{V_S \times V_O^3}{3\pi} + \frac{3 \times V_O^4}{128}}}{R_L}$$

Formula 1

As a worst-case example, assume the drivers are running on ±15.75V supplies, each delivering 19.4 V_{p-p} outputs into 119Ω (the parallel of resistors the driver in the first schematic would see), and quiescent supply current I_S is the maximum 43 mA, and is substantially constant over temperature. The quiescent dissipation (the first term of the equation) is 1.42W, and each driver adds 0.44W, for a total of 2.24W dissipation. The 19.4 V_{p-p} output level was chosen to produce the maximum internal dissipation: that is, $V_O = 1.234 \times V_S$ is the most dissipative output level.

The power supplies should be well bypassed close to the EL1501C. 3.3 μF tantalum capacitors work well. Since the load currents are differential, they need not travel through the board copper and set up ground loops that can return to amplifier inputs. Due to the class AB output stage design, these currents have heavy harmonic content. If the ground terminal of the positive and negative bypass capacitors are connected to each other directly and then returned to circuit ground, no ground loops will occur. This scheme is employed in the layout of the EL1501C demonstration board, and documentation can be obtained from the factory.

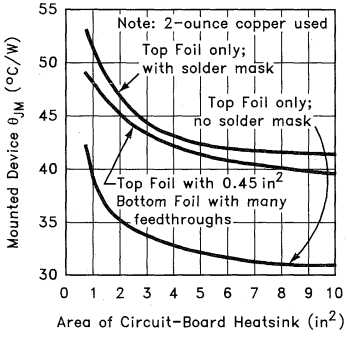
EL1501C—SLIDE*
Differential Line Driver/Receiver

Heat-Sinking

To disperse this heat, the center four leads on either side of the package are internally fused to the mounting platform of the die. Heat flows through the leads into the circuit board copper, then spreading and convecting to air. Thus, the ground plane on the component side of the board becomes the heatsink for the EL1501C. This has proven to be a very effective technique, but several aspects of board layout should be noted. First, the heat should not be shunted to internal copper layers of the board nor backside foil, since the feedthroughs and fiberglass of the board are not very thermally conductive. To obtain the best thermal resistance of the mounted part, θ_{JM}, the topside copper ground plane should have as much area as possible and be as thick as practical. If possible, the solder mask can be cut away from the EL1501C to improve thermal resistance. Finally, metal heatsinks can be placed against the board close to the part to draw heat toward the chassis.

The package will exhibit a θ_{JM} of 80°C/W with no assistance from circuit board heatsinks. This will suffice for the lowest supply voltages and output levels. The best θ_{JM} that can be obtained is about 30°C/W, and a practical layout would produce 43°C/W. More detail is available from the Elantec application note *Measuring the Thermal Resistance of Power Surface-Mount Packages.* This plot summarizes the note's results:

Thermal Resistance of EL1501C vs Copper Area



1501-28

For a given θ_{JM}, the maximum P_D is

$$P_D = (T_{MAX} - T_A)\theta_{JM},$$

where T_{MAX} = 150°C, the maximum die temperature in a plastic package, and T_A is the ambient air temperature.

Output Loading

While the drive amplifiers can output in excess of 250 mA, the internal metallization is not designed to carry more than 75 mA of steady DC current and there is no current-limit mechanism. This allows safely driving peak sinusoidal currents of $\pi \times 75$ mA, or 236 mA. This current is more than that required to drive line impedances to large output levels, but output short circuits cannot be tolerated. The series output resistor will usually limit currents to safe values in the event of line shorts. Driving lines with no series resistor is a serious hazard.

The amplifiers are sensitive to capacitive loading. More than 25 pF will cause peaking of the frequency response. The same is true of badly terminated lines connected without a series matching resistor.

Feedback Resistor Value

The bandwidth and peaking of the amplifiers varies with supply voltage somewhat and with gain settings. The receive amplifiers are connected in inverting mode and will produce a narrow range of characteristics, but the drives can be used for a wide range of gains. The feedback resistor values can be adjusted to produce an optimal frequency response. Here is a series of resistor values that produce an optimal driver frequency response (1 dB peaking) for different supply voltages and gains:

Optimum Driver Feedback Resistor for Various Gains and Supply Voltages

Supply Voltage	Driver Voltage Gain				
	−1	+1	2.5	5	10
±5V	750Ω	910Ω	750Ω	680Ω	620Ω
±9V	680Ω	820Ω	680Ω	620Ω	510Ω
±15V	620Ω	750Ω	620Ω	510Ω	470Ω

Driving Video Loads

Each driver amplifier can drive four doubly-terminated video loads while operating on ±5V supplies. Larger supply voltages slightly improve differential gain and phase distortions, which are around 0.2% and 0.1° for single-ended outputs with the standard NTSC test. Differential-output distortion drops to 0.09% and 0.08°.

Power MOSFET Drivers

élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7154C

High Speed, Monolithic Pin Driver

Features

- Comparatively low cost
- 3-State output
- 3V and 5V Input compatible
- Clocking speeds up to 10 MHz
- 20 ns Switching/delay time
- 4A Peak drive
- Isolated drains
- Low output impedance—2.5Ω
- Low quiescent current—5 mA
- Wide operating voltage—4.5V–16V
- Isolated P-channel device
- Separate ground and V_L pins

Applications

- Loaded circuit board testers
- Digital testers
- Level shifting below GND
- IGBT drivers
- CCD drivers

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL7154CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7154CS	−40°C to +85°C	8-Pin SOIC	MDP0027

Nominal Operating Voltage Range

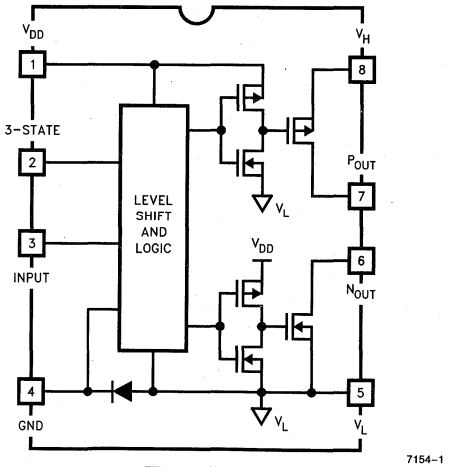
Pin	Min	Max
V_L	−3	0
V_{DD}–V_L	5	15
V_H–V_L	2	15
V_{DD}–V_H	−0.5	15
V_{DD}	5	15

General Description

The EL7154C 3-state pin driver is particularly well suited for ATE and level shifting applications. The 4A peak drive capability, makes the EL7154C an excellent choice when driving high speed capacitive lines.

The p-channel MOSFET is completely isolated from the power supply, providing a high degree of flexibility. Pin (7) can be grounded, and the output can be taken from pin (8) when a "source follower" output is desired. Then n-channel MOSFET has an isolated drain, but shares a common bus with pre-drivers and level shifter circuits. This is necessary to ensure that the n-channel device can turn off effectively when V_L goes below GND. In some power-FET and IGBT applications, negative drive is desirable to insure effective turn-off. The EL7154 can be used in these applications by returning V_L to a moderate negative potential.

Connection Diagram



Top View

Truth Table

3-State	Input	P_{OUT}	N_{OUT}
0	0	Open	Open
0	1	Open	Open
1	0	HIGH	Open
1	1	Open	LOW

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047, #5,352,578, #5,352,389, #5,351,012, #5,374,898

EL7154C
High Speed, Monolithic Pin Driver

Absolute Maximum Ratings

Supply (V_{DD} to V_L; V_H–V_L, V_H to GND),		Ambient Operating Temperature	−40°C to +85°C
V+ to V_H	16.5V	Operating Junction Temperature	125°C
V_L to GND	−5V	Power Dissipation	
Input Pins	−0.3V below V_L to +0.3V above V_{DD}	SOIC	570 mW
		PDIP	1050 mW
Peak Output Current	4A		
Storage Temperature Range	−65°C to +150°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

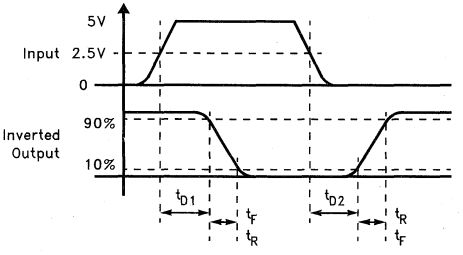
T_A = 25°C, V_{DD} = +12V, V_H = +12V, V_L = −3V, unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input							
V_{IH}	Logic "1" Input Voltage		2.4			I	V
I_{IH}	Logic "1" Input Current	$V_{IH} = V_{DD}$		0.1	10	I	µA
V_{IL}	Logic "0" Input Voltage				0.6	I	V
I_{IL}	Logic "0" Input Current	V_{IL} = 0V		0.1	10	I	µA
V_{HVS}	Input Hysteresis			0.3		V	V
Output							
R_{OH}	Pull-Up Resistance	I_{OUT} = −100 mA		1.5	4	I	Ω
R_{OL}	Pull-Down Resistance	I_{OUT} = +100 mA		2	4	I	Ω
I_{OUT}	Output Leakage Current	V_{DD}/GND		0.2	10	I	µA
I_{PK}	Peak Output Current	Source Sink		4.0 4.0		V	A
I_{DC}	Continuous Output Current	Source/Sink	200			I	mA
Power Supply							
I_S	Power Supply Current	Inputs = V_{DD}		1	2.5	I	mA
V_S	Operating Voltage		4.5		16	I	V
I_G	Current to GND (Pin 4)			1	10	I	µA
I_H	Off Leakage at V_H	Pin 8 = 0V		1	10	I	µA

AC Electrical Characteristics T_A = 25°C unless otherwise specified

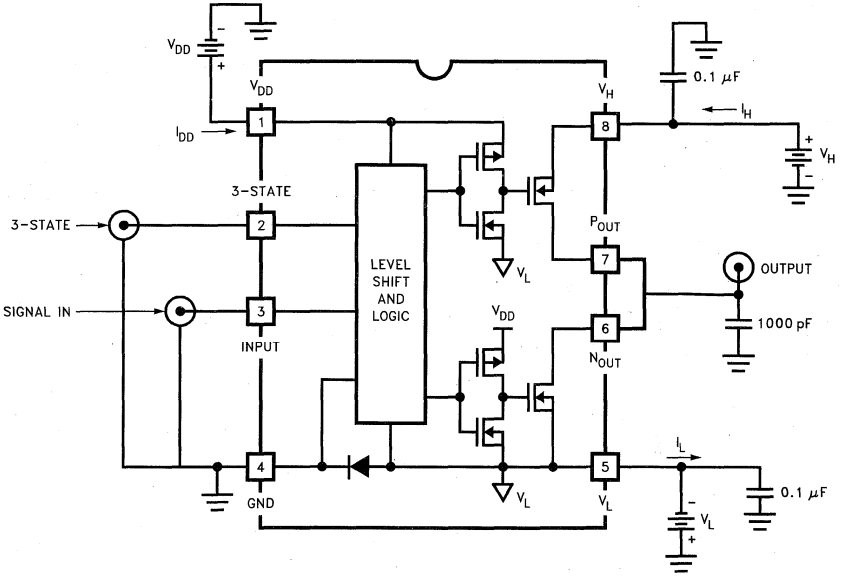
Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics (V_{DD} = V_H = 12V; V_L = −3V)							
t_R	Rise Time	C_L = 100 pF C_L = 2000 pF		4 20	25	IV	ns
t_F	Fall Time	C_L = 100 pF C_L = 2000 pF		4 20	25	IV	ns
t_{D-1}	Turn-Off Delay Time	C_L = 2000 pF		20	25	IV	ns
t_{D-2}	Turn-On Delay Time	C_L = 2000 pF		10	25	IV	ns
t_{D-1}	3-State Delay				25	IV	ns
t_{D-2}	3-State Delay				25	IV	ns

Timing Table



7154-2

Standard Test Configuration

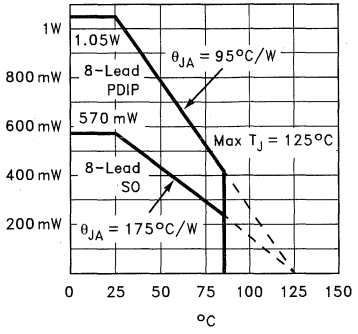


7154-3

EL7154C
High Speed, Monolithic Pin Driver

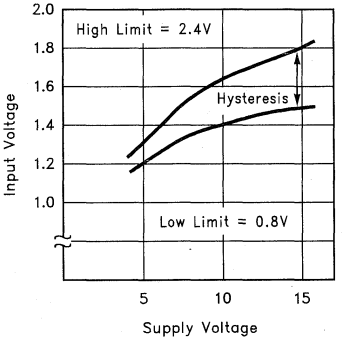
Typical Performance Curves

Max Power/Derating Curves



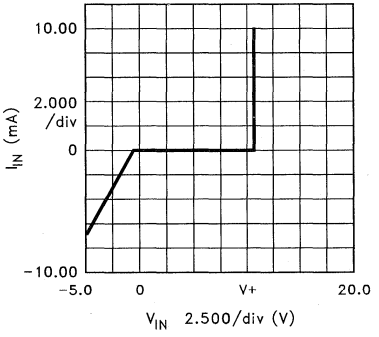
7154-9

Switch Threshold vs Supply Voltage



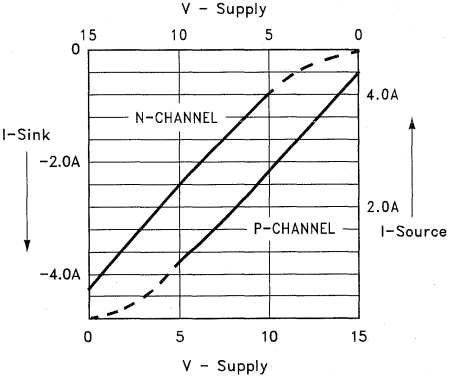
7154-10

Input Current vs Voltage



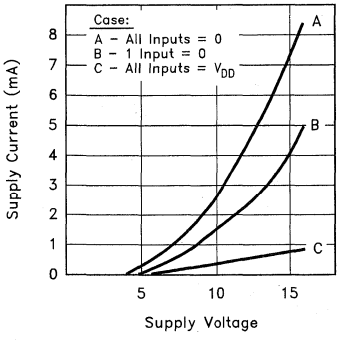
7154-11

Peak Drive vs Supply Voltage



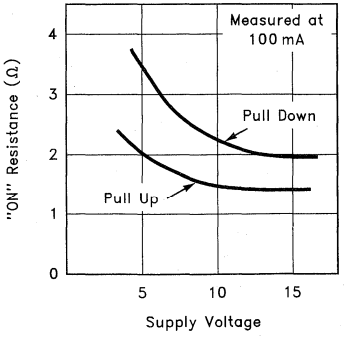
7154-12

Quiescent Supply Current



7154-13

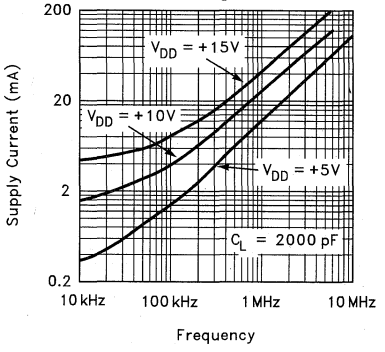
"ON" Resistance vs Supply Voltage



7154-14

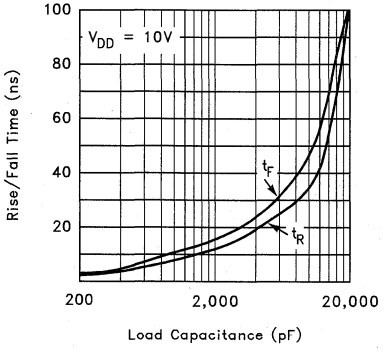
Typical Performance Curves — Contd.

Average Supply Current vs Voltage and Frequency



7154-15

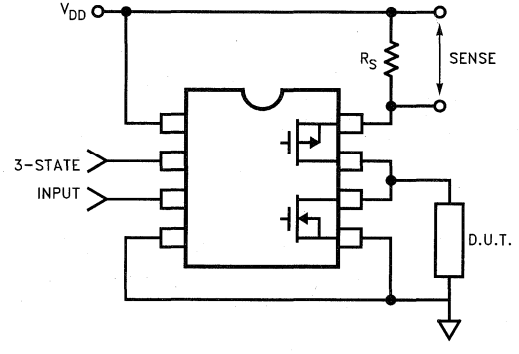
Rise/Fall Time vs Load



7154-16

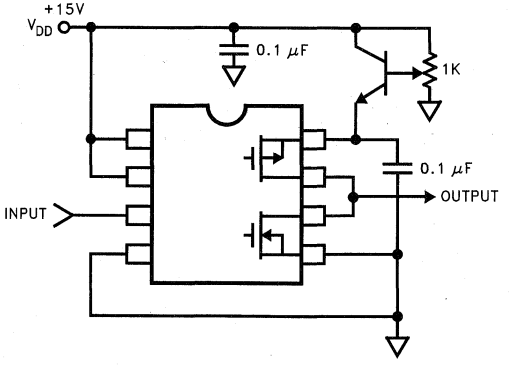
Typical Applications

Pin Driver



7154-4

Adjustable Amplitude Pulse Generator



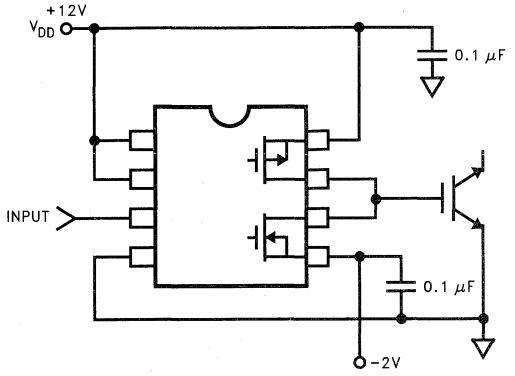
7154-5

5

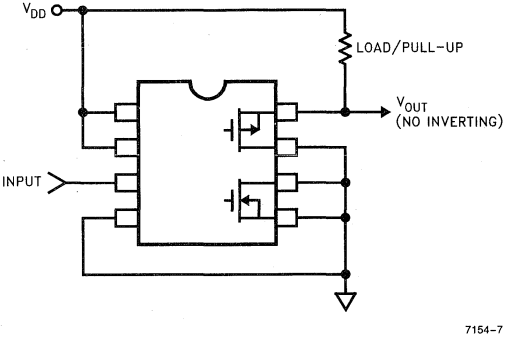
EL7154C
High Speed, Monolithic Pin Driver

Typical Applications — Contd.

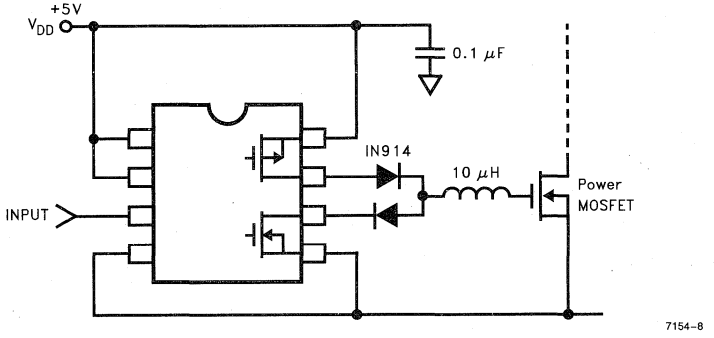
IGBT Driver (with Negative Swing)



PMOS Follower



Resonant Gate Driver



EL7240C/EL7241C
High Speed Coil Drivers

Features

- 20 ns Propagation delay
- Clock to 10 MHz
- 2 Amp peak output drive
- 3Ω output impedance
- 3V/5V Logic input compatible
- Outputs "OK" below ground
- Operating voltage 4.5V to 16V

Applications

- Tape drive-write head driver
- Current switching
- Center-Tapped transformer driver
- ATE-pin drivers
- Analog switching
- AC switching
- T - switch

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL7240CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7240CS	−40°C to +85°C	8-Pin P-SOIC	MDP0027
EL7241CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7241CS	−40°C to +85°C	8-Pin P-SOIC	MDP0027

Operating Voltage Range

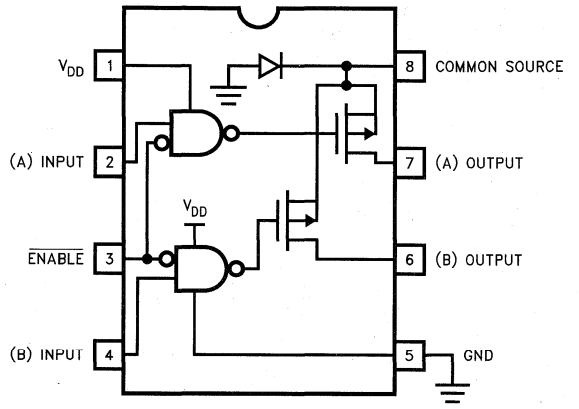
Pins	Min/Max (Volts)
V_{DD}/GND	4.5/16
V_{DD}/Output	0/−20
Source/Output	0/−16
Output/GND	16/−10

General Description

The EL7240C/EL7241C high speed coil drivers accept logic inputs which independently control a pair of 3Ω PMOS FET's. The output transistors share a common source, making these devices well suited for "current steering" and analog switching applications. The typical clamping diodes to ground are removed, thus allowing pins (6) and (7) to swing negative. This feature is desirable when driving "center-tapped" coils referenced to ground. The logic "NAND" input configuration can be used to "enable" the outputs. The EL7240C and EL7241C differ only by their logic polarity.

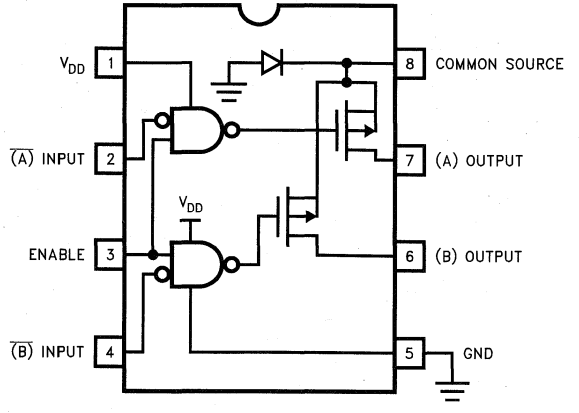
Connection Diagrams

EL7240C



7240-1

EL7241C



7240-2

EL7240C/EL7241C
High Speed Coil Drivers

Absolute Maximum Ratings

Supply (V+ to GND)	16.5V	Operating Junction Temperature	125°C
Input Pins	−0.3V to +0.3V above V+	Power Dissipation	
Combined Peak Output Current	4A	SOIC	670 mW
Storage Temperature Range	−65°C to +150°C	PDIP	1050 mW
Ambient Operating Temperature	−40°C to +85°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input							
V_{IH}	Logic "1" Input Voltage		2.4			I	V
I_{IH}	Logic "1" Input Current	@V+		0.1	10	I	μA
V_{IL}	Logic "0" Input Voltage				0.8	I	V
I_{IL}	Logic "0" Input Current	@0V		0.1	10	I	μA
V_{HVS}	Input Hysteresis			0.3		V	V
Output							
R_{ON}	Pull-Up Resistance	I_{OUT} = −100 mA		3	6	I	Ω
I_{OFF}	Off Leakage	V_{OUT} = 0V	0.2		10	I	μA
I_{PK}	Peak Output Current	Source		2.0		IV	A
I_{DC}	Continuous Output Current	Channel	100			I	mA
V_S	Source Potential with Grounded Drain	Channel A or B 100 mA Load		2.3	2.75	I	V
Power Supply							
I_S	Power Supply Current	Inputs High		1	2.5	I	mA
V_S	Operating Voltage		4.5		16	I	V

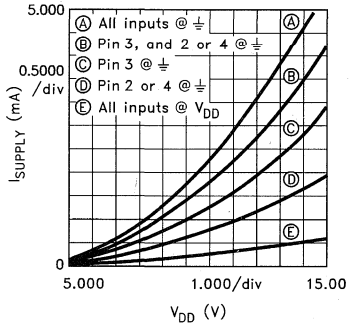
AC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
$t_{D\text{-}ON}$	Turn-On Delay Time			18	25	IV	ns
$t_{D\text{-}OFF}$	Turn-Off Delay Time			20	25	IV	ns

Rise and Fall times (t_R and t_F) are load dependant.

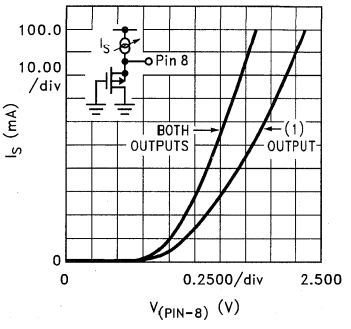
Typical Performance Curves

Supply Current vs V_{DD} and Input Connection



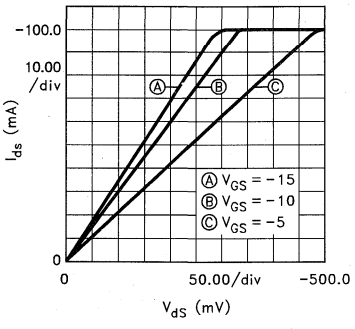
7240-3

Source Voltage vs Current (Grounded Drain)



7240-4

Output Conduction vs V_{GS}

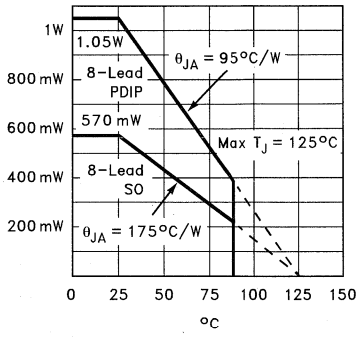


7240-5

EL7240C/EL7241C
High Speed Coil Drivers

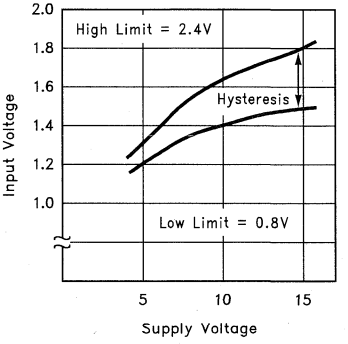
Typical Performance Curves — Contd.

Max Power/Derating Curves



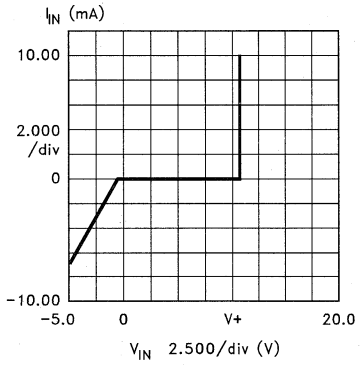
7240-6

Switch Threshold vs Supply Voltage



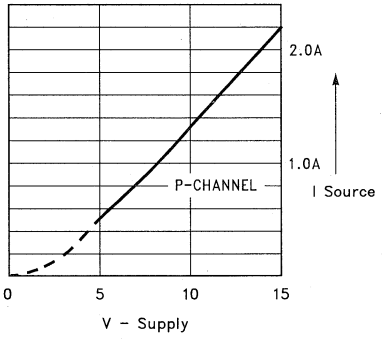
7240-7

Input Current vs Voltage



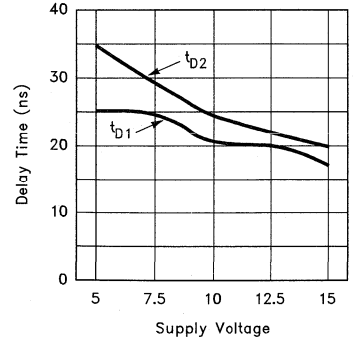
7240-8

Peak Drive vs Supply Voltage



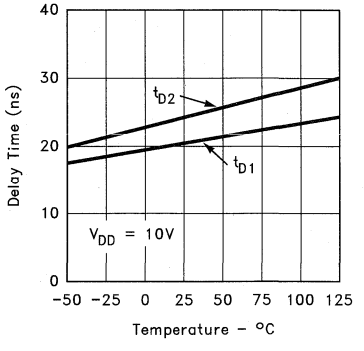
7240-9

Propagation Delay vs Supply Voltage



7240-10

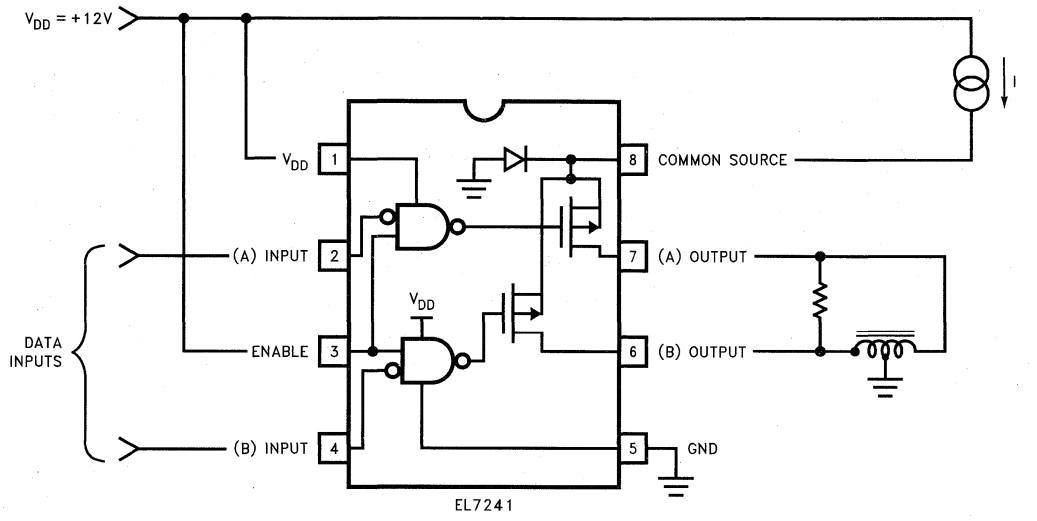
Delay vs Temperature



7240-11

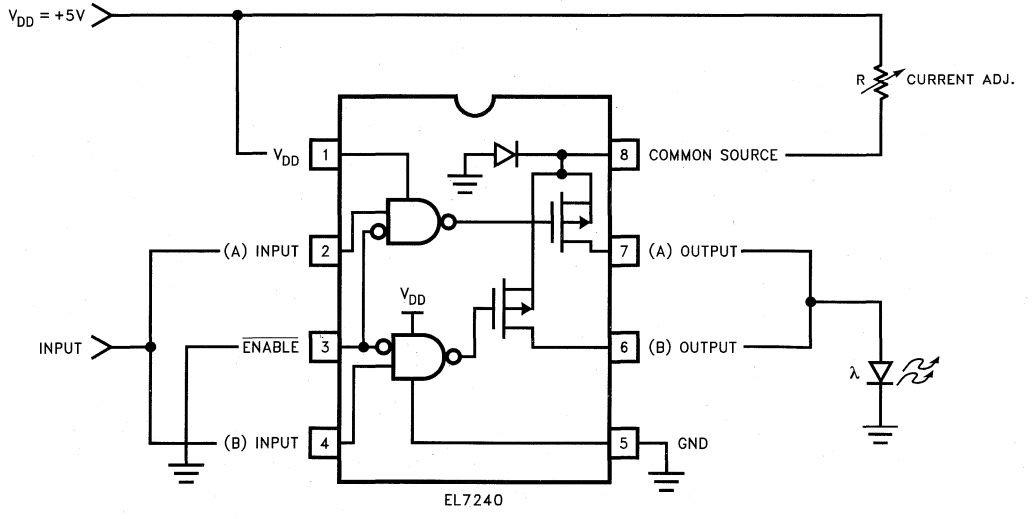
Typical Applications

Write Head Driver



7240-12

High Current LED/Laser Diode Driver

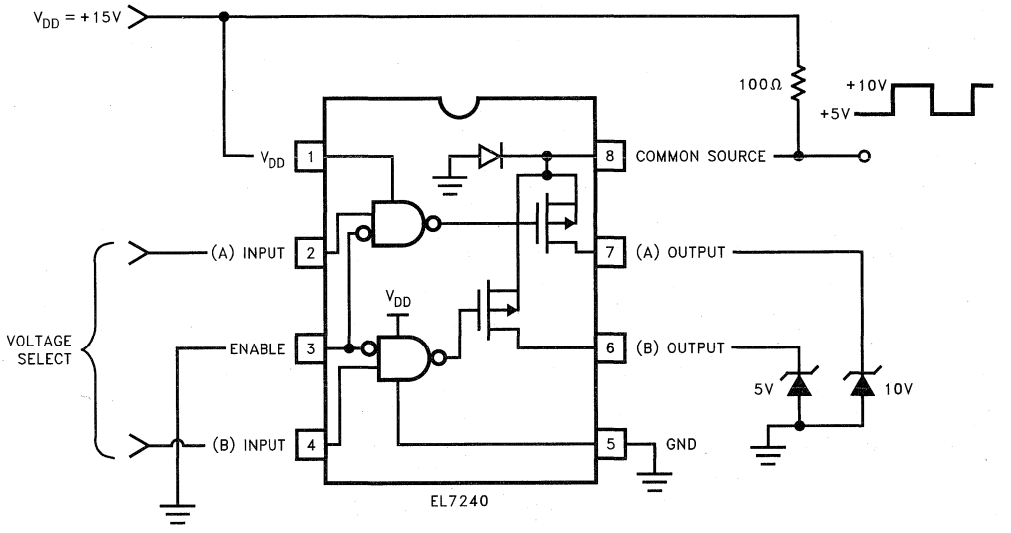


7240-13

EL7240C/EL7241C
High Speed Coil Drivers

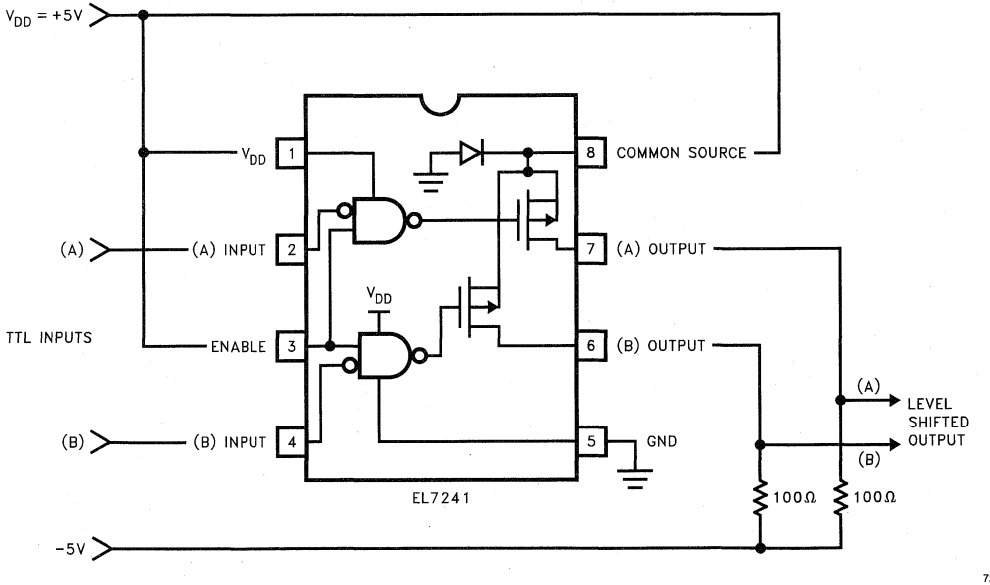
Typical Applications — Contd.

Bi-Level Step Generator



7240-14

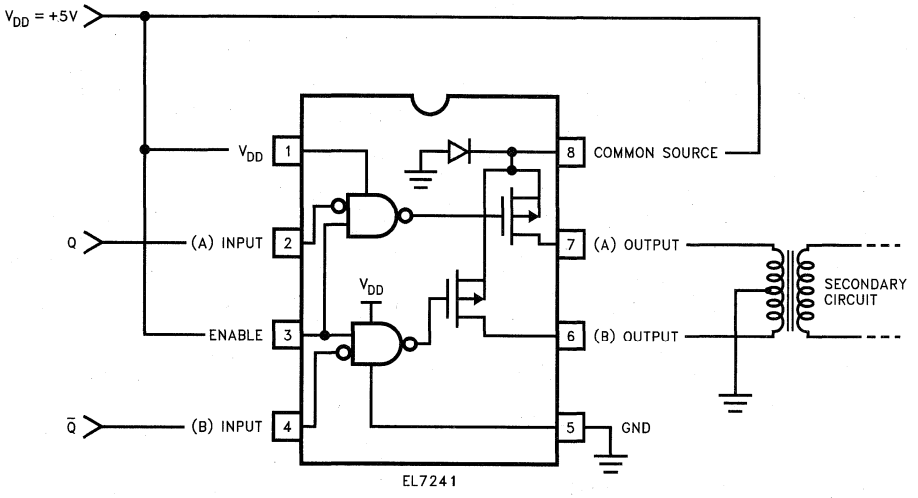
Level Shifter



7240-15

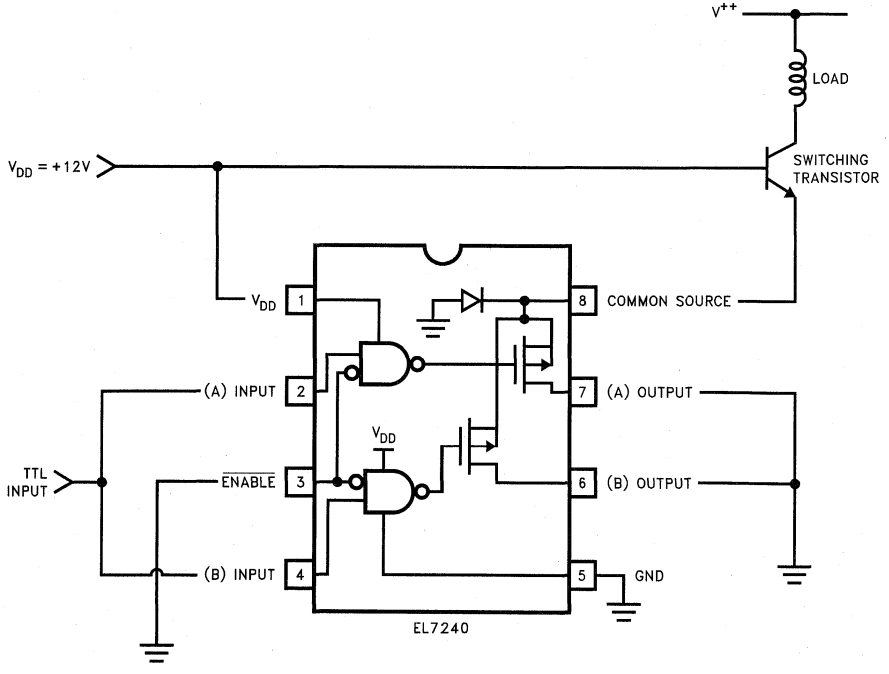
Typical Applications — Contd.

Push-Pull Transformer Driver



7240-16

High Speed Bipolar Drive Circuit

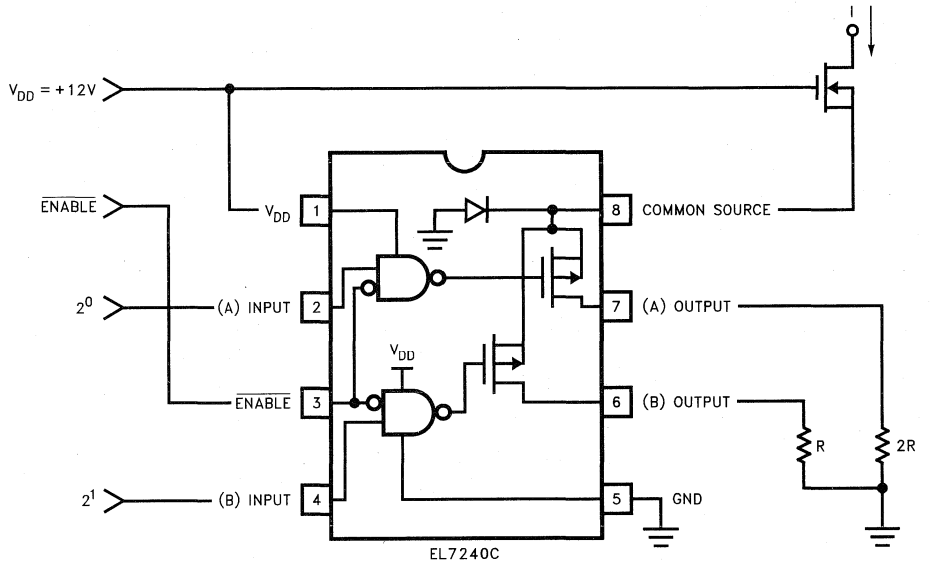


7240-17

EL7240C/EL7241C
High Speed Coil Drivers

Typical Applications — Contd.

"Two-Bit" Current Source with Gating



7240-18

EL7661C
100V Full Bridge Driver

Features

- 100V High Side Voltage
- Programmable Delay
- Direct Coupled
- No Start Up Ambiguity
- Rail to Rail Output
- 1 MHz Operation
- 1.0 Amp Peak Current
- Improved Response Times
- Matched Rise and Fall Times
- Low Supply Current
- Low Output Impedance
- Low Input Capacitance

Applications

- Uninterruptible Power Supplies
- Distributed Power Systems
- IGBT Drive
- DC-DC Converters
- Motor Control
- Power MOSFET Drive
- Switch Mode Power Supplies

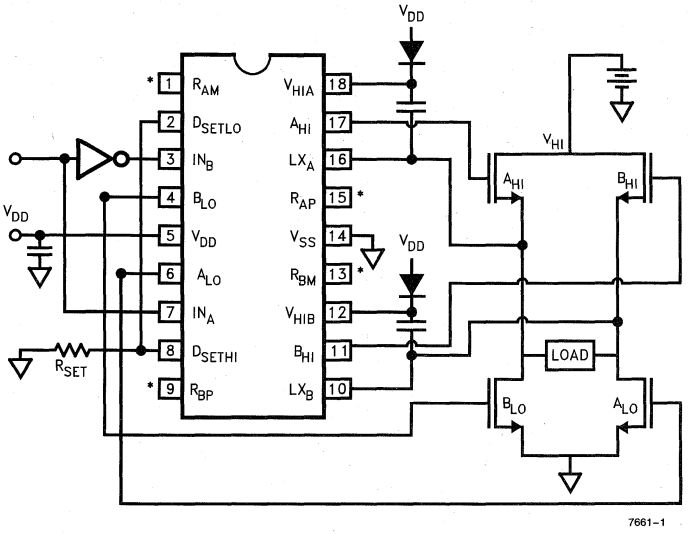
Ordering Information

Part No.	Temp. Range	Package	Outline #
EL7661CN	−40°C to +85°C	18-Pin P-DIP	MDP0031

General Description

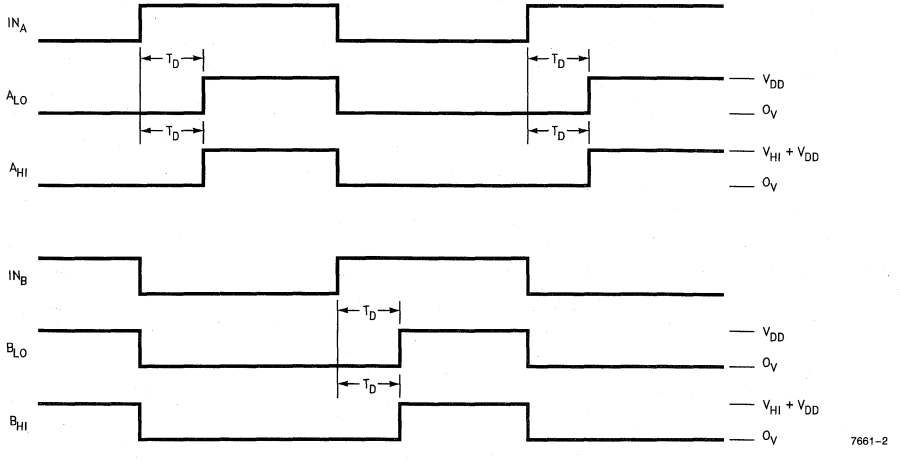
The EL7661 provides a low cost solution to many full bridge applications. The EL7661 is DC coupled so that there are no start up problems associated with AC coupled schemes. A single resistor from the D_{SET} pins to V_{SS} provides "dead time" programmability. Shorting the D_{SET} pins to V_{DD} gives the minimum delay (~ 100 ns).

Connection Diagram



*Pins 1, 9, 13, 15 must be open.

Timing Diagram



EL7661C
100V Full Bridge Driver

Absolute Maximum Ratings (T_A = 25°C)

Supply (V_{HIA} and V_{HIB} to V_{SS})	100V	Storage Temperature Range	−65°C to +150°C
Supply (V_{DD} to GND)	16.5V	Ambient Operating Temperature	−40°C to +85°C
Input Pins	−0.3V below V_{SS}, +0.3V above V_{DD}	Power Dissipation PDIP	1600 mW
Operating Junction Temperature	125°C		
Combined Peak Output Current	4A		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

(T_A = 25C, V_{DD} = 15V, V_{SS} = 0V, C_{LOAD} = 1000 pF, unless otherwise specified)

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input/Output							
V_{IL}	Logic "1" Input Voltage		3.0	2.4		I	V
I_{IH}	Logic "1" Input Current			0.1	10.0	I	μA
V_{IL}	Logic "0" Input Voltage			1.8	0.8	I	V
V_{HYS}	Input Hysteresis			0.5		IV	V
I_{IL}	Logic "0" Input Current			0.1	10.0	I	μA
R_{OH}	Pull-Up Resistance	I_{OUT} = −100 mA		5.0	10.0	I	Ω
R_{OL}	Pull-Down Resistance	I_{OUT} = +100 mA		5.0	10.0	I	Ω
I_{PK}	Peak Output Current			1.0		IV	A
I_{DC}	Continuous Output Current Source/Sink		50.0			IV	mA
Power Supply							
I_{DD}	Supply Current into V_{DD}	R_{SET} = 5.1k Inputs = 15V			15.0	I	mA
I_{HIA}	Supply Current into V_{HIA}				4.0	I	mA
I_{HIB}	Supply Current into V_{HIB}				4.0	I	mA
V_{DD}	Operating Voltage		4.5		15.0	I	V

AC Electrical Characteristics

(T_A = 25C, V_{DD} = 15V, V_{SS} = 0V, C_{LOAD} = 1000 pF, unless otherwise specified)

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
t_R	Rise Time	C_L = 500 pF C_L = 1000 pF		15.0 20.0	 40.0	IV	ns
t_F	Fall Time	C_L = 500 pF C_L = 1000 pF		15.0 20.0	 40.0	IV	ns
$t_{D\ ON\ HI}$	High Side Turn On Delay Time	D_{SET} = V_{DD} R_{SET} = 5.1k R_{SET} = 200k	50.0 75.0 750.0	100.0 125.0 1150.0	150.0 200.0 1500.0	IV I I	ns
$t_{D\ ON\ LO}$	Low Side Turn On Delay Time	D_{SET} = V_{DD} R_{SETLO} = 5.1k R_{SETLO} = 200k	50.0 75.0 750.0	100.0 125.0 1150.0	150.0 200.0 1500.0	IV I I	ns
$t_{D\ OFF\ HI}$	High Side Turn Off Delay Time	D_{SET} = V_{DD}		100.0	150.0	IV	ns
$t_{D\ OFF\ LO}$	Low Side Turn Off Delay Time	D_{SET} = V_{DD}		100.0	150.0	IV	ns
$t_{D\ MISMATCH}$	A_{HI} to A_{LO} Delay Mismatch	D_{SET} = 200k			+ /-10.0	I	%
$t_{D\ MISMATCH}$	B_{HI} to B_{LO} Delay Mismatch	D_{SET} = 200k			+ /-10.0	I	%
$t_{D\ MISMATCH}$	A_{HI} to B_{HI} Delay Mismatch	D_{SET} = 200k			+ /-10.0	I	%
$t_{D\ MISMATCH}$	A_{LO} to B_{LO} Delay Mismatch	D_{SET} = 200k			+ /-10.0	I	%

5

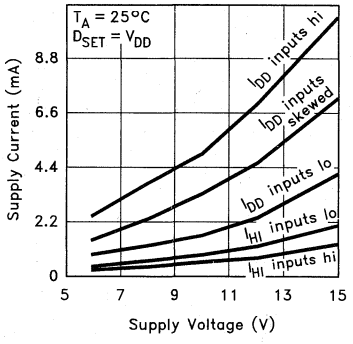
EL7661C
100V Full Bridge Driver

EL7661 Pin Description

Pin #	Name	Description
1	R_{AM}	Internal circuit connection. This pin swings from V_{SS} to V_{DD}. This pin is out of phase with IN_A. Normally this pin should be unconnected to any external circuitry.
2	D_{SETLO}	Connection for the delay setting resistor. This pin must be connected externally to the D_{SETHI} pin. This pin is connected internally to a PMOS diode referenced to V_{DD}.
3	IN_B	Digital input for the "B" drivers. Its polarity is non-inverting with respect to the "B" outputs.
4	B_{LO}	"B" lo-side output. Swings from V_{SS} to V_{DD}.
5	V_{DD}	Positive supply for the lo-side circuitry.
6	A_{LO}	"A" lo-side output. Swings from V_{SS} to V_{DD}.
7	IN_A	Digital input for the "A" drivers. Its polarity is non-inverting with respect to the "A" outputs.
8	D_{SETHI}	Connection for the delay setting resistor. This pin must be connected externally to the D_{SETLO} pin. This pin is connected internally to a PMOS diode referenced to V_{DD}.
9	R_{BP}	Internal circuit connection. This pin swings from V_{SS} to V_{DD}. It is in phase with IN_B. Normally this pin should be unconnected to any external circuitry.
10	LX_B	Negative supply for the "B" hi-side driver.
11	B_{HI}	"B" hi-side output. Swings from LX_B to V_{HIB}.
12	V_{HIB}	Positive supply for the "B" hi-side driver.
13	R_{BM}	Internal circuit connection. This pin swings from V_{SS} to V_{DD}. It is out of phase with IN_B. Normally this pin should be unconnected to any external circuitry.
14	V_{SS}	Negative supply for lo-side circuitry.
15	R_{AP}	Internal circuit connection. This pin swings from V_{SS} to V_{DD}. It is in phase with IN_A. Normally this pin should be unconnected to any external circuitry.
16	LX_A	Negative supply for the "A" hi-side driver.
17	A_{HI}	"A" hi-side output. Swings from LX_A to V_{HIA}.
18	V_{HIA}	Positive supply for the "A" hi-side driver.

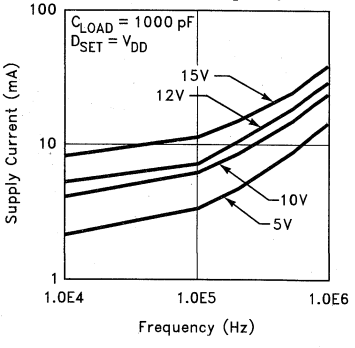
Typical Performance Curves

Quiescent Supply Current vs Supply Current



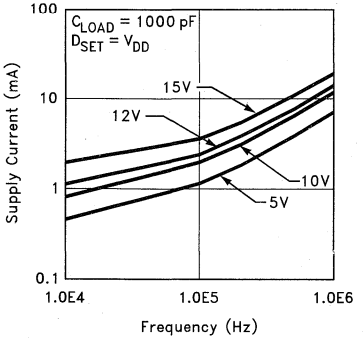
7661-3

Average Supply Curent into V_{DD} vs Voltage and Frequency



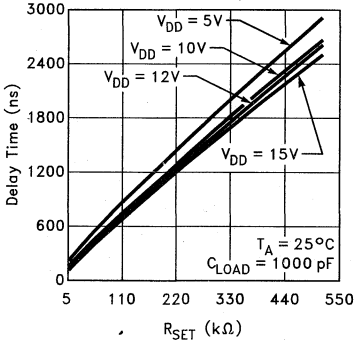
7661-4

Average Supply Curent into V_{HI} vs Voltage and Frequency



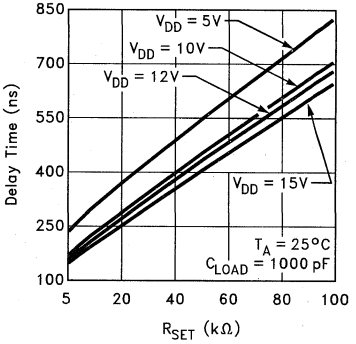
7661-5

Output Rising Edge Delay vs R_{SET} and Supply Voltage



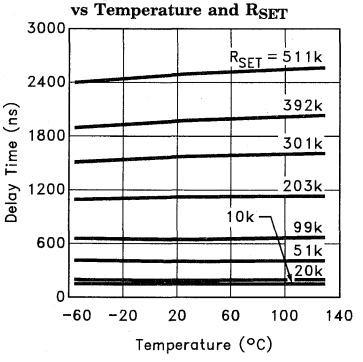
7661-6

Output Rising Edge Delay vs R_{SET} and Supply Voltage (Detail)



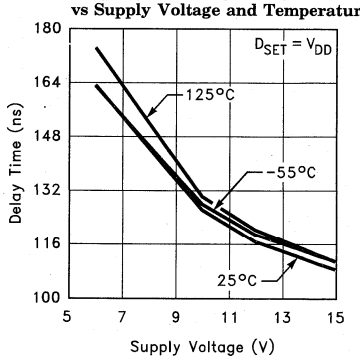
7661-7

Output Rising Edge Delay vs Temperature and R_{SET}



7661-8

Output Falling Edge Delay vs Supply Voltage and Temperature

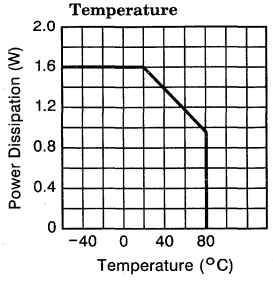


7661-9

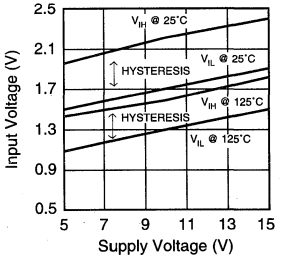
EL7661C
100V Full Bridge Driver

Typical Performance Curves — Contd.

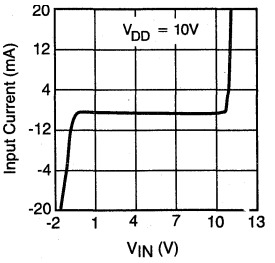
Power Dissipation vs Temperature



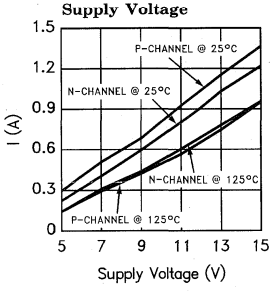
Input Threshold vs Supply Voltage



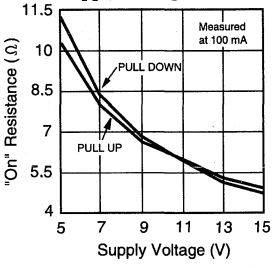
Input Current vs Input Voltage



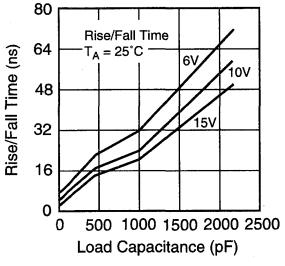
Peak Drive vs Supply Voltage



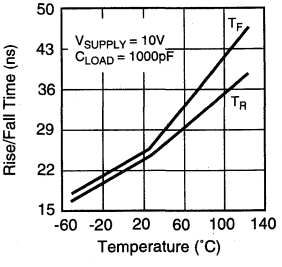
"On" Resistance vs Supply Voltage



Rise/Fall Time vs Load and Supply



Rise/Fall Time vs Temperature



7661-10

Theory of Operation

The EL7661 consists of, among other things, 4 CMOS super inverter output stages. The super inverter configuration minimizes the possibility of simultaneous conduction of the two output complementary MOS devices. Each output stage can source or sink up to 1 amp of peak current. The state of the two output stages denoted "A_{LO}" and "A_{HI}" is determined by the input "IN_A". In a like manner the state of the two output stages denoted "B_{LO}" and "B_{HI}" is determined by the input "IN_B". The lo-side output stages, "A_{LO}" and "B_{LO}" have V_{SS} as their negative supply and V_{DD} as their positive supply. The negative supply of the "A_{HI}" output stage is LX_A. The positive supply of the "A_{HI}" output stage is V_{HIA}. Similarly, the positive and negative supplies of the "B_{HI}" output stage are denoted V_{HIB} and LX_B. The hi-side supplies, LX_A, LX_B, V_{HIA}, and V_{HIB} can float with respect to V_{SS}. In fact the hi-side supplies can easily be 100V higher than V_{SS}. However, the differential voltage between V_{HIA} and LX_A, and between V_{HIB} and LX_B, should never exceed 15V.

The input signals, IN_A and IN_B, are level shifted from their quasi TTL levels to V_{SS} to V_{DD} voltages. After the level shift stage the rising edge of the signal is delayed some amount determined by the value of the resistor at the D_{SET} pin. (The falling edge of the signal has no extra delay added to it at this stage.) The delayed signal then drives its respective output drivers. The signals which drive the hi-side drivers are level shifted up to the appropriate levels while the signals which drive the lo-side drivers have an additional delay added to mimic the delay inherent in the hi-side level shift circuitry.

The circuitry which produces the resistor controlled delay of the rising edge of the output reduces down to a simple RC time constant. The R is provided by the user and the C is built into the delay circuitry. Ideally the delay would have no dependency on supply voltage or temperature since the R and C are well controlled, however, due to nonidealities of the exact implementation, the delay times are a weak function of supply voltage and temperature.

EL7661C
100V Full Bridge Driver

Macromodel

```
****EL7661 model****
*** top level circuit starts here ***
*                    a-input
*                    |       b-input
*                    |       |       a lo-side output
*                    |       |       |       b lo-side output
*                    |       |       |       |       a hi-side output
*                    |       |       |       |       |       b hi-side output
*                    |       |       |       |       |       |       a hi-side neg supply
*                    |       |       |       |       |       |       |       b hi-side neg supply
*                    |       |       |       |       |       |       |       |       lo-side neg supply
*                    |       |       |       |       |       |       |       |       |       a hi-side pos supply
*                    |       |       |       |       |       |       |       |       |       |       b hi-side pos supply
*                    |       |       |       |       |       |       |       |       |       |       |       lo-side pos supply
*                    |       |       |       |       |       |       |       |       |       |       |       |
.subckt M7661        ina     inb     alo     blo     ahi     bhi     lxa     lxb     vss     vhia    vhib    vdd
****top level subcircuit calls****
xdela ina outa vss delay
xdelb inb outb vss delay
xalo alo outa vdd vss vss outstg
xblo blo outb vdd vss vss outstg
xahi ahi outa vhia lxa vss outstg
xbhi bhi outb vhib lxb vss outstg
.ends M7661
****put in value of rset resistor here****
.param rset=50e3
****comparator subcircuit****
.subckt comp10 out inp inm vss
el out vss table {(v(inp)-v(inm))*5000} (0,0,15,15)
rout out vss 10meg
rinp inp vss 10meg
rinm inm vss 10meg
.ends comp10
```

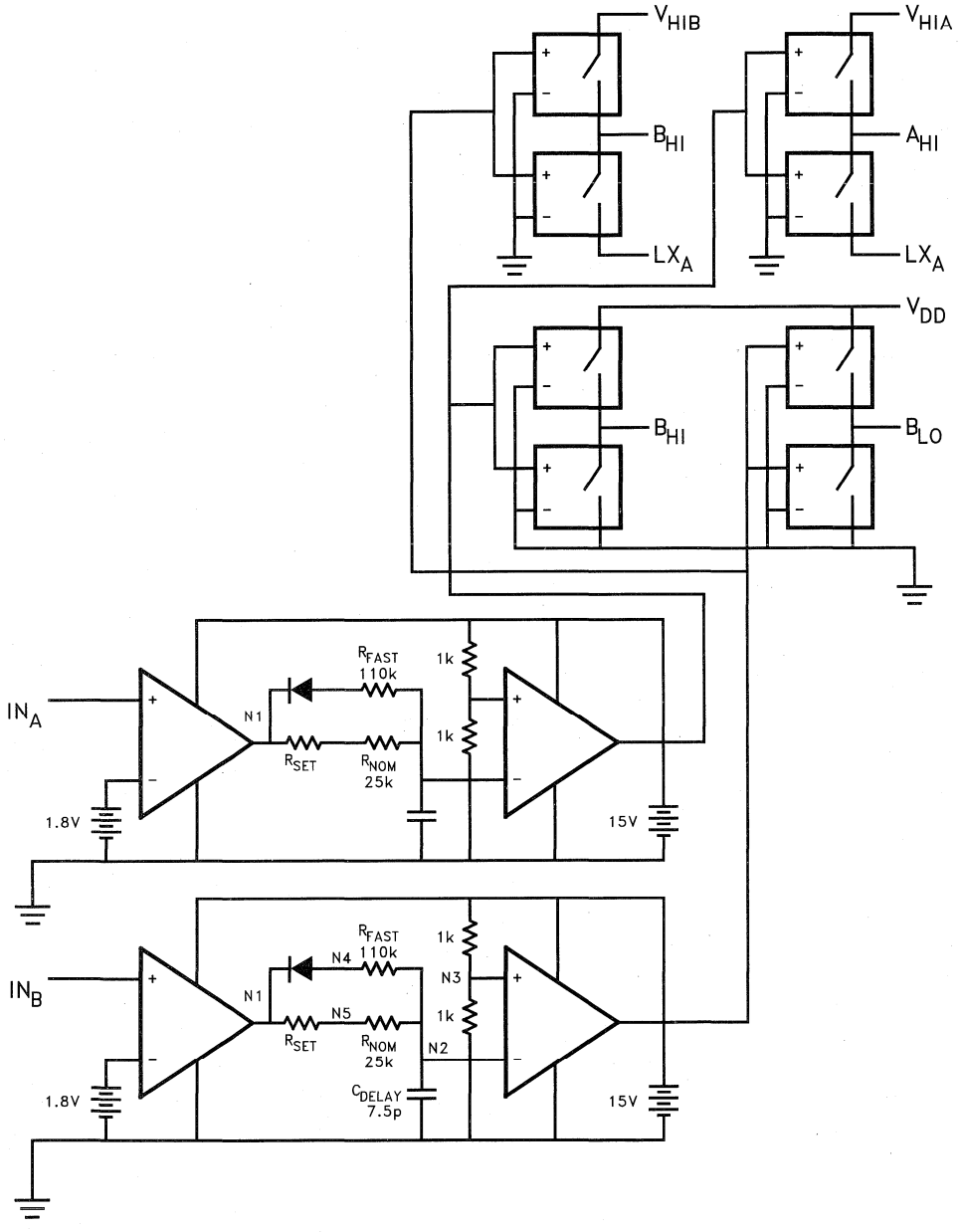
Macromodel — Contd.

****input, delay, and level shift subcircuit****
.subckt delay vin compout vss
vinref vinref vss 1.8
x1 n1 vin vinref vss comp10
rslow n1 n5 {rset}
rnom n5 n2 25k
cdelay n2 vss 7.5p
ddelay n4 n1 modd
rfast n4 n2 110k
rdiv1 vddint n3 1k
rdiv2 n3 vss 1k
x2 compout n3 n2 vss comp10
vddint vddint vss 15
.model modd d is = 1e-7
.ends delay
****5 ohm output stage subcircuit****
.subckt outstg out gate vhi lx vss
sp vhi out gate vss spmod
sn out 1x gate vss snmod
.model spmod vswitch ron = 5 roff = 2meg von = 2.5 voff = 4.5
.model snmod vswitch ron = 5 roff = 2meg von = 7.5 voff = 5.5
.ends outstg

EL7661C
100V Full Bridge Driver

Macromodel — Contd.

EL7661 Macromodel Schematic



Application Notes

élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

A Low-Noise Variable Gain Control

by Barry Harvey

The EL2082 current-mode variable gain control IC can be connected in a way to minimize circuit noise. In the usual forward configuration, the circuit has an 80 nV/$\sqrt{\text{Hz}}$ input noise which is constant with respect to gain adjustment. The circuit to be shown has an effective input noise which reduces as adjusted gain is increased. The circuit is useful in AGC or leveling functions where a relatively constant output amplitude is required for a range of inputs.

Figure 1 shows the schematic of the configuration. The EL2082 provides an output current equal to V_{GAIN}/1V times the input current. The output impedance of the EL2082 is in the megohm range and the input impedance is about 90Ω, and the part behaves as a current conveyor with adjustable gain. In essence, the EL2082 causes R_{FV} to behave as a variable feedback resistor, and in parallel with R_{FF} controls the gain of the circuit.

With V_{GAIN} = 0, the circuit gain is $-R_{FF}/R_{IN}$, and the noise of the EL2082 is gained to zero. In this mode, the circuit gain is maximum and input noise is determined by the op-amp alone. With V_{GAIN} = 1V, the circuit gain is $-(R_{FF}/R_{FV})/R_{IN}$, and EL2082 noise mixes with op-amp noise. For the maximum value of V_{GAIN} = 2V, the EL2082 dominates the feedback signal and gain is minimum while output noise is increased.

The op-amp must be a current-feedback type for the circuit to work. The CMF amplifier's low-input impedance prevents capacitance at the −input from causing a feedback pole and drastically limiting potential bandwidth. On the other hand, since the time delay of the EL2082 is inside the R_{FV} feedback loop, R_{FV} is a rather high value and must be adjusted to prevent excessive peaking or oscillation when V_{GAIN} = 2V. R_{FF} is set to control the maximum gain when V_{GAIN} = 0. For the values shown, the output can swing ±2V for 0.25% distortion, and the maximum swing is ±4V.

The input noise is successfully reduced by the circuit when small inputs require higher gain, as shown in Figure 2. The constancy of bandwidth and peaking and gain range are the tradeoffs. Here is a table of measured values:

V_{GAIN}	A_V	BW, −3 dB	Peaking	Input Noise
0	9.03	11 MHz	None	8.7 nV/$\sqrt{\text{Hz}}$
0.5V	5.41	26 MHz	None	19 nV/$\sqrt{\text{Hz}}$
1.0V	3.91	58 MHz	None	33 nV/$\sqrt{\text{Hz}}$
1.5V	3.11	75 MHz	2.2 dB	42 nV/$\sqrt{\text{Hz}}$
2.0V	2.62	80 MHz	5.5 dB	57 nV/$\sqrt{\text{Hz}}$

A Low-Noise Variable Gain Control

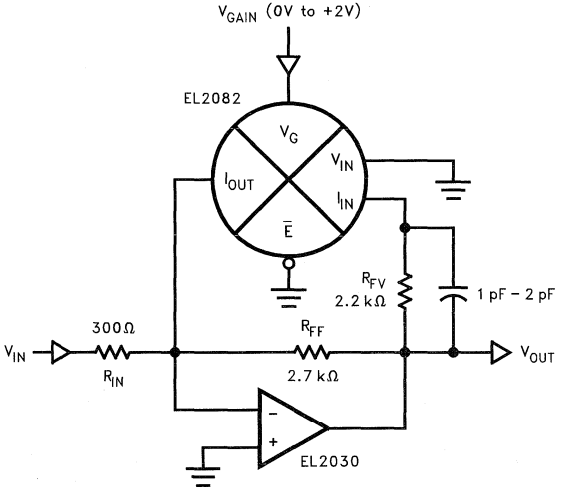


Figure 1

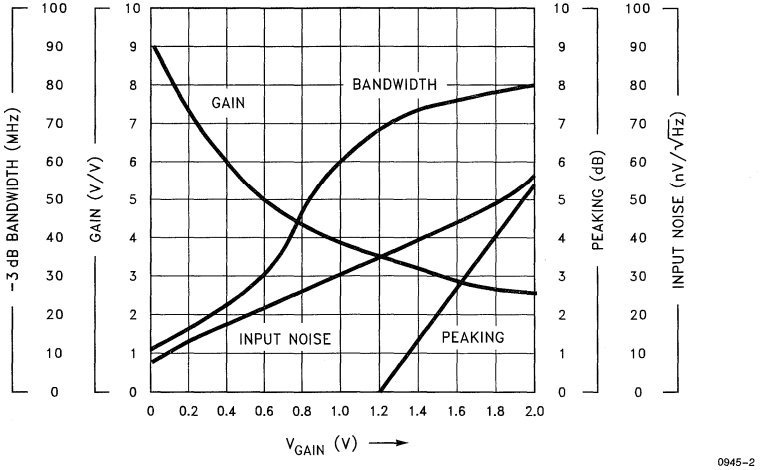


Figure 2

Thermal Considerations of the SO-8

by Barry Siegel

The world owes Phillips and Signetics a great debt in introducing the SO package. It offers a very small footprint, low cost, reliable, surface mounting package demanded by today's high density systems. However, since the thermal impedance of any package is, to the first order, inversely proportional to its area, the SO-8 imposes severe restrictions on the allowable power dissipation of the package. As pointed out in Reference (1), power dissipation raises the die junction temperature, and system reliability may be degraded. This brief sets forth a practical design method to ascertain what, if any, restrictions have to be placed on operating a linear IC in the SO package.

Analysis

Probably the best place to begin is to establish at what junction temperature a given device will be allowed to operate. Most manufacturers rate their junctions at a maximum of 150°C in plastic packages, but for reasons of reliability, a lower number may be mandated. The datasheet usually stipulates θ_{JA}, the thermal impedance from junction to ambient, and the difference between the maximum junction temperature we will allow and the maximum ambient temperature stipulates the thermal budget that we have or the junction temperature rise:

$$Pt = \frac{T_J(max) - T_A(max)}{\theta_{JA}} \qquad (1)$$

where:

Pt = Total Power Dissipated by the Device
$T_J(max)$ = Maximum Junction Temperature
$T_A(max)$ = Maximum Ambient Temperature

Power dissipation is comprised of two parts—Pq, the power dissipated by the device due simply to its supply current, and Pl, the power dissipated by the chip as a consequence of driving a load. In general, Pq is independent of Pl and vice versa, so an analysis can be made of each case and the results simply added together to obtain Pt.

The analysis should start with Pq since it is straightforward, and if $T_J(max)$ is exceeded under quiescent conditions, an alternate strategy is dictated. A word of caution, however, is in order. There are devices such as the EL2001 Unity Gain Buffer that draw a supply current of 1 mA but are capable of driving 100 mA loads. Clearly, in this case, power dissipation will be dominated by Pl. As a case in point, we might examine the EL2120 100 MHz CFA. Its quiescent supply current is specified as 20 mA. A typical video application is to use ±10V power supplies with 150Ω load driven to 8V peak-to-peak with an ambient temperature of 50°C. Under these conditions, Pq is equal to 400 mW, and using the datasheet value of 175°C/W for θ_{JA}, we obtain an average value for T_J of 120°C. What this tells us is that in order to keep the junction below 150°, the junction rise due to driving a load must be under 30°C.

Thermal Considerations of the SO-8

If we assume a steady state (sinusoidal) output voltage of 4V, the power dissipated in the EL2021's output transistor, Pl, would be:

$$Pl = (V+ - V_{OUT})(I_{OUT}) \quad (2)$$

Where:

$$I_{OUT} = \frac{V_{OUT}}{R_L'}$$

$$R_L' = R_L \parallel R_F$$

The recommended feedback resistor for the EL2120 is typically 300Ω, and for an inverter, R_F is indeed in parallel with R_L. For our particular case, Pl is equal to 240 mW, and the additional increase in junction temperature is 42°C exceeding our earlier requirement of limiting the load incurred junction rise to less than 30° and putting the junction at an average of 162°C.

In the final analysis, either the supply voltages have to be reduced or the load decreased to maintain the junction temperature below 150°. Our best advice is to approach the problem carefully, do the Pq "spot check" first, and verify the conditions with the vendor's applications department.

References

1. "Reliability and the Electronic Engineer" by Barry Siegel, paper given at the EE Times Analog conference, October, 1991
2. "A Simple Method for Characterizing Hybrid Package Thermal Impedances" by Steve Ott and Barry Siegel, *Hybrid Circuit Technology*, June, 1990

DC Restored 100 MHz Current Feedback Video Amplifier

by John Lidgey and Chris Toumazou

Summary

The EL2090 is an extremely versatile video amplifier with an integral on-board DC loop amplifier and sample-hold control circuitry. It is the first complete DC-restored monolithic video amplifier subsystem. It uses a current-feedback video amplifier with a nulling sample and hold amplifier specifically designed to stabilize video performance. This application note includes a video signal restorer with some fundamentals about DC restoration. As an application circuit of the EL2090, a x2 gain video amplifier is described together with a full evaluation circuit and double sided pc-board artwork. The EL2090 is a high-speed part, and some useful tips on layout have been included.

Although DC restoration is not a new concept, the high slew-rate, fast settling-time and low phase distortion at high frequencies provided by Elantec's family of monolithic current-feedback amplifiers, make CFAs the most attractive video amplifier choice for this application.

Video Signal Refresher

Figure 1 is a typical composite video signal which has a standard distribution level of 1V peak-to-peak into 75Ω, and comprises several sections. The video signal is the part containing the visible picture information, with a maximum amplitude between black and white of 0.7V. At the end of the picture information is the front-porch followed by a −0.3V of sync pulse, which is regenerated to provide system synchronization. The back porch is the part of the signal that represents the black or blanking level. In color NTSC systems the chroma or color burst signal is added to the back porch, normally occupying 9 cycles of 3.58 MHz subcarrier (4.43 MHz for PAL systems).

Video signals are often AC coupled to avoid DC bias interaction between different systems. The blanking level of the composite video signal needs to be restored to an externally set DC voltage, which locks the video signal to a predetermined common reference level, ensuring consistency in the picture displayed. This DC reference voltage V_R, sets and controls the picture brightness. The fundamental objective of the DC restore system is to force the DC baseline from the video amplifier to equal the externally set reference voltage V_R.

Figure 2 shows the schematic of a classical DC control servo system.

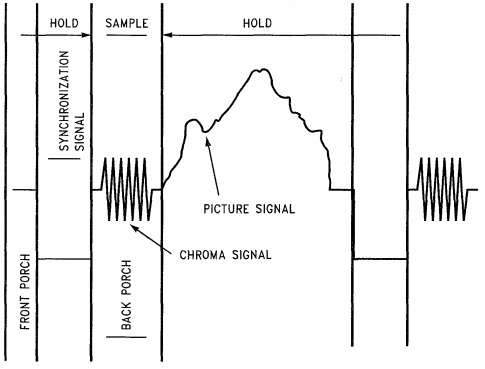


Figure 1. Video Signal

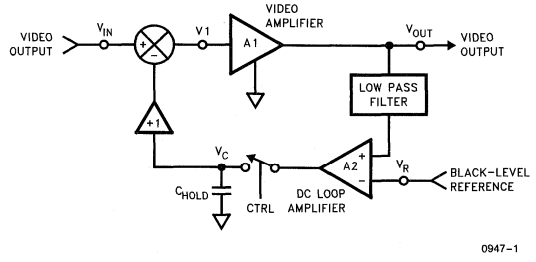


Figure 2. Classical DC Control Servo

DC Restored 100 MHz Current Feedback Video Amplifier

Video Signal Refresher — Contd.

The sync pulse is used to drive the control switch so that the DC servo loop is closed during the back porch of the video signal. The low pass filter removes the chroma burst. Operation of the DC loop is best understood by considering the voltage, V_C, across the hold capacitor, C_{HOLD}. During the back porch sample period, the switch is closed and the hold capacitor charges up. It can be shown from the loop dynamics that,

$$V_C = V_{BP} - V_{BP}/[A_1{}^*A_2] - V_R/A_1$$

where V_{BP} is the average back porch voltage for the sample period.

The net result is that $V_{OUT} = V_R - V_{BP}/A_2$, which shows that the output is clamped to V_R with an offset term of $-V_{BP}/A_2$. This offset is clearly small with a high gain DC loop amplifier, A_2. The EL2090 has a DC loop amplifier gain of 15 kV/V, reducing this offset to the order of a few millivolts. During the hold period the switch is open and the stored DC value of V_C is now subtracted from the incoming video signal, making

$$V_1 = V_{IN} - V_{BP} + V_R/A_1$$

and so

$$V_{OUT} = A_1 [V_{IN} - V_{BP}] + V_R$$

which effectively sets the back porch to V_R and the video signal is amplified by the forward amplifier with gain, A_1.

Subcircuits

The EL2090 DC restored amplifier is a 14-pin monolithic version of the circuit shown in Figure 2. The video amplifier, A_1, is a 100 MHz current feedback amplifier or CFA. These devices offer very high speed performance with excellent differential gain and phase. In many respects the CFA behaves as a conventional op-amp, but there are several key differences that must be considered by the user. In particular the two input impedances of the amplifier are different. The non-inverting input is high impedance and the inverting low impedance. However, the special feature of the CFA is that when in closed loop, the feedback current is determined by resistor, R_F, which controls the bandwidth of the amplifier independently of the gain setting resistor R_G.

The current feedback amplifier is essentially a transimpedance amplifier with an input voltage buffer to create a high input impedance non-inverting input. The transimpedance amplifier is formed by mirroring the output current of the input unity gain buffer into a high impedance internal Z-node and buffering this Z-node voltage through a low impedance output, as shown schematically in Figure 3 below.

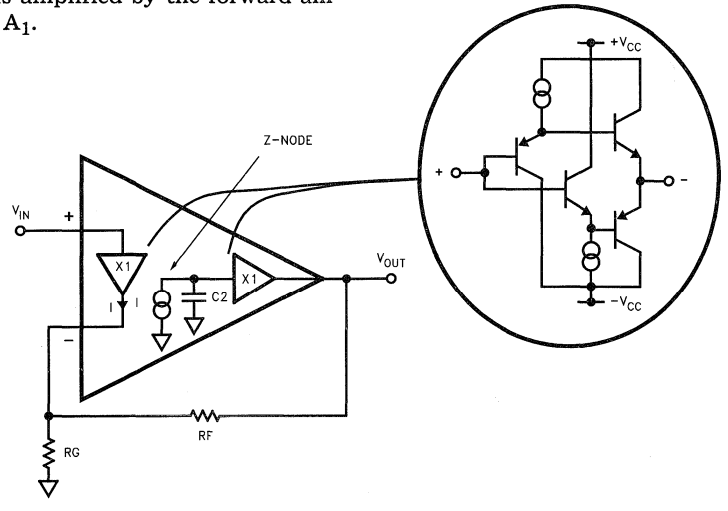


Figure 3. The Current-Feedback Amplifier

Subcircuits — Contd.

The unity gain buffers are a complementary class-AB common-collector stage, with DC current biasing. The slew-rate of the CFA is excellent due to the non-current-limiting input stage. The CFA has only one internal high impedance node (Z), so it is essentially a single pole dominant amplifier. Since the inverting input terminal is the output terminal of a voltage buffer, it is a low impedance point and the feedback signal is current. Intuitively one can see that in closed loop the feedback current through R_F supplies the current demanded by R_G and the input error current into the inverting input terminal. It is this feedback current component of R_F which is used to charge the compensation capacitance at the Z-node. Theoretically it can be shown that the −3 dB bandwidth is approximately,

$$f - 3\,dB = 1/[2\pi R_F C_Z]$$

where C_Z is the compensation capacitance of the Z-node. However, as for conventional op-amps, the closed loop gain, A_1, is simply

$$A_1 = [1 + R_F/R_G],$$

and the −3 dB frequency can be controlled with R_F while the closed loop gain can be set independently with R_G.

Features of the EL2090

Elantec pioneered the development of monolithic CFAs. A first to the market with the CFA the established reputation is confirmed with the EL2090 which is the first monolithic DC restored video amplifier. The device is built with Elantec's fast proprietary complementary bipolar technology which yields NPN and PNP transistors with equivalent AC and DC performance.

The on-chip current-feedback ampifier is optimized for video performance, and since it is a current-feedback amplifier it ensures that the −3 dB bandwidth stays essentially constant for various closed-loop gains. The amplifier performs well at frequencies as high as 100 MHz when driving 75Ω. The sample and hold circuit is optimized for fast sync pulse response; the switch operates in only 40 ns. A particular feature of this sample and hold output buffer is its low output impedance which is fairly constant over frequency and load current. This provides good isolation and thus prevents the DC restore circuit from interfering with video amplifier performance through R_{AZ}.

Note that the burst output of Elantec's EL4581 and EL4583 sync separator chips can drive the Hold input of the 2090 directly.

Typical Application Circuit

Figure 4 shows a component level schematic diagram of the gain x2 DC restored video amplifier. The operation of the circuit is based upon the simple analysis given with the amplifier connected in the non-inverting mode of operation. The application circuit will restore the video DC level in ten scan lines, even if the hold pulse is as short as 2 μs long. The current-feedback resistor R_F of 300Ω will give a stable bandwidth of 115 MHz and all component values are chosen to maintain optimum speed and performance.

DC feedback resistor R_{AZ} is 2 kΩ and is sufficiently larger than R_F to provide reasonable isolation between the sample and hold circuit and video amplifier and thus avoid any video signal coupling back to the sample-hold. R_{AZ} may be (optionally) split into two 1 kΩ resistors and a 820 pF bypass capacitor to reduce unwanted transient feedthrough from the sample and hold to the video signal to less than about 1 mV seen at the amplifier's output. The circuit is designed to operate using ±15V supplies, but it can operate down to ±5V supplies by changing R_{AZ} and C_{AZ} values. Alternatively an inverting configuration video amplifier could be used with appropriate exchange of the input signals to the DC loop amplifier.

DC Restored 100 MHz Current Feedback Video Amplifier

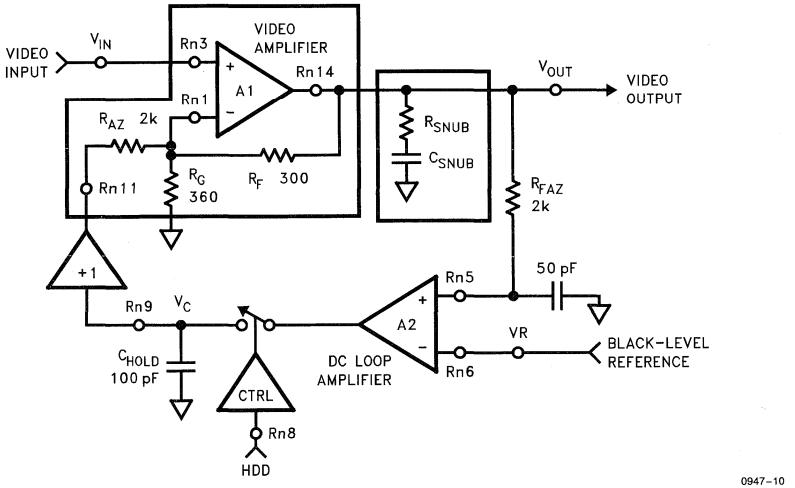


Figure 4. DC Restored Video Amplifier with $A_V = 2$

Design Procedures

1. Determining R_{AZ}

Ideally R_{AZ} should be large to provide good isolation between the sample and hold buffer and the video amplifier. This is because any video-induced current through R_{AZ} will cause changes in the buffer output impedance. A large series R_{AZ} will reduce the effect of buffer output impedance variations and thus preserve the differential gain error of the video amplifier. However, too large a value of R_{AZ} along with the output voltage compliance of the buffer will limit the maximum I_{AZ}, the DC correction current. A lower I_{AZ} will result in a lower restored reference level. Consequently, trade-offs have to be made between R_{AZ}, the maximum restored reference level, and the supply voltage which controls the output voltage compliance of the buffer. The following equations address some of the issues related to the trade-offs.

During the back-porch of the video signal, the sample and hold switch is closed. The servo loop charges C_{HOLD} to a voltage level necessary to bring the video amplifier output to the reference input level. The maximum voltage of C_{HOLD} is limited by the supply voltages.

$$V_{REF} = (V_{BP} * A_1) - V_{AZ}(R_F/R_{AZ}) \qquad (1)$$

where

V_{REF} is the new stabilized back-porch level at the output of the video amplifier.
V_{BP} is the input back-porch offset voltage at the video amplifier input
A_1 is the close loop gain of the video amplifier.

$$A_1 = R_F(1/R_{AZ} + 1/R_G) + 1 \qquad (2)$$

R_F is the feedback resistor of the current-feedback video amplifier. It is nominally 300Ω for $A_1 = +2$. In gain of +5 application, R_F should be decreased to 270Ω to maintain gain flatness.
V_{AZ} is the buffered C_{HOLD} voltage developed by the loop to maintain the output at the reference level.
V_{AZ} is limited to the supply rails less 2.5V.

$$-V_{SUPPLY} + 2.5V < V_{AZ} < +V_{SUPPLY} - 2.5V \qquad (3)$$

Analysis of equation (1) shows that since V_{BP}, A_1, and R_F values are established by system requirements, the maximum R_{AZ} is determined by V_{AZ} and V_{REF}. A high R_{AZ} value requires a proportionally high V_{AZ} voltage and low V_{ref}. Outside the back-porch period, the switch is opened. The DC offset is maintained.

2. Design Example

Below examples are intended to show how R_{AZ} changes under different supply voltages and reference level.

Example A.
$V_{SUPPLY} = \pm 15V$
$V_{REF} = 0V$
$A_1 = 2$
$V_{BP} = \pm 1V$
$R_F = 300\Omega$

Applying equation (3), the output voltage compliance V_{AZ} of the sample and hold buffer can be calculated,
$-12.5V \leq V_{AZ} \leq 12.5V$
Using equation (1), $R_{AZ} = 1.8\ k\Omega$ for $V_{BP} = \pm 1V$.
Once R_{AZ} is determined, equation (2) gives $R_G = 360\Omega$.

Example B.
$V_{SUPPLY} = \pm 5V$
$V_{REF} = 0V$
$A_1 = 2$
$V_{BP} = \pm 1V$

Applying equation (1), $R_{AZ} = 375\Omega$ for $V_{BP} = \pm 1V$.
Equation (2) gives $R_G = 1.5\ k\Omega$.

Example C.
$V_{SUPPLY} = \pm 15V$
$V_{REF} = 1$
$A_1 = 2$
$V_{BP} = \pm 1V$

Applying equation (3),
$-12.5V \leq V_{AZ} \leq 12.5V$
$R_F = 300\Omega$
Equation (1) gives
$R_{AZ} = 1.2\ k\Omega$ for $V_{BP} = -1V$
$R_{AZ} = 3.75\ k\Omega$ for $V_{BP} = -1V$
Therefore, $R_{AZ} = 1.2\ k\Omega$
Using equation (2), $R_G = 400\Omega$.

The above examples demonstrate the trade-off between the supply voltage, R_{AZ}, and the reference level. Examples A and B reveal that a lower supply voltage requires a lower R_{AZ}. Examples A and C show that when the supply rails are kept constant, a higher reference level requires a lower R_{AZ}.

3. Determine C_{HOLD}

Fast acquisition time is achieved with small values of C_{HOLD}, but this degrades droop performance. For video the droop needs to be better than ½ IRE in one horizontal line, or less than 3.5 mV in 45 μs for NTSC. The droop is primarily caused by C_{HOLD} voltage decaying. Since the droop of C_{HOLD} is amplified to the output by the ratio R_F/R_{AZ} then C_{HOLD} must be chosen to satisfy $dV_C/dt < 3.5\ mV/45\mu s$ multiply $R_{AZ}/R_F = 510\ V/\mu s$

$R_F = 510V/\mu s$.

Since $dVC/dt = I_{DROOP}/C_{HOLD}$, and the discharge current I_{DROOP} is a maximum of 50 nA, then

$C_{HOLD} \bullet 98$ pF, or 100 pF, the nearest preferred value.

If R_{AZ} is decreased for lower supply operation, C_{AZ} is correspondingly increased to preserve droop and acquisition characteristics.

4. Acquisition Time

Based on the values shown in Figure 4 the acquisition time is approximately 20μs. Note that it will take 10 chroma-burst of 2μs each to finish settling from a Δ1.0V input signal shift.

Evaluation Printed Circuit Board

A component layout of the application circuit is shown in Figure 5(b) with some additional features.

- V_{REF} is applied externally to the grounded resistor R_{14}, which is decoupled with capacitor C_{11}.
- Optional 75Ω termination resistor has been included at the input and output.
- Built in guard ring on PCB board layout (Figure 5(b)) ensures that leakage from the hold capacitor is minimal to improve droop performance. The guard ring is connected to the S/H Out. The hold capacitor should be low leakage and so mica or mylar capacitors are recommended here.

DC Restored 100 MHz Current Feedback Video Amplifier

Evaluation Printed Circuit Board — Contd.

- Diode clamp circuit to overcome lock-up has been included on board.
- Optional AC input coupling capacitors of about 10 μF has been included.
- Optional snubber circuit has been included.
- Optional R-C low pass filter on hold input logic drive has been included should the logic signal require slowing down.

Printed Circuit Board and Layout Hints

Figure 5(a)–(d) on following pages, shows a component layout together with double sided pc-board. Ground plane is essential throughout to reduce parasitic inductance and stray pickup. Special precautions have been taken to avoid any discontinuity in ground plane since this will make the function of ground plane much less effective. Supply decoupling capacitors are kept close to the power supply pins to ensure good power supply integrity. The feedback path of the video amplifier should be kept as small as possible to avoid deterioration in high frequency gain accuracy. BNC connectors are included at the input and output.

R1 = 360Ω
R2 = 300Ω
R3 = 1 kΩ
R5 = 75Ω
R6 = 220Ω
R7 = 4.7 kΩ
R8 = 10 kΩ
R9 = 10 kΩ
R10 = 2 kΩ
R11 = 100Ω
R12 = 10 kΩ
R13 = 75Ω
R14 = 10 kΩ

C1 = 0.1 μF
C2 = 0.1 μF
C3 = 4.7 μF (Tant.)
C5 = 820 pF
C6 = 39 pF
C7 = 50 pF
C8 = 100 pF
C9 = 0.1 μF (Ceramic)
C10 = 4.7 μF (Tant., 25V)
C11 = 4.7 μF (Tant., 25V)
C12 = 30 pF
C13 = 0.1 μF (Ceramic)

POT1 = 10 kΩ
D1 = 1N914
D2 = ZN458B
D3 = ZN458B (2.45 V_{REF})

Figure 5(a). Component Values

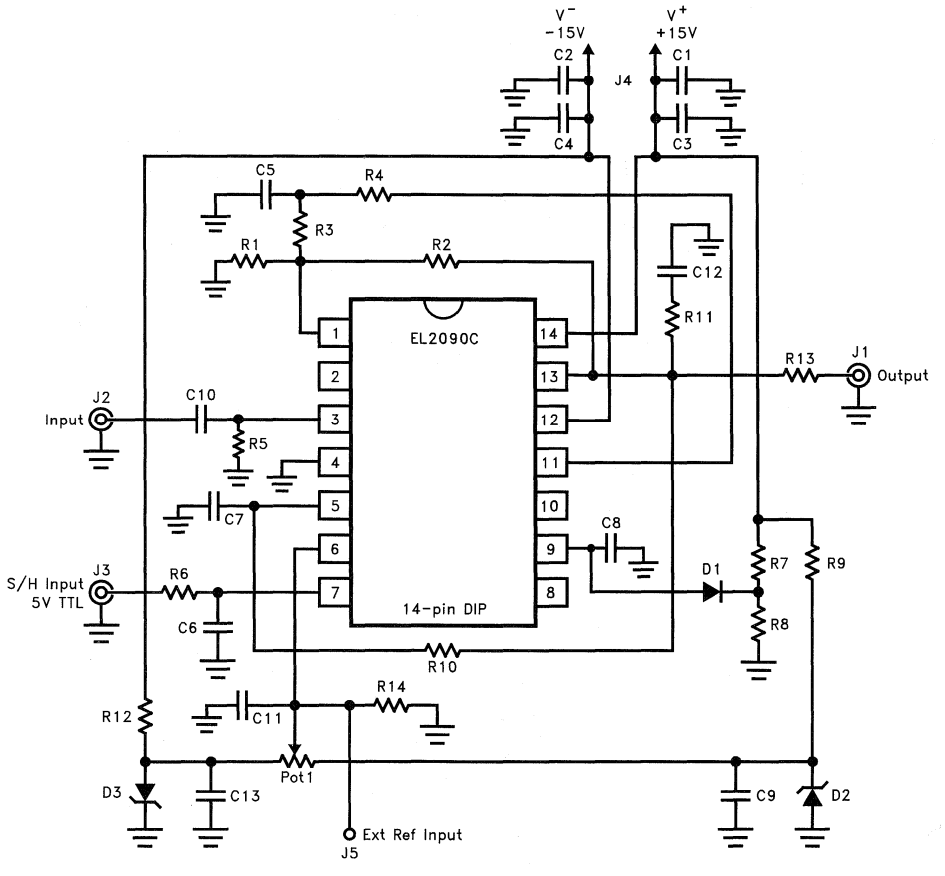

V⁻
-15V
V⁺
+15V
C2
C1
J4
C4
C3
C5
R4
R3
R1
R2
C12
R11
EL2090C
1
2
3
4
5
6
7
14
13
12
11
10
9
8
R13
J1
Output
J2
Input
C10
R5
C7
C8
J3
S/H Input
5V TTL
R6
D1
R7
R9
R8
C6
14-pin DIP
R10
R14
R12
C11
Pot1
D3
C13
C9
D2
Ext Ref Input
J5
0947-2

Figure 5(a)

DC Restored 100 MHz Current Feedback Video Amplifier

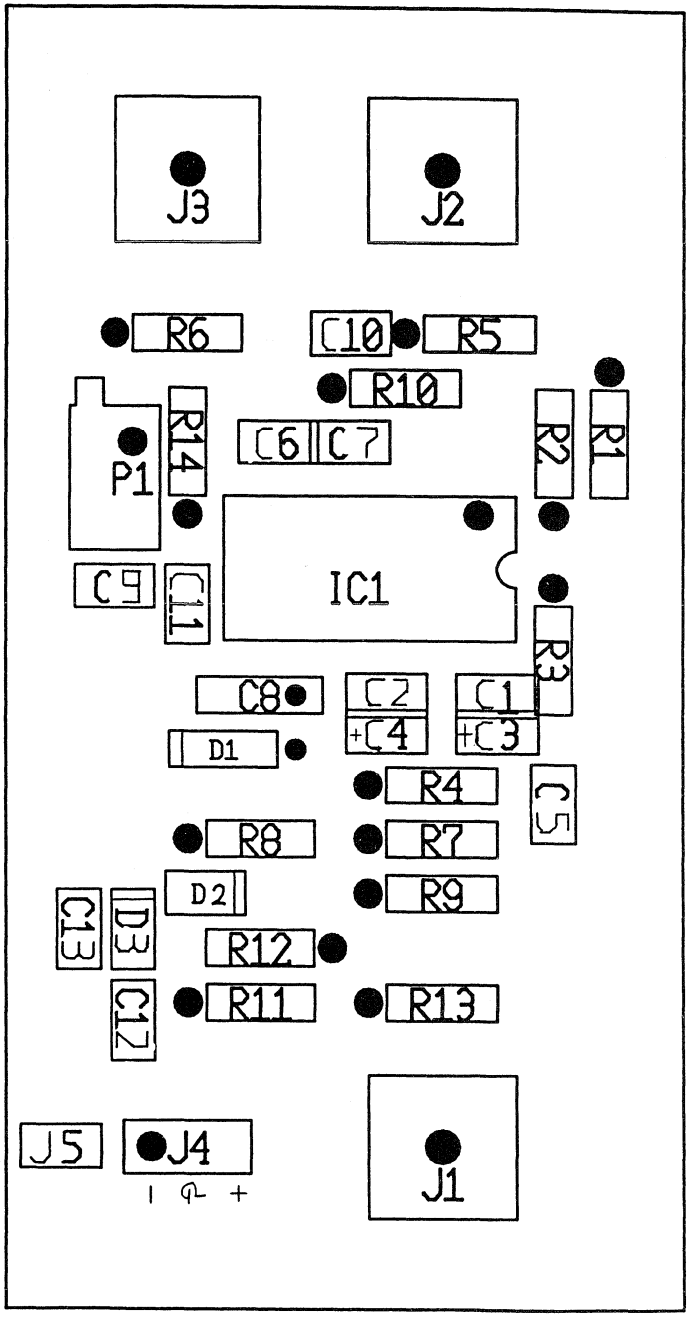


Figure 5(b)

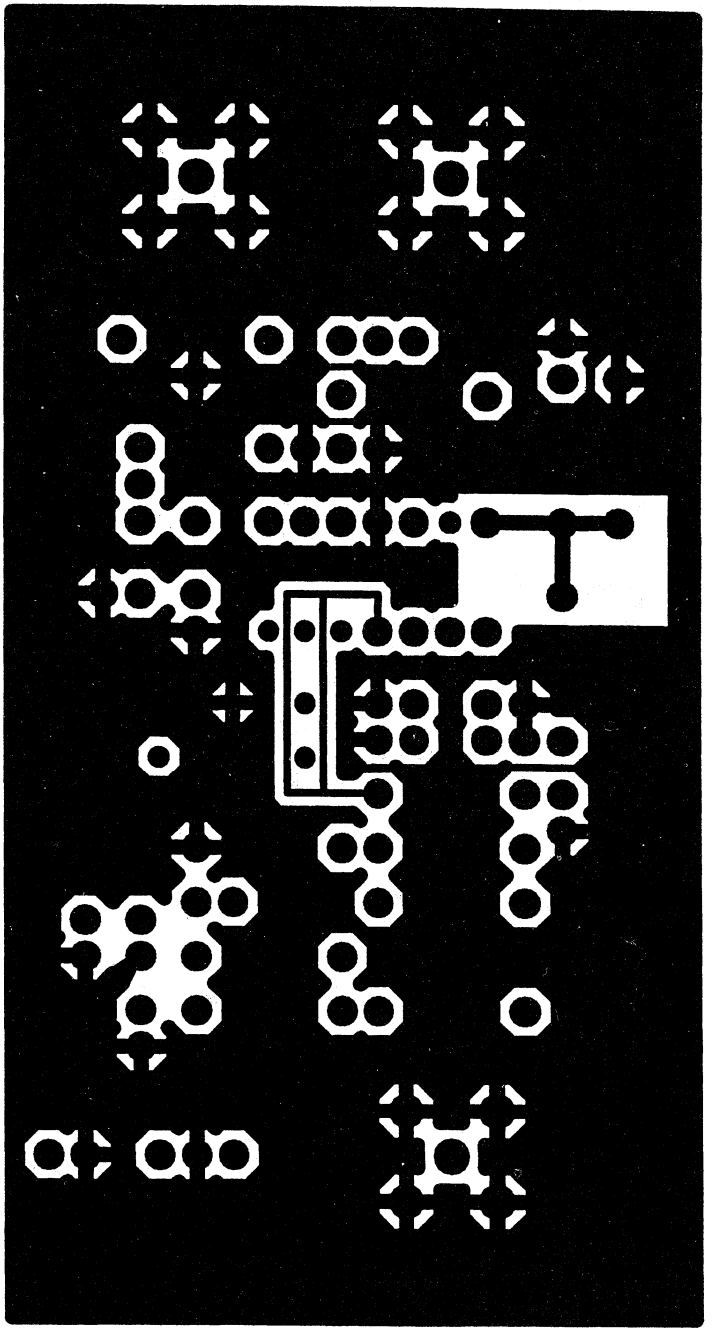


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Figure 5(c)

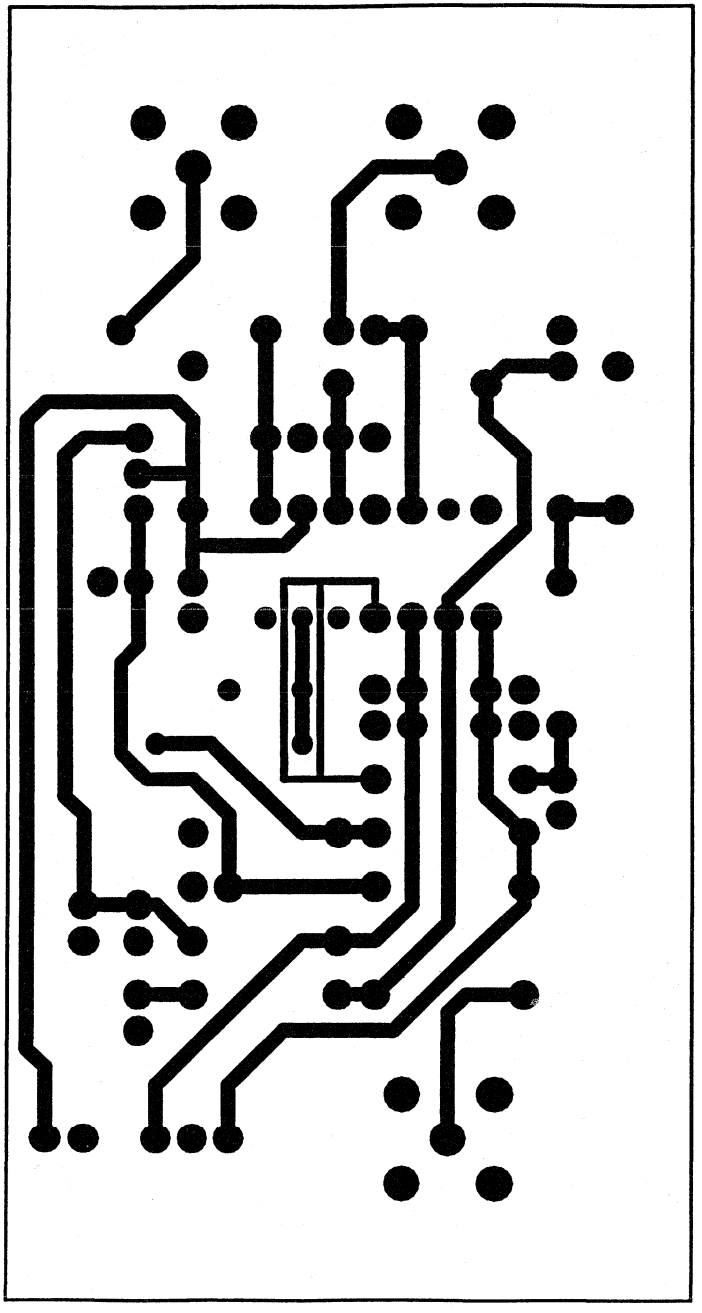

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Figure 5(d)

Do's and Don'ts

General Circuit Layout

As with all high frequency devices care must be taken with printed circuit board layout. Good ground plane construction is essential and DC power supply integrity must be ensured, so the power supply pins should be bypassed to ground with ceramic capacitors as close to the supply pins of the device as possible. The video current feedback amplifier is, like all CFAs, particularly sensitive to stray capacitance at the inverting input. This capacitance combined with the inverting node input resistance generates an additional high frequency pole in the feedback loop of the CFA leading to gain peaking in the response. Consequently pc-boards should be designed to keep lead lengths as short as possible around the inverting input node, with the ground plane positioned sufficiently far away to prevent this gain peaking effect.

Load Capacitance

In general load capacitance with negative feedback amplifiers causes gain peaking. This is because the load capacitance with the non-zero output resistance of the amplifier creates an additional pole in the feedback loop. The video CFA within the EL2090 is no exception to this and it may be necessary to add a series R-C snubber network to ground to minimize peaking, as shown in the data sheet, where the appropriate components are selected for a particular value of load capacitance.

Sample and Hold Section

Clock-feedthrough to C_{HOLD} leads to an undesirable hold-step, effecting the DC bias level.

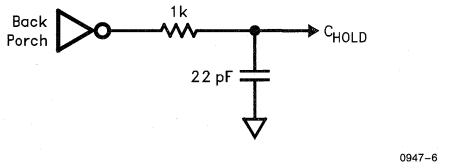


Figure 6

Increasing C_{HOLD} is the most direct way of reducing this effect. Under normal operation the loop amplifier only deals with a small correction to V_C and although increasing C_{HOLD} will compromise the slew-rate of the sample-hold section, this is not a practical limitation. However with $C_{HOLD} > 1$ nF and the sampling interval $t_S <$ 2 ms then on power up the device may lock-up if V_C approaches V_{CC}, causing the output transistors of the sample-hold amplifier to be taken out of their active region. The net result is that the lock-up does not self recover. Limiting V_C to V_{CC} − 3V using the external clamp circuit shown in Figure 4 prevents this lock-up condition from occuring.

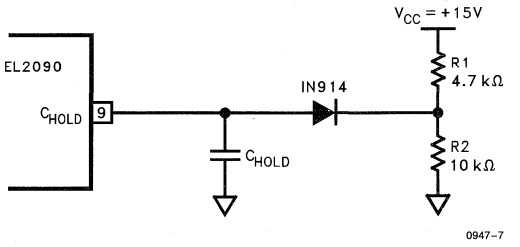


Figure 7

A Low Distortion Tuneable Sine Wave Oscillator

Summary of Performance Characteristics

One can make a low distortion tuneable oscillator by incorporating an active filter inside an AGC loop. With a control voltage V_G of 0.1 to 2V, one can obtain over a decade of tuning range, with oscillation frequencies from 200 kHz to 3 MHz in this particular design. Total Harmonic Distortion (THD) is -64.5 dB at $V_G = 1V$, and is kept below -57 dB over most of the tuning range. Modulation sidebands due to loop jitter are at least 50 dB down over the entire tuning range, with suppression approaching 56 dB for higher V_G. Linearity error for f_{OSC} vs. V_G is below 4%.

Theory of Operation

The active filter employed in this design is a state variable configuration with the EL2082 in the integrator path providing the frequency control; a circuit diagram of this filter is shown in Figure 1. The EL2082 is a current mode multiplier with low input impedance (95Ω nom) and current source output. It takes the current through the integrator resistor R_{IN}, scales it by a gain determined by V_G, then outputs the scaled signal current to the integrator capacitor C_F. In effect, we can modify the integrator time constants by adjusting V_G; the filter cutoff frequency is then given by

$$f_O = \frac{V_G}{1V} \frac{1}{2\pi (R_{IN} + 95\Omega) C_F}$$

This filter serves as the feedback network for the oscillator, a block diagram of which is shown in Figure 2. At frequency f_O, the filter phase is 0°, and if the feedback gain is ≥ 1, sustained oscillation will occur. To ensure startup, many oscillator designs have feedback gain >1, but then oscillation amplitude grows until nonlinearity sets in and reduces the loop gain down to 1, thus making it difficult to generate a pure sine wave. In this design, Automatic Gain Control (AGC) is used to maintain unity gain and stable oscillation amplitude. The AGC circuit consists of a 4-quadrant multiplier, which multiplies the output sine wave with itself to generate a DC and double frequency term. The high frequency term is filtered and the remaining DC voltage, which provides a measure of the output amplitude, is used to control the variable gain amplifier. This gain is continually adjusted to provide unity gain around the feedback loop.

Figure 3 shows a circuit diagram of this oscillator. The top part of the diagram is the tuneable active filter implemented using two EL2082s and a EL2444 quad op amp package. The output of this filter is fed back to its input via a unity gain buffer, obtained by connecting pins 11 and 14 of the EL4451 together. To compensate for filter losses, this output is also fed through the resistive divider R_1/R_2 into the variable gain amplifier of the EL4451. By setting the gain to just the right amount, we have unity gain in the feedback path and the necessary conditions for stable oscillation.

This adjustment is provided by an AGC, which consists of the EL4450 four quadrant multiplier and a filter to act as a RMS to DC converter. If the oscillation amplitude increases, the DC control voltage also increases to lower the gain of the EL4451 amplifier. The inverse can be said for oscillation amplitude that is too small. The loop will servo itself until the mean-square of the oscillation amplitude equals the reference voltage on pin 10 of the EL4450. This reference voltage can be changed by adjusting the potentiometer VR1.

Design Notes

Several issues were raised in this design, the first of which is the speed and stability of the AGC loop. A loop that is too slow, as was found early on, is not able to track the oscillation amplitudes; what results is a backlash phenonmenon where the loop is constantly over-correcting and never finds a stable operating point. On the other hand, a loop with too much bandwidth would allow excessive feedthrough, again destabilizing itself and distorting the output. A loop bandwidth of ~ 16 kHz has been found to be adequate for this design.

A Low Distortion Tuneable Sine Wave Oscillator

Referring to Figure 3, we see that the EL4450 provides a "pseudo" integrator in its output path; it is termed pseudo since it provides rolloff only until ~16 kHz, after which it becomes a unity gain element. To continue the rolloff after 16 kHz, we need an additional lowpass filter with a pole at the above frequency. Although this seems sound, we encountered loop instabilities with this implementation. By moving the pole of the lowpass filter above the "integrator zero", the loop is stabilized.

The residual loop jitter causes another problem: modulation noise. Small variations in the loop voltage that reach the GAIN− pin of the EL4451 modulates the gain and creates Amplitude Modulation (AM) in the output waveform. Although this modulation is small, it is observable on the spectrum analyzer as sidebands around the fundamental. To reduce these sidebands we lowered the feedback into the multiplier, set by R_1 and R_2. Since the loop voltage directly modulates this feedback, by lowering the feedback we also lower the modulated components.

Another problem is the limited Q provided by the active filter network. As opposed to a crystal or LC tuned circuits, we are limited to painfully low Q's in this filter. Since Q ≠ 1 unbalances the gain between filter stages, there is a practical limit to Q before the 2nd integrator is overdriven. Ideally we would like a high Q to reduce phase noise and to reduce the loop jitter. Unfortunately in this implementation, while Q > 1 does reduce modulation effects, it also increases the THD due to the gain unbalance mentioned earlier. In addition, a Q > 1 also introduces clipping problems in that during startup, the oscillator can swing to large amplitudes and clip, and the AGC has no hope of recovering from such an unhappy beginning. Hence, a Q = 1 was chosen for this design to provide reliable startup and lower THD.

As the frequency of operation increases, we see peaking in the active filter due to increased phase shifts through the op amp stages. Once the peaking causes the filter gain to exceed 0 dB at 0° filter phase, the AGC is no longer able to keep the feedback gain to 1, and clipping occurs in the oscillator output. For this reason it is recommended that the oscillation frequency be kept under 3.5 MHz. The range of operation in this design thus lies quite close to the upper limit. For those desiring lower frequencies of operation some recommended component values are given below:

Tuning Range	R_{in}	C_F	R_1	R_2	C_1	C_2
20 kHz–300 kHz	3k	330 pF	330	240	10 nF	10 nF
200 kHz–3 MHz	3k	33 pF	330	120	1 nF	1 nF

The current design runs on a supply of ±5V. It is possible to push the upper frequency limit to about 4 MHz by operating on ±12V supplies, provided that the current limiting resistor R_Z for the LM337 is raised to 2 kΩ.

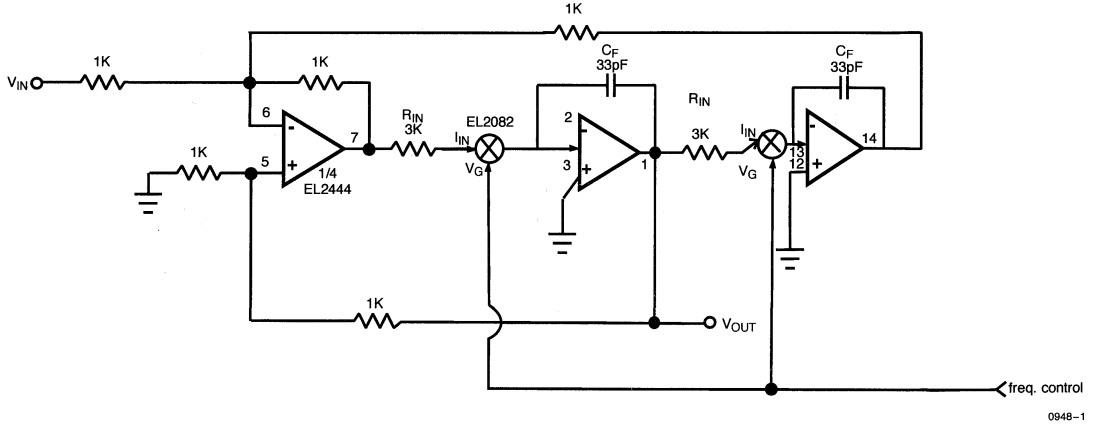


Figure 1

A Low Distortion Tuneable Sine Wave Oscillator

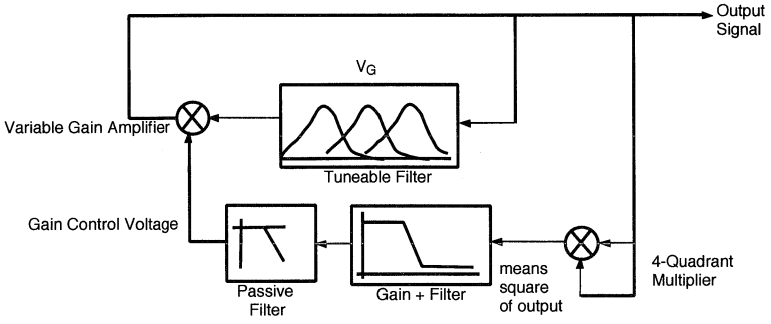


Figure 2

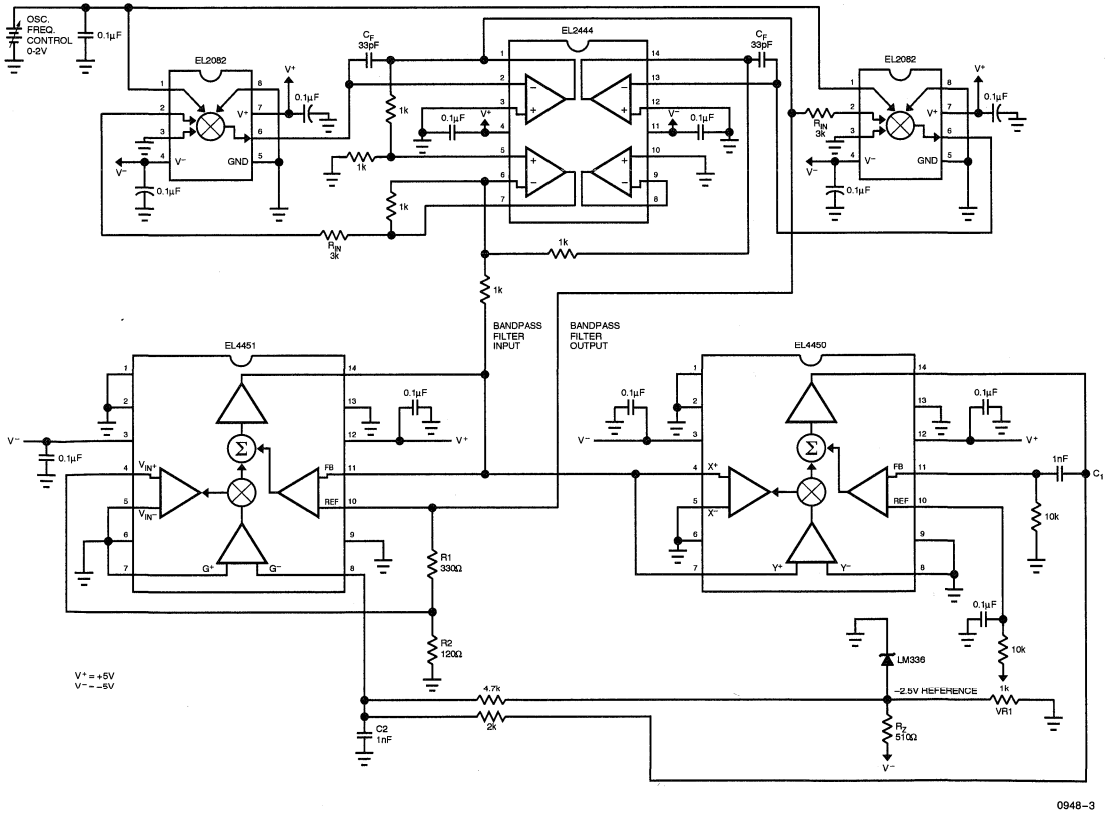
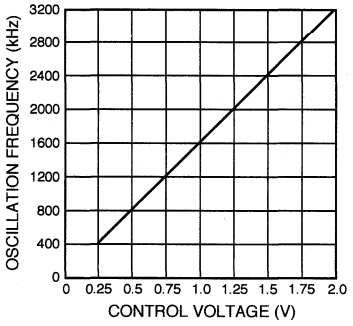


Figure 3

Typical Performance Curves



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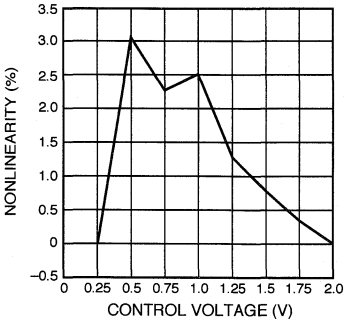

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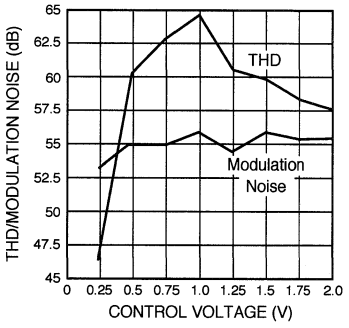


0948-6

6

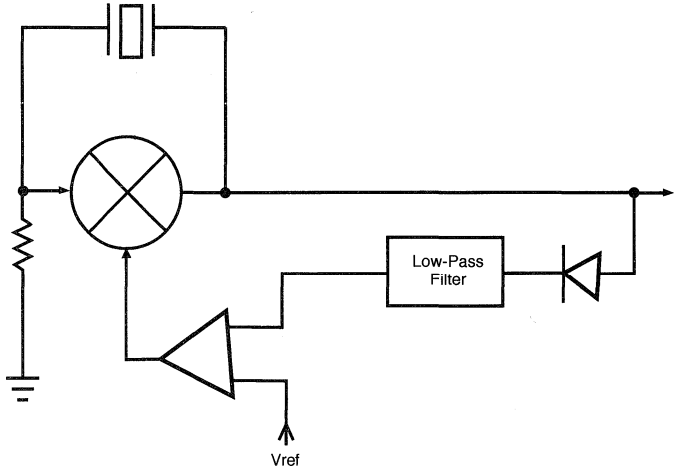
High-Purity Sinewave Oscillators With Amplitude Stabilization

by Barry Harvey

While a wide variety of circuits and components are used to generate sinewaves, it has always been a challenge to produce spectrally pure and regulated sines in circuits that require no tuning nor adjustments. This article shows a practical method of achieving these goals. The classic system architecture is shown below.

The crystal (or other frequency-selective network) provides the oscillation path around the multiplier or variable-gain amplifier. The multiplier's output is sampled by some amplitude detector, shown here as a rectifier diode. The DC output of the rectifier is filtered by a low-pass filter, and the output of that is compared to a DC reference voltage by the servo amplifier. The gained-up error is then used as the multiplier's gain-control input. The amplitude-control loop serves to set the oscillation path gain to just unity, so that the multiplier's output doesn't grow nor decay, and the loop also maintains oscillation amplitude within the linear range of all components. This gain-controlled oscillator is more complicated than simple overdriven circuits, but it produces very pure sinewaves and has no start-up problems.

Basic Stabilized Oscillator Loop



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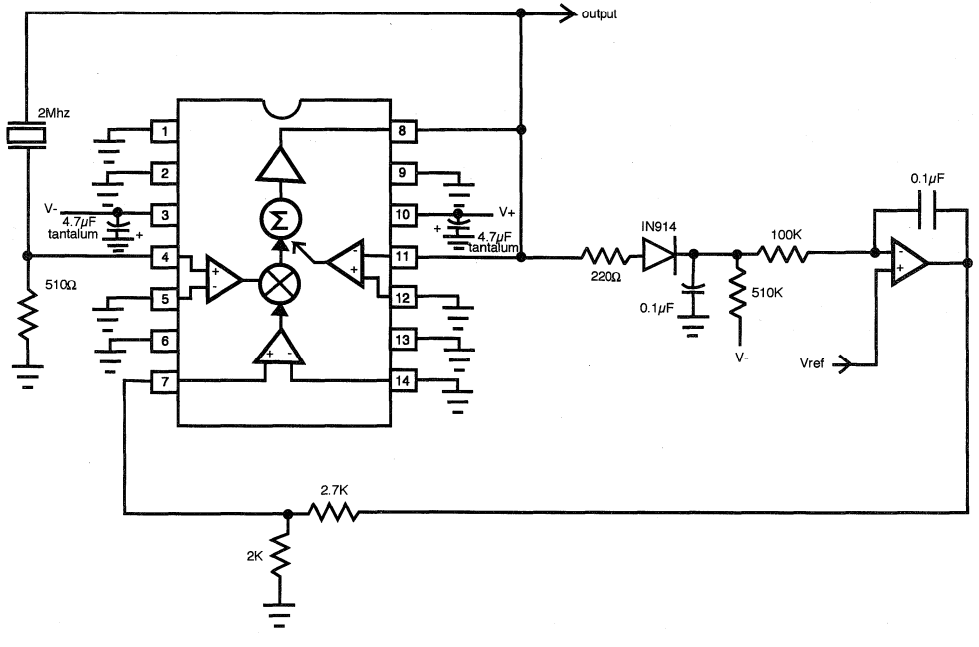
High-Purity Sinewave Oscillators with Amplitude Stabilization

Here is a realization using common components:

Basic Oscillator with Amplitude Stabilization Loop



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The EL4451 is a two-quadrant multiplier, whose gain-control input voltage of 0 ⟶ +2V produces a voltage gain of 0 to 2. The signal input receives a portion of the output signal passed through a series crystal. At resonance, the crystals impedance phase passes through 0° and positive feedback occurs around the multiplier. The crystal has a series resistance of about 100Ω, so with the crystals 510Ω load the multiplier will need to have a gain of 1.2 to sustain oscillation.

The output is rectified by a simple diode detector and compared to a reference voltage by an integrating op-amp. The integrators output is attenuated by the 2 kΩ and 2.7 kΩ resistors so it cannot overdrive the EL4451 gain-control input and cause nonlinear oscillations. The diode detector has a 220W resistor in series so as to not cause output distortions due to charging pulses. A pull-down current flows through the 510k resistor to allow proper rectification.

Any crystal, up to about 50 MHz fundamental mode resonance, can be used. Overtone crystals will require an added series-tuned circuit to force harmonic oscillation modes. The crystal and 510W resistor can be exchanged to put the crystal at ground, using the parallel resonance mode of the crystal.

This circuit generates −53 dBc harmonic distortion at 2 MHz with ±5V supplies and 1 Vrms output into 500Ω. This is mostly due to the output stage nonlinearities of the EL4451, and it drops to −60 dBc at ±12V supplies. Reducing the output amplitude further improves distortion levels, although the simple diode detector requires a minimum 0.5 Vrms level. Sideband noise is excellent, spanning only 14 Hz at −90 dBc, the resolution of the spectrum analyzer used.

A series-tuned LC filter can be substituted for the crystal. As long as the loaded Q is greater than about 5, the output distortion will be as good as with the crystal. Sideband noise is worse than with the crystal, however.

High-Purity Sinewave Oscillators with Amplitude Stabilization

This circuit generates very low distortion levels:

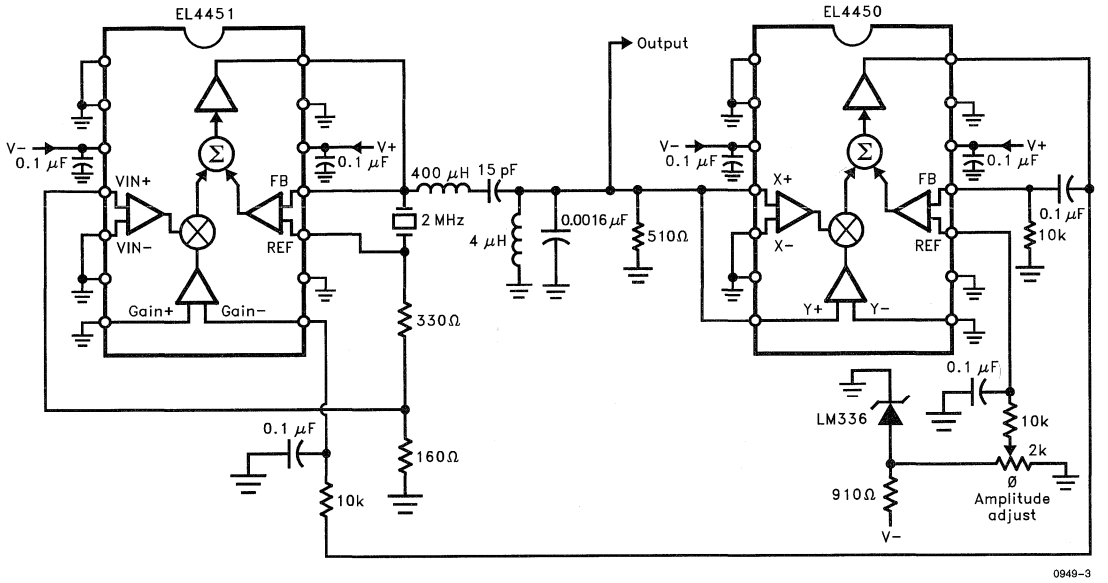


Figure 2. Very Low-Distortion Oscillator

The EL4451 is connected in a slightly different way; the majority of crystal feedback is delivered to the REF input of the feedback amplifier, and a smaller amount of signal routed through the variable-gain input port. In this way, most of the signal runs through a simple voltage-follower path with minimal distortion. The total gain of the EL4451 in this connection is 1 + (Vgain/2V) (160W/(160W + 330W)), which needs to be servoed to about 1.2 for stable oscillation.

The output of the EL4451 is passed through a simple filter to additionally reduce harmonics, then used as the output. For my measurements, I loaded the output with an additional 500Ω, bringing the total load to 250Ω. The EL4451 can drive lower impedances, but the output distortion will rise. Note that no active amplifier nor buffer can be used to drive the output with distortion levels anywhere near that of the passive filter.

Rather than load the filter with a highly nonlinear diode detector, this circuit uses the high-impedance inputs of the EL4450 to sense output amplitude. This is a four-quadrant multiplier, and is used as a mean-square amplitude detector. The advantages include much more precise initial calibration, easier ripple filtering since its at twice the oscillator frequency, and a built-in amplifier which can be used as the servo error amplifier. The X- and Y- inputs of the EL4450 are wired together to produce an internal output^2 quantity at the Σ point. Added to this is a static level from the LM336 reference that has a polarity that subtracts from the mean-square quantity. The FB terminal, normally used for DC feedback, is connected as something like an integrator using the 0.1 μF capacitor. Thus, the output amplifier of the EL4450 is both the low-pass filter and error amplifier for the servo loop, and attempts to maintain the output mean-squared voltage equal to that of the reference.

High-Purity Sinewave Oscillators with Amplitude Stabilization

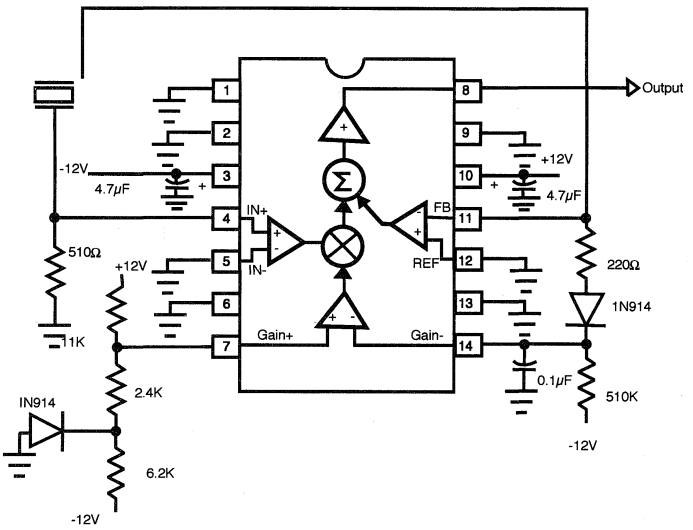
Harmonic distortion is −74 dB with the circuit running on ±5V supplies, and −80 dB with ±12V. As before, reducing the output amplitude improves distortion further.

The error amplifier is not actually required for amplitude stabilization. Since even a miniscule amount of oscillation loop gain more than unity results in a continuously growing amplitude, or a tad less than unity gain creates an ever-shrinking level, we could say that the gain-control input of the oscillating EL4451 already has infinite gain. This circuit makes use of this fact:

This circuit is very simple and still has the low distortion levels of the previous oscillators, but the output level is not well calibrated, despite the diode forward voltage compensation network connected to the Gain + terminal. Variations in crystal series resistance will vary output amplitude.

In summary, we see that recent multiplier ICs can be employed in simple circuits to generate highly pure sinewaves over wide frequency ranges. The particular devices shown are low-cost, yet well calibrated and flexible.

Simple Linear Oscillator



0949–4

EL4089 and EL4390 DC Restored Video Amplifier

John Lidgey, Chris Toumazou and Mike Wong

1. Introduction

The EL4089 is a complete monolithic video amplifier sub-system in a single 8-pin package. It comprises a high quality video amplifier and a nulling, sample-and-hold amplifier specifically designed to stabilize video performance. The part is a derivative of Elantec's high performance video DC restoration amplifier, the EL2090, but has been optimized for lower system cost by reducing the pin count and the number of external components. For R_{GB} and YUV applications the EL4390 provides three channel in a single 16-pin package.

This application note provides background information on DC restoration. Typical applications circuits and design hints are given to assist in the development of cost effective systems based on the EL4089 and EL4390.

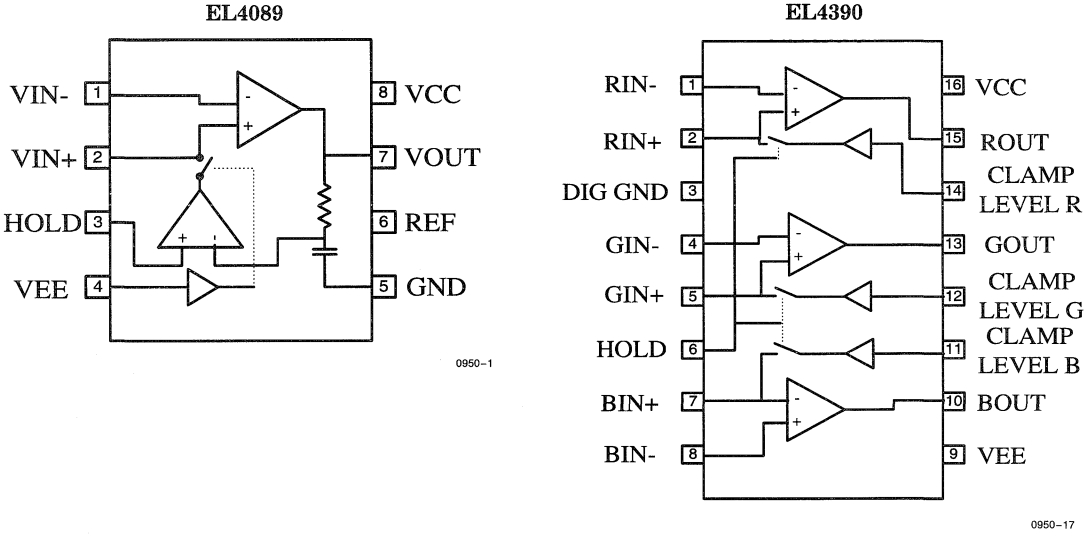


Figure 1. EL4089 and EL4093 Package Outlines

2. Video Signal Refresher

2.1 Composite Video Signal

The figure shown below represents a typical composite video signal, which has a standard distribution level of 1 V_{P-P} into a 75Ω load, and comprises several sections. The video signal is the part containing the visible picture information, with a maximum amplitude between black and white of 0.7V. At the end of the picture information is the front-porch, followed by a sync pulse, which is regenerated to provide system synchronization. The back-porch is the part of the signal that represents the black or blanking level. In NTSC color systems, the chroma or color burst signal is added to the back-porch and normally occupies 9 cycles of the 3.58 MHz subcarrier.

2.2 DC Restoration—The Classical Approach

Video signals are often AC coupled to avoid DC bias interaction between different systems. The blanking level of the composite video signal therefore needs to be restored to an externally defined DC voltage, which locks the video signal to a predetermined common reference level, ensuring consistency in the displayed picture. This DC reference voltage, VR, sets and controls the picture brightness. The fundamental objective of the DC restore system is to force the DC output from the video amplifier to be equal to an externally defined reference voltage VR. Figure 3 shows a classical approach to DC restoration in video systems.

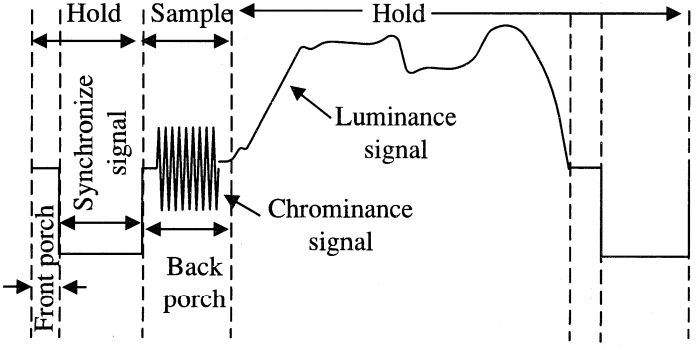


Figure 2. Typical Composite Video Signal

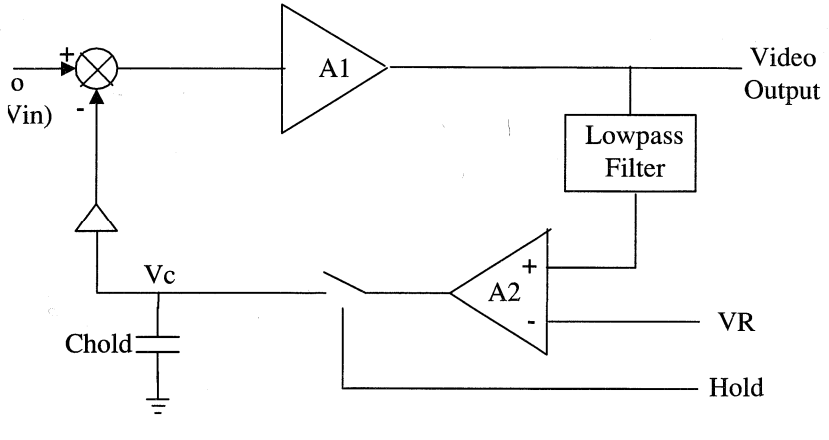


Figure 3. Classical DC Restoration Control Servo Loop

EL4089 and EL4390 DC Restored Video Amplifier

2. Video Signal Refresher — Contd.

The Sync pulse is used to drive the control switch to the sample-and-hold, so that the DC servo loop is closed during the back-porch of the video signal. The lowpass filter is used to remove the chroma burst. The operation of the DC loop is perhaps best understood by considering the voltage appearing across the hold capacitor, C_{HOLD}. During the back-porch sampling period, the switch is closed and the hold capacitor charges up. It can be shown from the loop dynamics that

$$V_C = V_{IN} - \frac{VR}{A1} \quad (1)$$

where V_{IN} = VBP (the average back-porch voltage of the incoming video signal). Equation (1) can be reconfigured,

$$V_C = VBP - \frac{VR}{A1}$$

The net result is that

$$V_{OUT} \approx VR + \frac{VBP}{A2} \quad (2)$$

which shows that the output is clamped to VR with an offset term of VBP/A2. This offset is clearly small for a high gain DC loop amplifier, A2. During the hold period, the switch is open and the stored DC value of V_C is now subtracted from the incoming video signal, which effectively sets the back-porch to VR and the video signal is amplified by the forward amplifier with gain, A1, giving

$$V_{OUT} = (V_{IN} - V_C)A1$$
$$= A1\left(V_{IN} - VBP + \frac{VR}{A1}\right)$$

$$V_{OUT} = A1(V_{IN} - VBP) + VR \quad (3)$$

2.3 DC Restoration—The EL4089 Approach

A simplified scheme of the EL4089 as a feedback system is shown in Figure 4. Unlike Figure 3, the input difference symbol is not shown because the error/correction voltage is stored across the coupling capacitor C_{HOLD} which is outside the control loop.

The operation of the EL4089 is simple, but very subtle. In sample mode, the amplifier's dynamics are such that the output is set to a predetermined reference voltage VR, which may be at ground potential. The correction voltage required at the input of amplifier A1 to maintain V_{OUT} at VR is simply stored across capacitor C_{HOLD}.

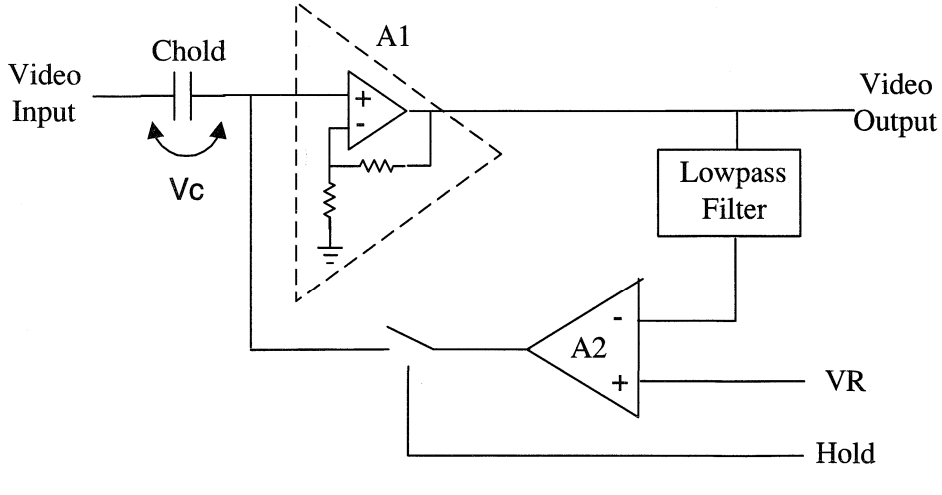


Figure 4. Simplified Block Diagram of EL4089

2. Video Signal Refresher — Contd.

Consider the following analysis. With the switch closed, the input voltage of amplifier A1 is (VR − V_{OUT})A2 giving V_{OUT} = (VR − V_{OUT})A1A2 and thus

$$V_{OUT} = VR\left\{\frac{A1A2}{1 + A1A2}\right\} \approx VR \qquad (4)$$

Assuming that the loop gain A1A2 is very high.

The correction voltage stored across capacitor C_{HOLD} is simply

$$VC = V_{IN} - (VR - V_{OUT})A2 \qquad (5)$$

Assuming in this instance that V_{IN} = VBP, which is the average back-porch reference of the incoming signal, and substituting for V_{OUT} from Equations (4) and (5) gives

$$VC = VBP - \frac{VR}{A1} \qquad (6)$$

Notice that the correction voltage VC is stored across that coupling capacitor C_{HOLD}, which is external to the loop amplifier. Unlike the classical system of Figure 3, it is this unique feature of the EL4089 which obviates the need for a classical sample-and-hold buffer amplifier in the feedback path; thus allowing a very economical 8-pin solution to be realized. Furthermore, the coupling capacitor has two functions, namely to avoid DC bias interaction between different systems and to hold the correction voltage as described above.

During the hold period, the video input signal (V_{IN}) is amplified in the classical way by the *2 video amplifier A1, but in this case the correction voltage held by C_{HOLD} is subtracted from the input to give

$$V_{OUT} = VR + (V_{IN} - VBP)A1 \qquad (7)$$

Summary of Operation

1. When the HOLD logic input is set to TTL/CMOS logic 0, the sample-and-hold amplifier can be used to null the DC offset of the video amplifier.
2. When the HOLD input goes to a TTL/CMOS logic 1, the correcting voltage is stored on the video amplifiers input coupling capacitor. The correction voltage can be further corrected as need be, on each video line.
3. The video amplifier is optimized for video performance and low power. Its current-feedback design allows the user to maintain essentially the same bandwidth over a given gain range of nearly 10:1. The amplifier drives back-terminated 75Ω lines.

Subcircuits

The EL4089 DC restored amplifier is an 8-pin monolithic version of the circuit shown in Figure 4. The video amplifier, A1, is a 60 MHz current feedback amplifier or CFA. These devices offer very high speed performance with excellent differential gain and phase. In many respects the CFA behaves as a conventional op-amp, but there are several key differences that must be considered by the user. In particular the two input impedances of the amplifier are different. The non-inverting input impedance is high and the inverting a low impedance. However, the special feature of the CFA is that when in a closed loop configuration, the feedback current is determined by the resistor, R_F, which controls that bandwidth of the amplifier independently of the gain setting resistor R_G.

EL4089 and EL4390
DC Restored Video Amplifier

2. Video Signal Refresher — Contd.

The current feedback amplifier is essentially a transimpedance amplifier with an input voltage buffer to create a high input impedance non-inverting input. The transimpedance amplifier is formed by mirroring the output current of the input unity gain buffer into a high impedance internal Z-node and buffering this Z-node voltage through to a low impedance output, as shown schematically in Figure 5 below.

The unity gain buffers are a complementary class-AB common-collector stage, with DC current biasing. The slew-rate of the CFA is excellent due to the non-current limiting input stage. The CFA has only one internal high impedance node (Z), so it is essentially a single pole dominant amplifier. Since the inverting input terminal is the output terminal of a voltage buffer, it is a low impedance point and the feedback signal is current. Intuitively one can see that in closed loop the feedback current through R_F supplies the current demanded by R_G and the input error current into the inverting input terminal. It is this feedback current component of R_F which is used to charge the compensation capacitance at the Z-node. Theoretically it can be shown that the −3 dB bandwidth is approximately,

$$f - 3\,dB = \frac{1}{2pRFCZ} \quad (8)$$

where CZ is the compensation capacitance of the Z-node. However, as for conventional op-amps, the closed loop gain, A1, is simply

$$A1 = 1 + \frac{R_F}{R_G} \quad (9)$$

and the −3 dB frequency can be controlled with R_F while the closed loop gain can be set independently with R_G.

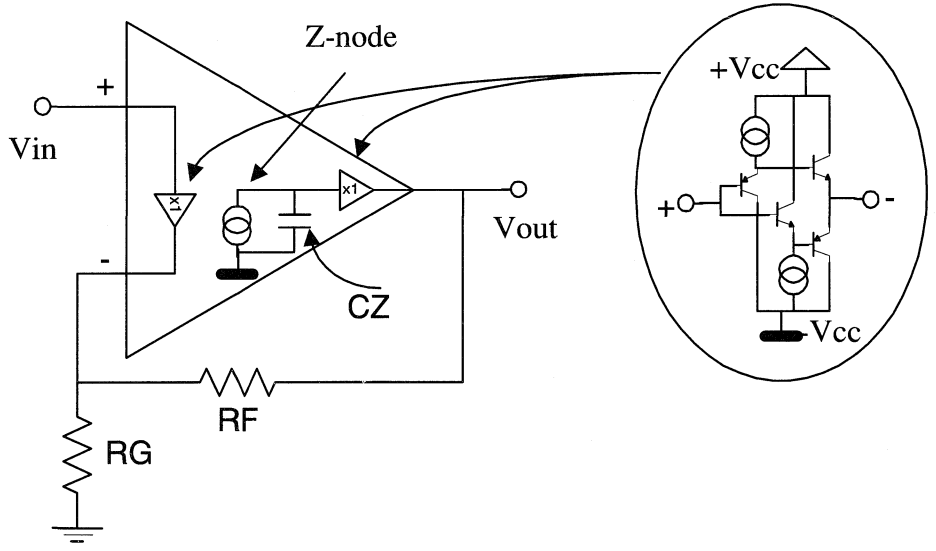


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Figure 5. The Current-Feedback Op-Amp

2. Video Signal Refresher — Contd.

The EL4390 Approach

The EL4390 is three high performance current feed-back amplifiers with DC restore function. A simplified schematic diagram of one of the channels in a DC restore configuration is shown in Figure 6. Its basic approach is very similar to the EL4089 in that the error/correction voltage is stored across the coupling capacitor C_{HOLD} from the video input to the positive input of the amplifier. Different from the EL4089, when the sample and hold switch is close, an internal buffer amplifier is enabled to force the non-inverting input of the video amplifier to be equal to the reference input level. When the switch is open, an error voltage is stored on the input coupling capacitor C_{HOLD} to maintain the offset at the output. The following details the mathematical relationships between the inputs and output.

When the sample and hold switch is close,

$$V_{OUT} = A1 * VR \quad (11)$$

where A1 is the close-loop gain of the amplifier.

The voltage across the hold capacitor is

$$VC = V_{IN} - VR \quad (12)$$

In many NTSC video applications, the back-porch of the video signal is clamped. Thus, V_{IN} is the input back-porch level, VBP.

$$VC = VBP - VR \quad (13)$$

When the sample and hold switch is open, the voltage across the hold capacitor maintains the proper offset.

$$\begin{aligned} V_{OUT} &= A1(V_{IN} - VC) \\ &= A1\,(V_{IN} - VBP + VR) \end{aligned} \quad (14)$$

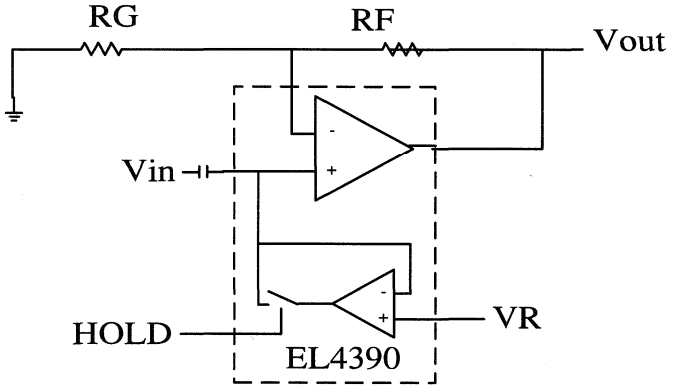

Figure 6. Simplified Connection Diagram of EL4390

EL4089 and EL4390 DC Restored Video Amplifier

3. Features of the EL4089C

Elantec pioneered the development of monolithic CFAs. As first to the market with the CFA our established reputation is confirmed with the EL4089 which is the first 8-pin monolithic DC restored video amplifier. A connection diagram for the EL4089 configured as a DC restoring amplifier with a gain of 2 restoring to ground (pin 3—zero voltage reference) is shown in Figure 7.

The EL4089C is fabricated in Elantec's propriety Complementary Bipolar process which produces NPN and PNP transistors with equivalent AC and DC performance. The EL4089C is specified for operation over the 0°C to +75°C temperature range.

The on-chip current-feedback amplifier of EL4089 and EL4390 is optimized for video performance. Since it is a current-feedback amplifier, the −3 dB bandwidth stays essentially constant for various closed-loop gains. The amplifier performs well at frequencies as high as 60 MHz for the EL4089 and 80 MHz for the EL4390 when driving 75Ω. The sample and hold circuit is optimized for fast sync pulse response.

4. Typical Application Circuits

The EL4089 and EL4390 are designed to DC-restore a video waveform (Figure 2). A typical application circuit of the EL4089 is illustrated in Figure 8. The following analysis also applies to the EL4390. This circuit forces the cable driving video amplifier's output to pin 3 reference voltage level when the HOLD pin is at a logic low. In the case of EL4390, when HOLD pin is logic low, the output of the video amplifier is driven to the reference voltage multiply by the close loop gain of the video amplifier. In Figure 8, pin 3 is grounded and HOLD pin is low during back-porch of the video signal, consequently, the back-porch is clamped to the ground voltage level.

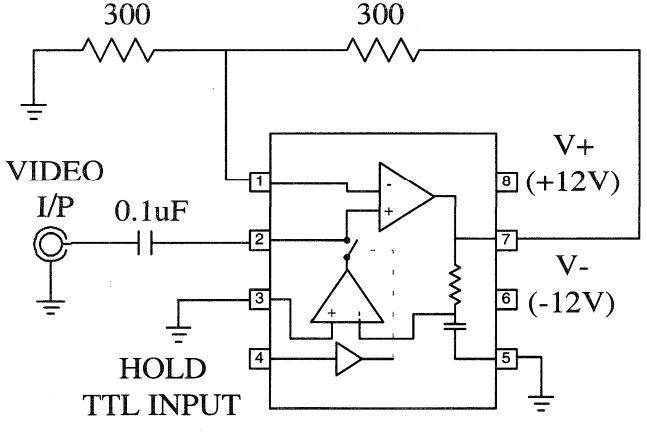

Figure 7. EL4089 Connection Diagram (Configured as a DC Restoring Amplifier with a Gain of 2, Restoring to Ground)

4. Typical Application Circuits — Contd.

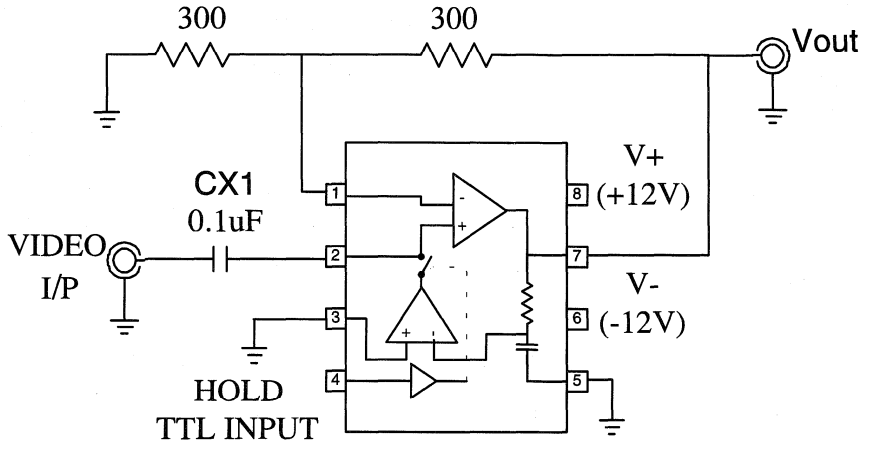

Figure 8

CX1 Determination

The correction voltage is stored across the capacitor CX1, an external ceramic capacitor connecting from the video signal input to the non-inverting input of the video amplifier. The following demonstrates how the CX1 capacitor should be chosen to satisfy the system droop voltage and sampling requirements.

Ideally the input impedance of the video amplifier should be infinite during the hold period to avoid any discharging effects on the CX1 capacitor. However, due to the inherent nature of the bipolar transistors, a bias current is always present. This bias current discharges CX1 during the hold time and as a result causes the correction voltage across CX1 to drift. Equation (15) gives the basic relationship between correction droop voltage and the CX1 value.

$$V(droop) = \frac{(I_B+)(T_{LINE} - T_{SAMPLE})}{CX1} \qquad (15)$$

Where:

V(droop) is the voltage change across CX1 during hold period.

I_B+ is the amplifier's non-inverting input bias current.

T_{LINE} is the single video line duration.

T_{SAMPLE} is the sampling time during which the S/H switch is closed.

The output voltage change due to voltage drooping is simply,

$$V_{OUT}(droop) = V(droop) * A1$$

Where:

A1 is the close loop gain of the video amplifier.

In the Figure 8 design example, a typical input bias current of the video amplifier is 1 μA, so for a 62 μs hold time and 0.01 μF capacitor, the correction voltage droops 6.2 mV; consequently, the output voltage drifts by 12.4 mV in one video line.

EL4089 and EL4390 DC Restored Video Amplifier

4. Typical Application Circuits — Contd.

The CX1 value and sampling time also determinate the amount of time required by the EL4089 to reach within its DC-restored voltage range.

$$V(charge) = I_{OUT}\frac{T_{SAMPLE}}{CX1} \quad (16)$$

Where:

I_{OUT} is the sample and hold amplifier output current.

The sample and hold amplifier can typically provide a current of 300 μA to charge CX1, so with 1.2 μs sampling time, the output can be corrected by 36 mV in each line.

Equations (15) and (16) demonstrate the tradeoffs between CX1, sampling time, DC off-set droop voltage, and speed of the DC-restore function. Using a smaller value of CX1 increases both the voltages that can be corrected each line and the drift while being held, likewise, using a larger value of CX1 reduces those voltages.

In Figure 9, a resistor is connected from the non-inverting input of the amplifier to the negative supply to compensate for the non-inverting input bias current. To obtain the optimum performance, the compensation resistor R1 should be adjusted to give 0 mV droop voltage at 50% field.

The restore current generated by the sample and hold amplifier decreases as the output voltage approaches the reference voltage. This effect combines with the 7 mV of offset voltage error in the sample and hold amplifier can result in a 22 mV of total error from the output to the reference voltage input during clamping. A method of correcting this problem is depicted in Figure 10. A voltage divider is used to compensate for the sample and hold amplifier offsets.

A complete DC-restore circuit with the EL4581 sync separator is shown in Figure 11. An optional RC low pass filter on HOLD input pin is included should the logic signal require slowing down. This RC network can also serve to prevent feet-through from the falling and rising edges of the back-porch sync timing signal to the video amplifier output. The video DC restore output and EL4581 back-porch timing waveforms are illustrated in Figure 12. During the back-porch interval, the EL4581 pulls the hold pin of the EL4089 low and the EL4089 servo loop forces the output to the reference voltage level. In the photo, the input back-porch voltage level is 0.5V and the output back porch voltage level is restored to 0V, the reference voltage level.

4. Typical Application Circuits — Contd.

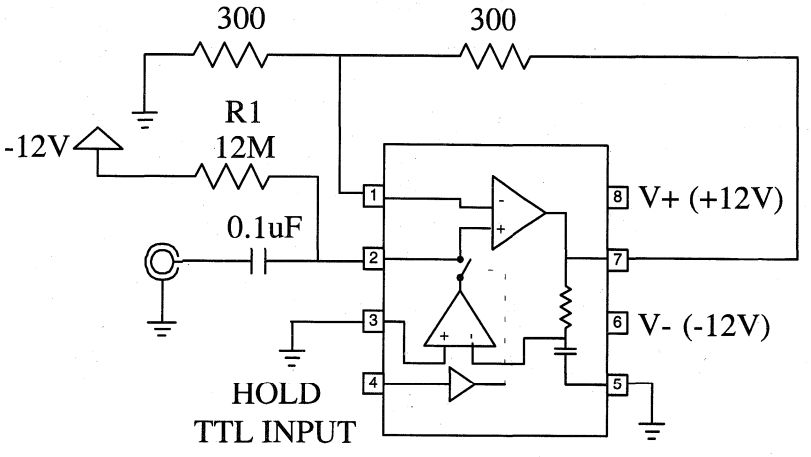

Figure 9. I_B+ Bias Current Correction

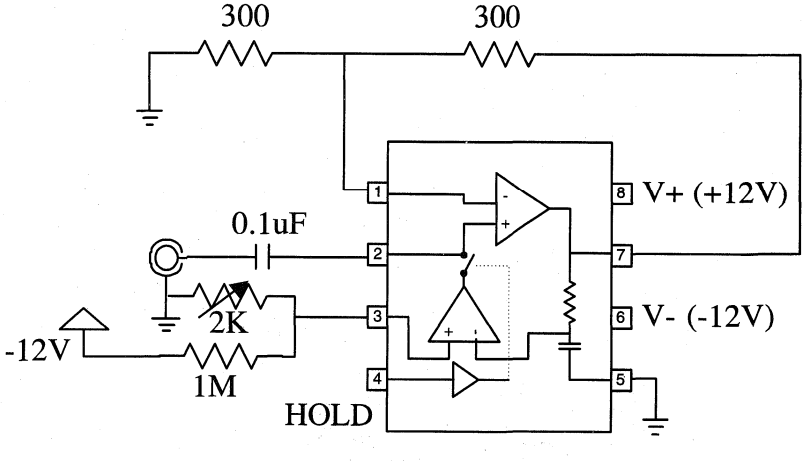

Figure 10. Sample and Hold Off-Set Error Compensation

4. Typical Application Circuits — Contd.

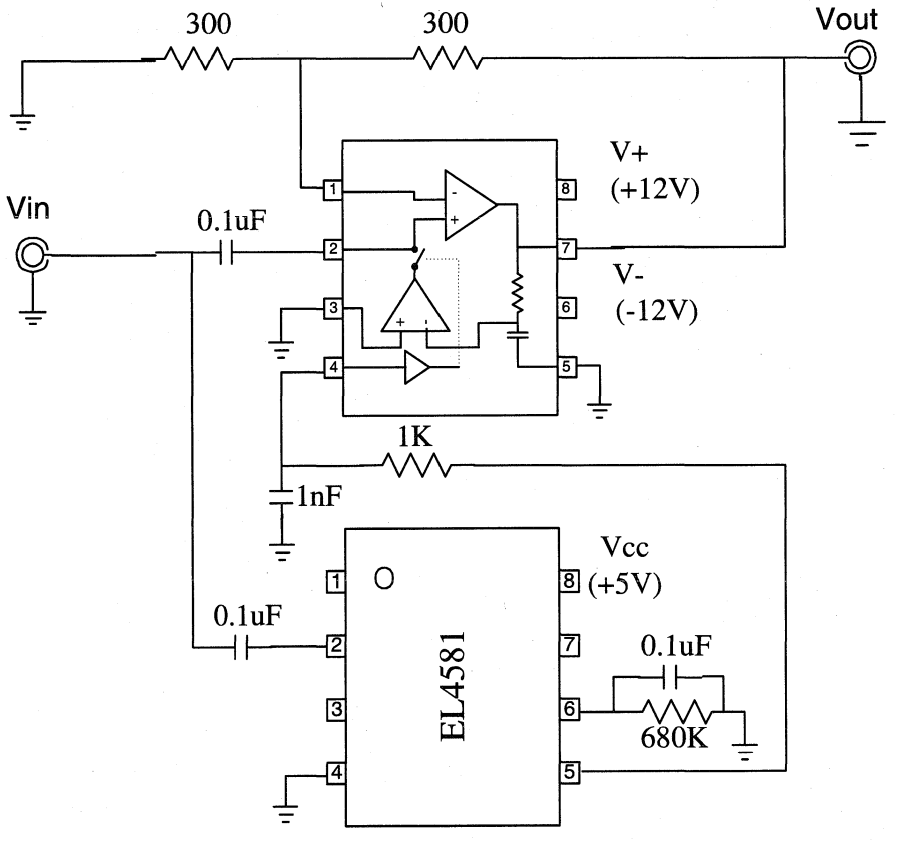

Figure 11. EL4581 and EL4089 Restore Amplifier and Sync Separator

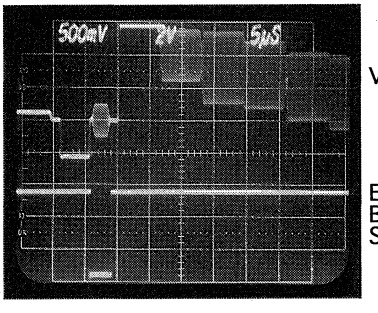

Figure 12. Video Output and EL4581 Back-Porch Sync Signal

4. Typical Application Circuits — Contd.

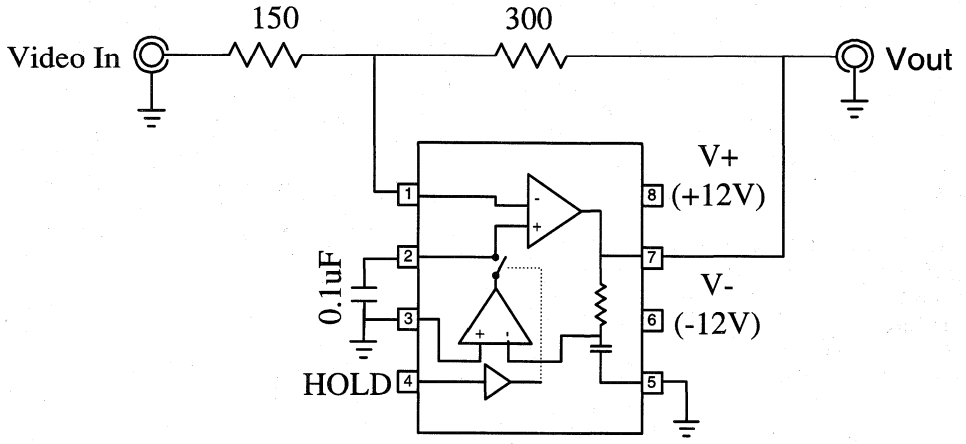

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Figure 13. EL4089 DC-Restore Amplifier in −2 Gain Configuration

EL4089 in Inverting Gain Configuration

Placing the hold capacitor in the signal path leads to sync signal feed-through and phase distortion of the burst signal. Rearranging the EL4089 in the inverting configuration as shown in Figure 13 provides significant improvements. Figure 14 indicates a 15 mV of voltage spike in amplifier output during the sampling interval and coincides with the falling and rising edge of the HOLD signal. The output voltage spike is caused by the charging current injecting out of the output of S/H amplifier during the back-porch interval. One way to minimize the sync feed-through is to feed the video input signal directly into the inverting input of the video amplifier and short the DC restore capacitor to ground. As a result, the video input signal is not affected by output current of the S/H amplifier. The voltage spike is also reduced by an addition of a simple RC network from the output of the EL4581 to the HOLD input of the EL4089. Figure 15 test result shows no voltage spikes and only a 4 mV of voltage dip during the sampling period. In the inverting configuration, the video signal goes directly into a purely resistive component, thus, no phase shift occurs.

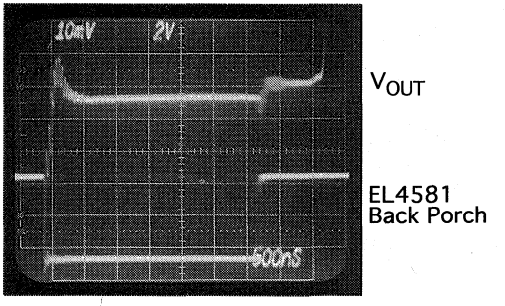

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Figure 14. Back-Porch Sync Edge Feed-Through

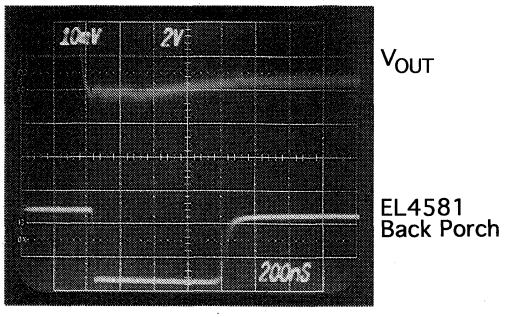

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Figure 15. EL4089 Inverting Amplifier Output Waveform

EL4089 and EL4390 DC Restored Video Amplifier

4. Typical Application Circuits — Contd.

EL4581 Interface

The hold input of the EL4089 is designed to interface directly to Elantec's existing suite of sync separators, namely the EL4581 and the EL4583. The connection diagram of the EL4581 is shown in Figure 16.

The EL4581 extracts timing information including composite sync, vertical sync, burst/back-porch timing and odd/even field information from standard negative going sync NTSC, PAL, and SECAM video signals. The EL4581 detects video signals from 0.5 to 2 V_{P-P}. The 50% slicing feature provides precise sync edge detection even in the presence of noise and variable signal amplitudes. A built-in linear phase, third order, color burst filter minimizes spurious timing information and reduces the number of external components. The integrated circuit is also capable of providing sync separation for non-standard, faster, horizontal rate video signals by changing an external horizontal scan rate setting resistor. The vertical output is produced on the rising edge of the first serration in the vertical sync period. A default output is produced after an internally generated time delay, in the event of missing serration pulses, for example, in the case of a non-standard video signal. All outputs are active low.

5. Printed Circuit Board Layout Hints

The feedback path of the video amplifier should be kept as small as possible to avoid deterioration of high frequency gain accuracy.

The board layout should have a ground plane underneath the EL4089, with the ground plane cut away from the vicinity of the $V_{IN}-$ pin (pin 1) to minimize the stray capacitance between pin 1 and ground.

Power supply bypassing is important and a 0.1 μF ceramic capacitor, from each power pin to ground, placed very close to the power pins, together with a 4.7 μF tantalum bead capacitor, is recommended.

When both digital and analog grounds are on the same board, the EL4089 should be on the analog ground. The digital ground can be connected to the analog ground through a 100Ω–300Ω resistor near the EL4089. This allows the digital signal a return path while preventing the digital noise from corrupting the analog ground.

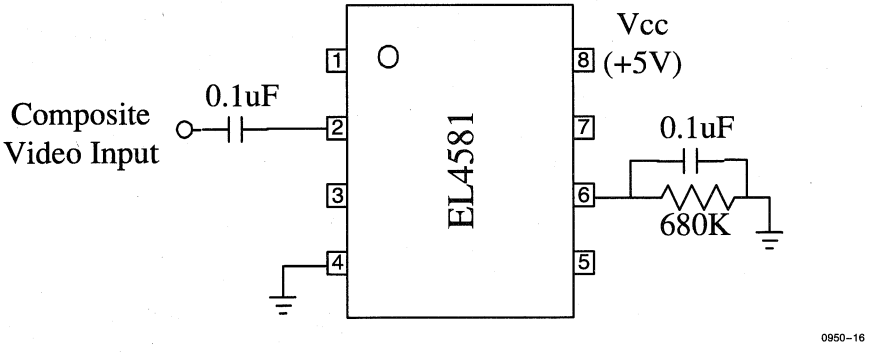


Figure 16. EL4581 Connection Diagram

An Improved Peak Detector

by Tamara I. Ahrens

Diodes have long served as adequate rectifiers despite necessarily large input voltages and poor accuracy. The most common configuration for a simple diode peak detector (Figure 1) provides a mediocre 10% error for very large input voltages (Figure 2). If the diode is linearized, the necessary input voltage is only reduced to 1V peak for the same 10% error (Figure 2). However, development of high frequency op amps allows feedback circuitry to provide better accuracy and more sensitivity at the input. With feedback (Figure 3), peak detection is feasible at input voltages as small as 50 mV/rms.

Function of Feedback Diode Circuitry

The input stage consists of a high frequency op amp whose output is fed into both a diode (D1), which functions similar to the diode of a simple peak detector, and a clamping network, which limits the negative output swing of the forward op amp. The output of the diode (D1) is connected to the storage capacitor and is also fed back to the input through a buffer. A storage capacitor of 0.1μF is recommended for peak detection at audio frequencies. A small resistance is shown in series with the storage capacitor to isolate it from the feedback loop. The smallest functional value is recommended for minimal peaking and maximum bandwidth; 10Ω is suggested. A bleed current is necessary to allow the output to relax for a smaller input or in the absence of an input. 20μA, small enough to avoid deteriorating the output value substantially, but large enough to dominate the bias current of the feedback buffer, was chosen. The output of the buffer is fed back to the negative input of the forward op amp through a resistor. This resistor buffers the emitter of the pnp transistor of the clamping network from the low impedance at the output of the buffer. Please note: a compensation capacitor on the forward op amp may be a necessary addition to ensure stability and the output of the entire peak detection circuit must be buffered to prevent a disturbance in performance.

Clamping Network

The diode (D2) of the clamping network is always held on by the current source. For voltage signals greater than the peak held at the output, the forward, rectifying diode (D1) is conducting, the output voltage is raised to match the input voltage, the buffer feeds that voltage back around to the negative input of the forward op amp, and the emitter of the pnp transistor is held at the same voltage as its base, keeping it off and eliminating the second feedback loop.

For voltage signals less than the peak held at the output, the rectifying diode (D1) is off. The emitter of the pnp transistor is set as high as the output voltage by the buffer through the 1kΩ resistor while the base is pulled down by the output of the forward op amp through the feedback diode (D2). The 270Ω resistor adds a 0.3V bias to the base of the transistor producing a charge-discharge current ratio of 10,000:1. When the transistor turns on, a crude unity gain feedback loop is completed through the clamping network (from the output voltage, down a diode drop and up the base-emitter diode of the transistor, to the input voltage) and a voltage drop builds across the 1kΩ resistor. This clamping action minimizes the recovery time of the circuit. Since the clamping network works like a unity gain buffer for inputs less than the peak voltage, the output needs to slew less than one diode drop to turn on the rectifying diode (D1) for inputs greater than the peak voltage. In this manner, the clamping network prevents the forward op amp from exhibiting open loop behavior and railing negative for inputs less than the peak voltage. This greatly reduces the slew rate necessary to achieve a desired bandwidth.

Amplitude Considerations

This circuit has the ability to function with amplitudes 30 times smaller than a simple diode peak detector. The EL2244 has an open loop gain of 60dB, raising smaller input signals enough to be detectable by the diode. The smallest amplitudes recoverable will be determined by the noise

An Improved Peak Detector

amplified within the circuit. For the given circuit, this limit is approximately 30mV/rms input voltage. The largest amplitudes allowable will be determined by the input constraints of the op amp. For the EL2244 at ±5V supplies, the maximum input range is approximately ±3.5V.

Frequency Considerations

If 5% errors can be tolerated, this circuit has a bandwidth of 100 kHz (Figure 4), making it ideal for audio applications. A great deal of small signal bandwidth and large slew rates are necessary to swing quickly through the dead zone at the output of the first op amp and these quantities limit circuit performance.

Thus, for a handful of inexpensive parts, a drastic improvement can be made in the performance of a peak detector over that of a simple diode. With the utilization of modern, high-speed op amps, the feedback diode peak detector offers almost two decades of input voltage range improvement while maintaining functionality into the megahertz range.

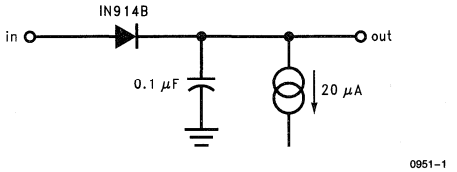


Figure 1. Simple Diode Peak Detector

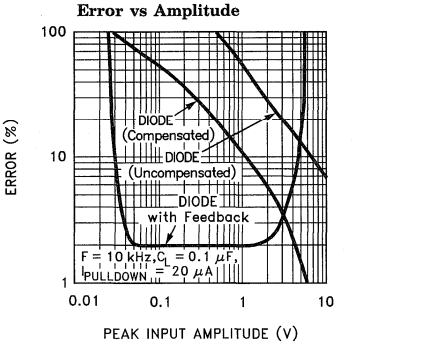


Figure 2

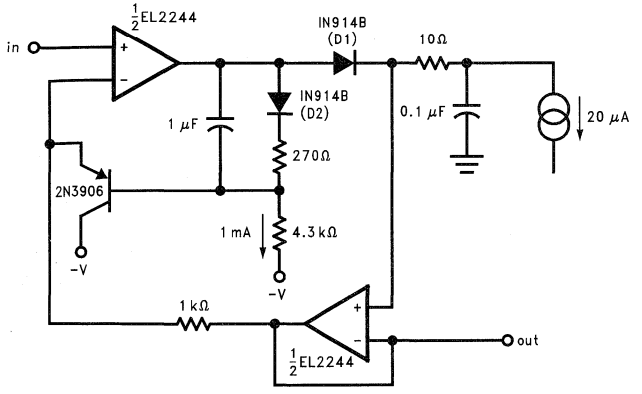
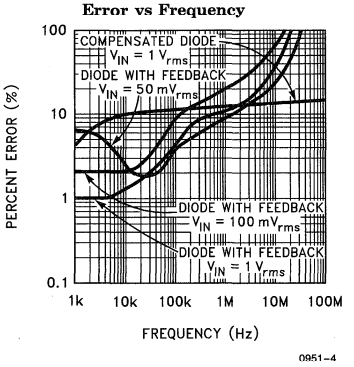


Figure 3. Diode with Feedback



0951-3

Figure 4

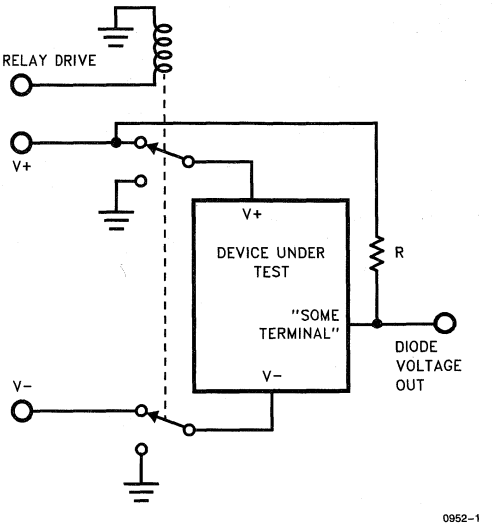
Measuring the Thermal Resistance of Power Surface-Mount Packages

by B. Harvey

Modern miniature IC packages have allowed great space savings in products, but frustrate the designer by concentrating the heat generated by circuits into smaller volumes. Increasing IC speeds and complexities over the years have also demanded greater power dissipation. Higher internal operating temperatures will shorten the life of an IC; elevated but safe temperatures often reduce the quality of performance in circuits, for instance degrading frequency response or distortion.

To cope with the problem, a variety of heat management packages have been introduced which conduct heat from the IC die through the package leads to the circuit board. The board becomes the major heatsink, and the onus of thermal design passes from the IC manufacturer to the board designer. This article is intended to assist the board designer in measuring thermal resistance of mounted IC devices efficiently.

Traditional parameters θ_{JA} (thermal resistance of a device not connected to anything) and θ_{JC} (infinite heatsink connected to the part) are not useful with mounted devices. Circuit boards are neither insignificant nor infinite heat sinks. We will use the parameter θ_{JM} as the mounted thermal resistance of an IC, and it will vary with die size, package type, and circuit board features. The θ_{JM} can be estimated by thermal simulation of the part and its mounting environment, but seldom is there concrete data on the thermal structure of the IC, and correctly modeling the board environment is difficult. A good way to estimate θ_{JM} is to solder the IC to an area of circuit board that has been suitably sculpted with a Dremel tool to emulate a final board pattern in the region of the test device (or a finished board itself) and use the following circuit to measure θ_{JM}:



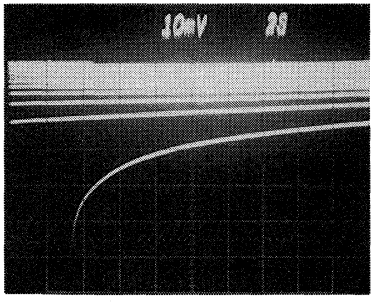
"Some terminal" is any pin that is connected to an internal parasitic diode whose other connection is either power supply pin. The IC manufacturer's technical support people can help select the right pin and drive polarity. We will use the forward voltage as a measure of internal die temperature. When the relay grounds the supply pins, R provides a current from a supply to bias the diode. Depending on the internal diode connection, V+ or V− will be connected to R. R should supply a current low enough to create minimal resistive drop in series with the diode. 50 μA is a good guess for the current, or any current that sets up about 600 mV of forward diode voltage at room temperature. The general equation for diode tempco (it generally need not be measured directly) is:
$\Delta V/\Delta T = -(1.12V - Vbe\ (25°C))/300°K$. Thus a 600 mV junction at room temperature has a −1.7 mV/°C temperature coefficient.

Measuring the Thermal Resistance of Power Surface-Mount Packages

Using a storage or digitizing oscilloscope measuring the forward diode voltage, we will observe the thermal relaxation of the die after a steady power dissipation is terminated. The dissipation is the part's own supply current, applied through the relay. The relay's drive is also the oscilloscope trigger. Because the temperature change may only cause tens of millivolts of diode voltage variation against the background of 600 mV, a stable differential-amplifier with adjustable offset will be used for the oscilloscope input. Alternately, the ground of the above circuit may be shifted with a third supply before being connected to the oscilloscope.

This is the test sequence:

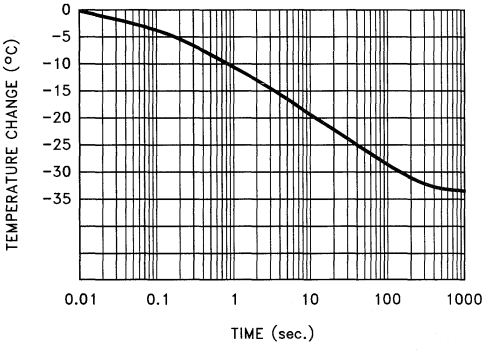
1. Connect everything with the device powered down. Set the oscilloscope sweep to the slowest setting, continuously sweeping.
2. Adjust the offset against the diode voltage to center the oscilloscope trace. The 10 mV/div. sensitivity is a good start.
3. Apply power to the device via the relay. The oscilloscope trace will be off-screen. Allow the part at least ten minutes to warm up its mounting.
4. Clear any stored trace. Turn off power to the device. The following trace should be seen on the oscilloscope:



0952-2

Oscilloscope Display of Diode Voltage Relaxation During Cooling

We see an initial rapid cooling followed by very slow settling back toward room temperature. The cooling rate is not a simple exponential decay, but has a wide range of time dynamics. Here is the decay behavior of an EL1501 mounted on a large heat spreader:



0952-3

Thermal Relaxation vs. Time of a Mounted Power SO-20 Package

For the first ten milliseconds little die temperature change occurs. Then the heat makes its way through the die and flows out through the leadframe, which occurs in around ten seconds. The last event is the settling of the heat-sinking board, which resolves in ten minutes. Clearly, thermal measurements require patience and time.

The thermal resistance θ_{JM} is then the temperture variation (long-term) divided by the power dissipated, so:

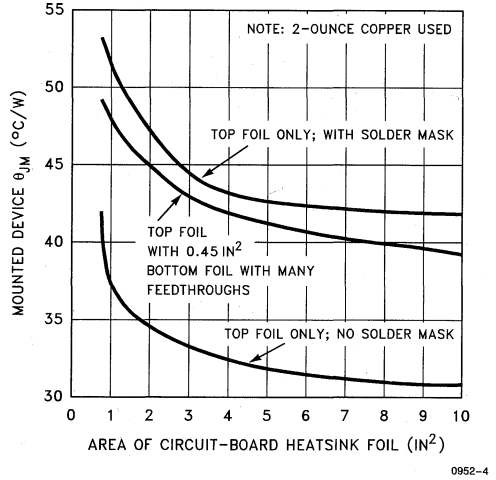
$$\theta_{JM} = \Delta T_{diode}/P_{diss,\ quiescent}$$

$$= \frac{\Delta Vdiode * 300°K}{P_{diss,\ quiescent} * (1.12V - V_{BE}\ (25°C)}$$

Measuring the Thermal Resistance of Power Surface-Mount Packages

Using this technique, the thermal resistance of the SOL-20 fused-lead package was measured. This package houses the EL1501 and has four center leads on each side fused to the IC's mounting header. Thus, heat flows directly through these pins from the IC and spreads through the ground plane on top of the circuit board. A nearly continuous ground plane is hand-drawn. Several variations of the board were tested. The first was the most straightforward: just the top foil is a heatsink. By cutting away board material, a variable area was implemented and thermal resistance measured. Then the measurements are repeated on an identical board with no solder mask to add to thermal resistance. Another variation was to create another heatsink area on the back of the board, thermally connected to the top foil by a multitude of feedthroughs. Finally, a copper sheet-metal heatsink was soldered to the top foil near the IC's heat-spreading pins.

The results are shown in this graph:



Thermal Resistance of Dual-4-Fused-Lead SOL-20 Package

The SO-20 standard package has a θ_{JA} of 80°C/W. With 4in^2 of circuit board heatsink copper with solder maskcutout, the thermal resistance drops to 32°C/W. Given a quiescent dissipation of 1.25W, the die temperature rise of the mounted EL1501 is 40°C. With a maximum ambient temperature of 85°C, we have a worst-case die temperature of 125°C, safely within the 150°C package limit.

Some observations:

1. 4in^2 of copper area is sufficient in that more doesn't help much.
2. The bottom foil did not greatly help.
3. Removing the solder mask over the heat spreading area, if appropriate, reduces θ_{JM} nicely.

Finally, a large metal heatsink mounted close to the heat-spreading pins produced a θ_{JC} of 30°C/W.

Driving Reactive Loads with High Frequency Op-Amps

by Barry Harvey and Chris Siu

As the bandwidth of op-amps today pushes past 100 MHz towards the GHz region, increasing attention must be paid to the components, loads, and circuit traces which surround the op-amp. Not only is this necessary to optimize performance, but neglecting to do so may throw the amplifier into oscillation. This application note discusses the effect of loads, especially capacitive ones, on the behaviour of a high speed op-amp.

1.0 Real World Loads

To start, one needs to question whether there are any pure capacitive loads at high frequencies. To connect any load we need some wires or metal interconnect, and associated with these wires are resistance and self-inductance. In the following sections we will examine some possible loads and their behaviour over frequency.

Coaxial Cables

Coaxial cables must be terminated in the proper impedance to look like a resistive load to the driving source. A common myth is that an unterminated cable looks capacitive. While this may be true for short cables at low frequencies, it certainly does not hold at higher frequencies. An unterminated cable presents a varying impedance to the source over frequency, and it can look capacitive or inductive depending on the length of the cable and the frequency. This behaviour can be explained by viewing the coaxial cable as a lossless transmission line. The input impedance Z_i of a transmission line with characteristic impedance Z_o and length L, terminated in a load Z_L, is given by:

$$Z_i = Z_o \frac{Z_L + jZ_o \bullet \tan \beta L}{Z_o + jZ_L \bullet \tan \beta L}$$

where $\beta = 2\pi/\lambda$, and λ is the size of one wavelength on the line. As an example, consider the standard RG58C/U 50Ω coaxial cable. If we terminate the cable with a 50Ω load, then by the above equation $Z_i = Z_o$ and the cable should look perfectly resistive over frequency. Figure 1.1 shows an actual measurement done on a 5′ long cable terminated in a 50Ω load. Except for minor impedance variations due to mismatch and line loss, the cable does look like 50Ω over a wide range of frequency. If the cable was terminated improperly, with a 75Ω load for example, the impedance then varies with frequency as shown in Figure 1.2. Note that even though we have terminated the cable with a resistive load, the cable impedance phase varies between ±23°. In the extreme, if the cable is unterminated, then $Z_L = \infty$ and the equation reduces to $Z_i = -jZ_o/(\tan \beta L)$. Figure 1.3 shows the input impedance of an unterminated 50Ω cable, and we see the phase skipping between −90° (capacitive) to +90° (inductive) at regular intervals. In fact, for frequencies at which the line length is an odd multiple of a quarter wavelength, Z_i becomes zero. Conversely, for frequencies at which the line is a multiple of a half wavelength, Z_i becomes infinite.

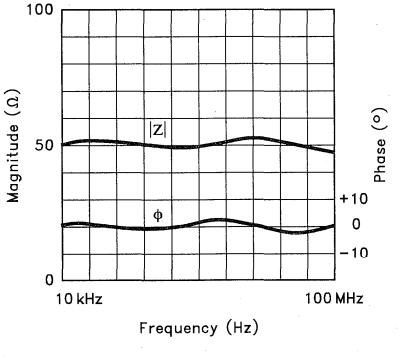


Figure 1.1. Impedance of a 50Ω Cable Terminated in 50Ω

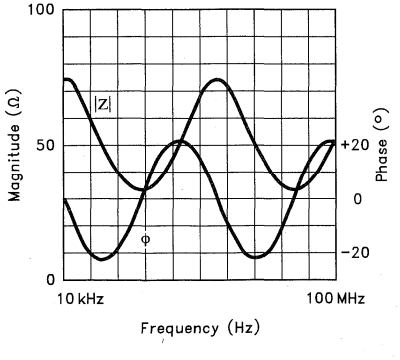


Figure 1.2. Impedance of a 50Ω Cable Terminated in 75Ω

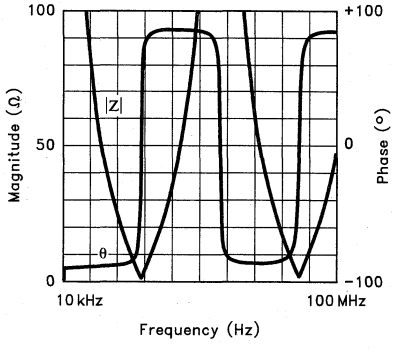


Figure 1.3. Impedance of an Unterminated in 50Ω Cable

The moral of the story is that you must terminate your cable with the correct load at high frequencies. Otherwise, the driving source will see a wildly changing load with frequency, and this may cause the amplifier to oscillate.

Discrete Capacitors

At high frequencies, another parasitic which becomes dominant is the inductance of a leaded capacitor. We can treat the capacitor as a series RLC circuit, with L modelling the lead inductance and R modelling the losses due to the electrodes, leads, and dielectric. The capacitor will thus self-resonate at a frequency given by:

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

As an example, the impedance of a 10 nF leaded ceramic capacitor was measured, yielding the equivalent series RLC values of 0.66Ω, 36 nH, and 8.6 nF respectively. Figure 1.4 shows the impedance of this capacitor over frequency, and we see that it self-resonates at 9.1 MHz, behaving as an inductor for frequencies above that. For this measurement the leads of the capacitor were kept as short as possible. If we were a bit sloppy and left 1" leads on the capacitor, the inductance would increase to about 60 nH, lowering the resonance down to 7 MHz. Generally, an inch of slender wire has about 20 nH of inductance per inch, which is why it is so important in high frequency work to minimize lead length.

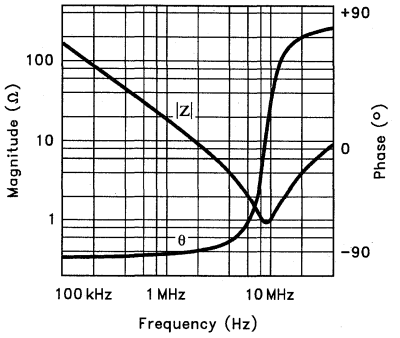
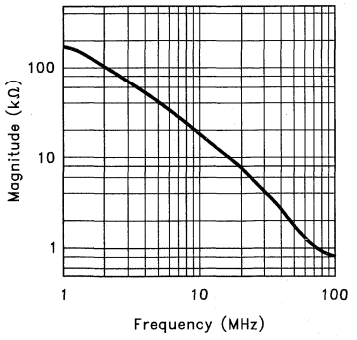


Figure 1.4. Impedance of a Leader 10 nF Capacitor

Inputs of Active Devices

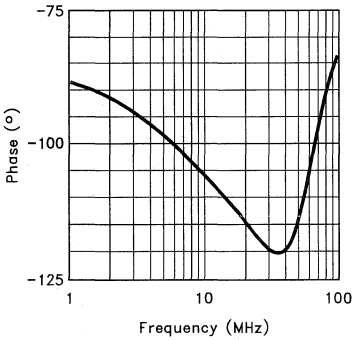
Besides driving cables or passive loads, an amplifier could also be driving the input of another active device. At first, one might think that the input of an op-amp can be modeled by some high-value resistance in parallel with a capacitance. While this model is correct to some extent, some measurements quickly reveal that the input capacitance is not all that "pure". Figure 1.5 shows the input impedance of the EL2044 connected as an unity gain buffer. While the impedance does decrease with frequency, it does not do so at −6 dB/octave; rather, the impedance is decreasing at a greater rate. The phase of the input impedance also reveals the "impurity" of this input capacitance.

Driving Reactive Loads with High Frequency Op-Amps



(a) Magnitude

0954-5



(b) Phase

0954-6

Figure 1.5. Input Impedance of a Unity Gain Follower Using The EL2044

Other Capacitive Loads

As the examples above may suggest, strictly capacitive loads are difficult to find at high frequencies. The only load we know of that is capacitive at high frequencies is a Liquid Crystal Display (LCD). In this instance, the intersection of the row and column lines causes many capacitances to be distributed along the line, and because of numerous parallel lines the inductance tends to be low, giving loads upwards of 1000 pF without large amounts of inductance.

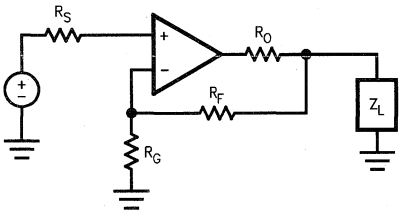
Although pure capacitive loads are rare at high frequencies, this does not mean that we can ignore them. Capacitive reactance can exist over narrow frequency ranges, and we must ensure that our amplifier does not oscillate in these ranges.

2.0 Capacitive Loads are Hard

Generally, an op-amp has no problem driving resistive or inductive loads. Of course, this statement needs to be qualified as to the size of the load, but the point is that both kinds of loads do not degrade the phase margin of the amplifier. Capacitive loads, on the other hand, do reduce an amplifier's phase margin, and in severe cases can cause the op-amp to oscillate.

Op-Amp Output Resistance

To see how various loads affect the phase margin, we can model the open-loop output impedance of an op-amp as the resistance R_o. Shown in Figure 2.1, R_o forms a divider with the load Z_L, and the output V_o goes to the feedback network R_F and R_G. If the phase lag of V_o increased due to the R_oZ_L divider, the phase margin around the loop diminishes and peaking, even oscillation, will occur.



0954-7

Figure 2.1. Open Loop Output Resistance of an Op-Amp

First, if Z_L is resistive, then there is no phase lag and the phase margin is preserved. If Z_L is inductive, then V_o gets a phase lead and the phase margin is increased! Finally, if Z_L is capacitive then we do get a phase lag and the amplifier will peak due to this load. The severity of this problem increases with high speed op-amps, as the example below illustrates.

Suppose that we have a 100 MHz amplifier with 45° of phase margin. Let $R_o = 50\Omega$ and $Z_L =$ 15 pF, then this network has a cutoff frequency f_c of 212 MHz. At 100 MHz, this network provides 25° of phase lag and thus reduces the phase margin to 20°. Severe peaking will result in the frequency response. The loss of phase margin due to a capacitive load is given by:

$$\Delta PM = TAN^{-1}\frac{f_u}{f_c}$$

where f_u is the op-amp's unity gain frequency, and f_c is the cutoff frequency of the R_oC_L network. Thus we see that for high frequency op-amps, even a small capacitive load can cause a large reduction in the phase margin.

Op-Amp Output Inductance

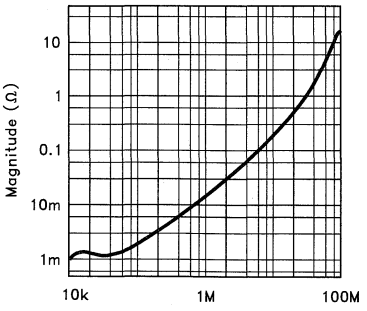
Another way to understand an op-amp's sensitivity to capacitive loads is to look at its closed-loop output impedance more closely. As an example, consider the output impedance vs frequency curve of the EL2044, reproduced in Figure 2.2. We see that beyond about 200 kHz, the output impedance actually looks inductive, and this would resonate with a capacitive load! To see why an op-amp's output impedance looks inductive, consider the circuit in Figure 2.3, where we have an op-amp with open loop gain A(s) and some general feedback network with gain β. The transfer function of this circuit is given by:

$$H(s) = \frac{A(s)}{1 + A(s)\beta}$$

If the loop transmission $A(s)\beta$ is large, then $H(s) \cong 1/\beta$, and we arrive at one of the important results of negative feedback: the system's gain depends largely on the feedback network and not on the op-amp itself. Similarly, the system's output impedance is given by:

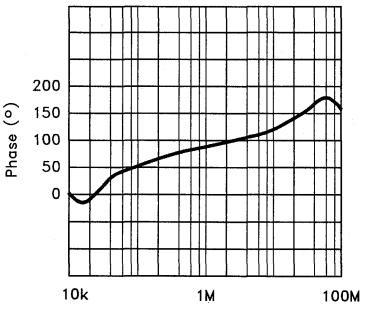
$$Z_{OUT} = \frac{R_o}{1 + A(s)\beta}$$

where R_o is the op-amp's open loop output resistance. Thus for large values of loop transmission, negative feedback drives the output impedance to some low value. As frequency increases, however, the magnitude of A(s) rolls off, reducing the loop transmission and raising Z_{OUT}. Eventually, at frequencies where $A(s)\beta << 1$, Z_{OUT} asymtotes to the output impedance of the op-amp output stage.



(a) Magnitude

0954-9



(b) Phase

0954-10

Figure 2.2. Closed Loop Output Impedance of EL2044

Output Stage Superinductance

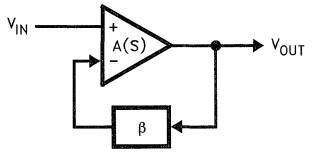
Beyond the system level explanations given above, we can gain understanding into the problem by looking at the op-amp at the transistor level. In any op-amp we have an output stage that buffers the gain stage from the external load. The emitter follower is often used for this purpose, so we will consider the follower's output impedance under different conditions. Figure 2.4 shows the general circuit. At low frequencies we can find the output impedance using the reflection rule:

$$R_{OUT} = \frac{R}{\beta + 1}$$

Driving Reactive Loads with High Frequency Op-Amps

At higher frequencies, however, we cannot neglect the frequency dependence of β. If we model β as a single-pole system with DC gain β_0 and unity gain crossing w_u, then the output impedance becomes the following:

$$Z_{OUT} \cong \frac{R}{\left(\frac{B_0}{1 + j\frac{f\beta_0}{f_T}}\right)} = \frac{R}{\beta_0}\left(1 + \frac{f\beta_0}{f_T}\right) = \frac{R}{\beta_0} + jf\frac{R}{f_T}$$



0954-8

Figure 2.3. Block Diagram of General Feedback System

then we get the transformations shown in Figure 2.4. In the first case where the source is resistive, the output impedance is resistive and inductive. This is intuitively similar to the op-amp example presented earlier; since β decreases with frequency, R_{OUT} rises and thus appears inductive. Hence we see that even a simple emitter follower can resonate into a capacitive load. As an example, a transistor with an internal base resistance of 200Ω and a f_T of 300 MHz has an output inductance of 100 nH. If this was used to drive a 50 pF load, its resonant frequency would be at 70 MHz, well within the range of today's high speed op-amps.

The next transformation is for a capacitive source, which results in a resistive and capacitive output impedance.

Finally, when the source is inductive, the output impedance has a negative real component. This negative impedance has no reactive phase, but its magnitude increases as the frequency squared; we will name this component a "super-inductor". If the sum of series resistance in a network is negative and all the reactances cancel, then the network will oscillate. Thus the seemingly benign emitter follower really misbehaves if we drive it with an inductive source!

So where do we get an inductive source from within an op-amp? The Darlington connection is one possibility. In this configuration, an emitter follower drives another emitter follower. The first follower transforms its base resistance into an output inductance, and the second follower transforms this inductance into an output super-inductance. The effect is the same for a NPN follower driving a PNP, or vice versa. Since base resistance tends to be larger for IC transistors than for discrete transistors, super-inductance is very much an issue for monolithic amplifiers. An output stage with this topology is shown in Figure 2.5, first used in the LH0002 buffer amplifier. Most integrated amplifiers built with a complementary bipolar process also use this output stage, and so a real amplifier's output impedance is the sum of resistive, inductive, and super-inductive components. If a capacitive load resonates with the inductance at a frequency where the super-inductance is greater than the real resistance, oscillations will occur in the output stage independent of loop characteristics.

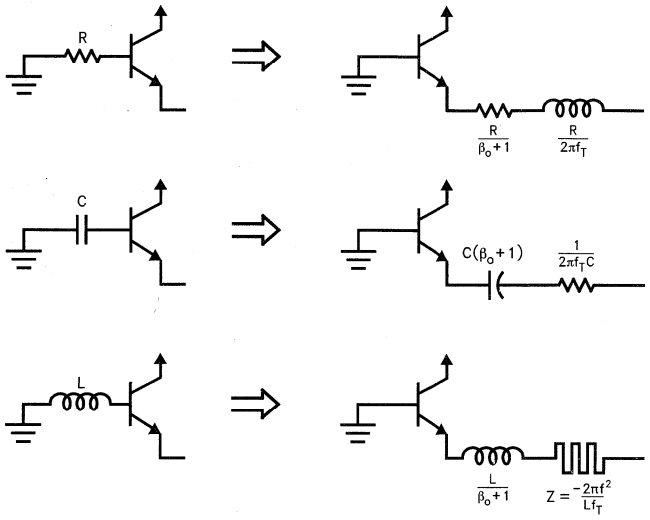


Figure 2.4. Impedance Transformations for an Emitter Follower with Various Source Impedances

Driving Reactive Loads with High Frequency Op-Amps

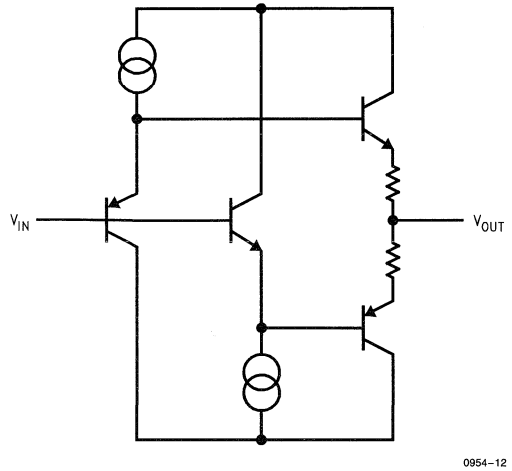


Figure 2.5. LH0002 Output Stage Topology

3.0 Possible Solutions

Like death and taxes, it is inevitable that we will have to drive some form of capacitance. Unlike death and taxes, techniques exist to deal with capacitive loads to some degree. We will present some of these techniques in the following sections.

Internal Compensation

As we saw earlier, heavy capacitive loads can reduce the phase margin of an amplifier, and thus cause the amplifier response to peak. However, if we can lower the dominant pole of the amplifier such that the phase margin is restored, then the overall amplifier response should not peak, although the bandwidth will also be reduced. Is there such a way of sensing the amount of capacitive load and adjusting the dominant pole appropriately? The answer is yes, and the solution can be seen in Figure 3.1, where a capacitor C_C has been connected between the gain stage and output of an op-amp.

First, consider a light load on the output (high R_L, low C_L). Driving this load, the two voltages V_{OUT} and V_{HIZ} should track each other closely, and no current will flow thru the R_cC_c combination. The compensation network does no work in this case, and we get the normal amplifier response as given by Curve A in Figure 3.2. Now suppose we raise C_L to some high value. The voltage V_{OUT} will not follow V_{HIZ} as closely, and current begins to flow in the R_cC_c network.

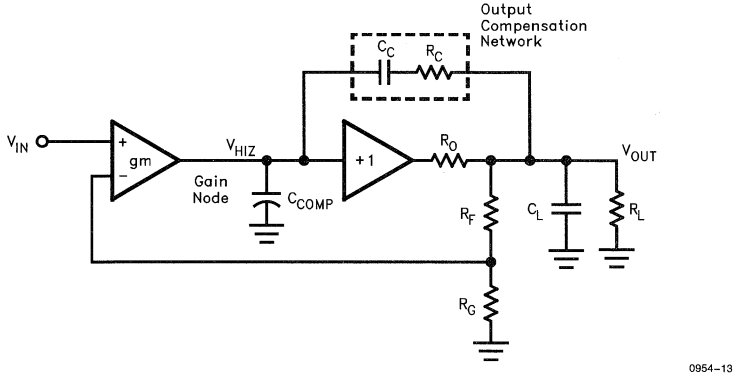


Figure 3.1. Compensation Scheme To Make Op-Amps More Tolerant of Capacitive Loads

This in effect puts part of C_C on the gain node, thus lowering the bandwidth of the amplifier. Curve B in Figure 3.2 shows what the response may look like in this case. On the other hand, Curve C shows what will happen if we did not use the compensation network to drive a large C_L; although we retain the bandwidth, severe peaking occurs.

This technique does have its drawback: the bandwidth reduces for heavy loads in general. Thus, the bandwidth lowers for heavy resistive loading as well, which is an undesirable trait. In addition, this technique degrades the RF linearity of the amplifier, ruining such performance parameters as differential gain and phase.

External Compensation—Series Resistor

To avoid sacrificing performance, most of Elantec's op-amps are not heavily compensated for capacitive loads. The use of external compensation networks may be required to optimize certain applications. Figure 3.3 shows one such network, where we have inserted a series resistor with the op-amp's output. The stabilizing effect of this resistor can be thought of in two ways. One is that R_{SERIES} serves to isolate the op-amp output and feedback network from the capacitive load. The other way to think about it is to recall the superinductor concept introduced earlier. Since the output stage presents a negative resistance over certain frequencies, adding enough series resistance would cancel this negative resistance and prevent oscillation.

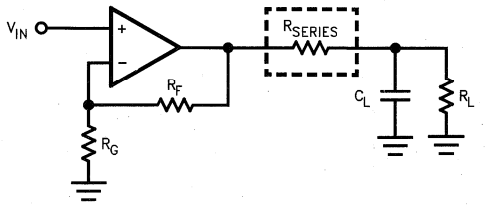


Figure 3.3. Series Resistor Compensation To Stabilize an Op-Amp Driving Capacitive Loads

The required amount of series resistance depends on the part used, but values of 5Ω to 15Ω is usually sufficient to prevent local resonances. The disadvantage of this technique is a reduction in gain accuracy, and extra distortion when driving nonlinear loads.

External Compensation—The Snubber

Another way to stabilize an op-amp driving a capacitive load is the use of a snubber, as shown in Figure 3.4. To see how a snubber can reduce peaking, consider the 300 MHz f_T transistor presented in Section 2. For that example, the output inductance of the emitter follower was shown to be 100 nH. With a light resistive load $R_L = 1\ k\Omega$ and moderate capacitive load $C_L = 50$ pF, the circuit resonates at 70 MHz with a Q given by:

$$Q = \frac{R_L}{\sqrt{\frac{L}{C_L}}}$$

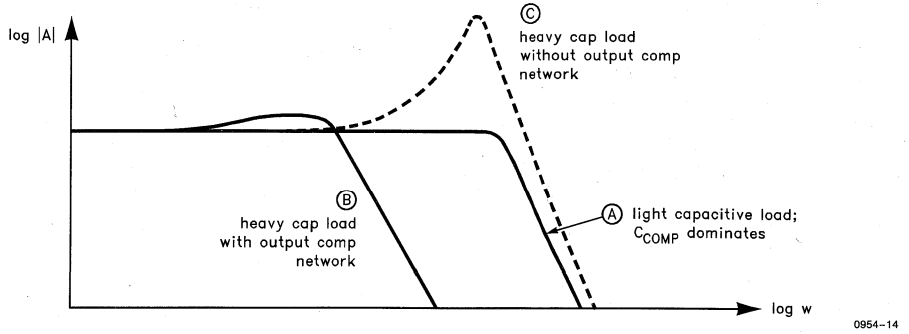


Figure 3.2. Effects of Compensation Scheme Shown in Figure 3.1

Driving Reactive Loads with High Frequency Op-Amps

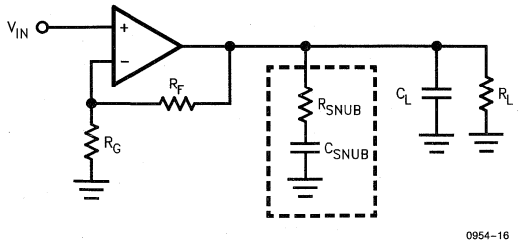


Figure 3.4. The Snubber

In this case, Q works out to be about 22, giving us severe peaking in the frequency response. However, with a load of 150Ω, the Q reduces to 3. Thus the extra stabillty gained with a heavy load resistor is desirable, but we may be wasting DC load current with this approach. A way around this is to insert a capacitor in series with the resistor, resulting in a snubber.

There are various ways to determine appropriate values for R_{SNUB} and C_{SNUB}, one of which is presented in [2]. We will describe an alternative method here. First, operate the amplifier as in the intended application and look at its frequency response on a network analyzer. Find the frequency at which the peak occurs, and denote that as f_p. Next, try loading the amplifier with different load resistances until the peaking reduces to a satisfactory level; this value will be R_{SNUB}. Finally, we need a capacitor that will make the snubber look resistive at the frequency of the peak. A rough guideline is to make the snubber zero frequency 3 times lower than f_p, resulting in the following design equation:

$$C_{SNUB} = \frac{3}{2\pi \bullet f_p \bullet R_{SNUB}}$$

Note that as opposed to the series resistor method, the use of a snubber does not degrade the gain accuracy or cause extra distortion when driving a nonlinear load.

Unterminated Coaxial Lines

As we may have hinted earlier, unterminated coaxial lines mean trouble. The simple remedy for this is to terminate the line in its characteristic impedance, and the cable will look like a stable resistive load to the driving amplifier.

In certain cases the cable termination may be unknown, or it may not be under our control at all times. A good example of this is in ATE systems, where an amplifier drives a signal through a coaxial cable to a test pin. However, when a device under test is not plugged in, the test pin is left unterminated, and so the amplifier is driving into an open cable. Figure 3.5 shows how we can use back-matching to solve this problem. In back-matching, we insert a resistor R_{BM} equal to the cable's characteristic impedance between the amplifier and the cable. R_{BM} serves to isolate the amplifier from the cable, the impedance of which could wildly vary with frequency. Also, since R_{BM} terminates the cable at the source end, reflected signals are absorbed in R_{BM}, preventing multiple reflections from occurring.

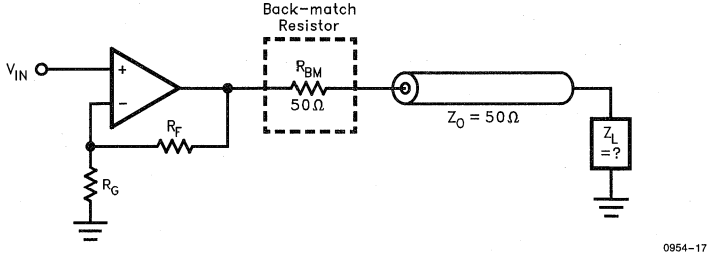


Figure 3.5. Backmatching

4.0 Summary

High frequency op-amps are sensitive to capacitive loads due to the loss of phase margin in driving these loads. In addition, the op-amp output stage can introduce its own resonance, further complicating the stability issue. These problems can introduce severe peaking in the frequency response or excessive ringing in the transient response. Some recent op-amp designs have incorporated an internal compensation network for capacitive loads. Such op-amps, however, sacrifice bandwidth and RF linearity in return for foolproof usage. For the best performance, amplifiers without the internal compensation network should be used in conjunction with a snubber when necessary. Proper bypassing and board layout have not been stressed in this application note, but they are equally important to the well-being of a high speed op-amp.

References

1. Cheng, David K., *Field and Wave Electromagnetics*, Addison-Wesley: New York, 1989.
2. Siegel, Barry. "High Frequency Amplifier Instability". Elantec, October 1992.

Current Boosted and DC Stabilized Half Bridge Driver

by Les Mills

Following are two applications notes for the EL7661 half bridge driver.

1. The current boosted half bridge driver offers the control functions of the EL7661 with enhanced drive capability. For example an application with V_S = 16V, a 25 ns turn on time and a 3000 pF load would require I_{PK} = (V_S + V_{GS}) * C/T_{ON} = (16 + 10) * 3000 pF/25 ns = 3.12A peak current from the driver. Since the EL7761 specifies I_{PK} = 1A typical, the output requires current boosting to achieve the desired turn on time. This circuit is also useful in applications where the switching time is less stringent or the load is lighter but the output is required to swing over a greater range due to higher supplies voltages.

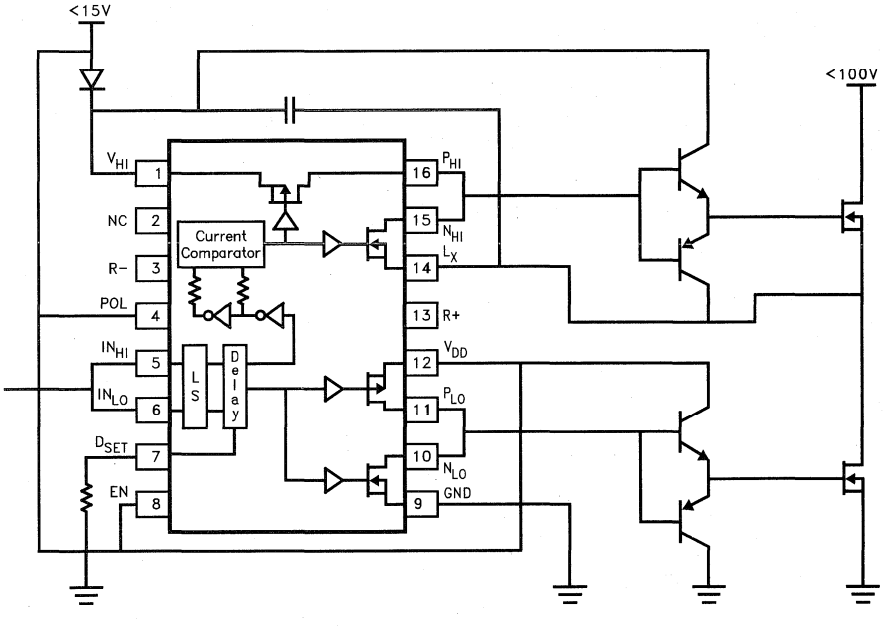


Figure 1. EL7661 Half Bridge Driver with Output Current Boost

2. DC stabilization of the half bridge driver is achieved by charge pumping the high side supply storage capacitor while the output is in the high state. This keeps the top half of the circuit (V_{DD} to L_X) biased at 12V when a 12V Zener is used as shown. The Zener should be 15V or less. The EL7232 was selected for the oscillator since its output must swing between GND and the 16V supply and provide a minimum of 10 mA, the supply current of the EL7761. The EL7232 is capable of 1.5A peak. Any driver providing 30 mA, swinging between GND and the 16V supply would also be suitable.

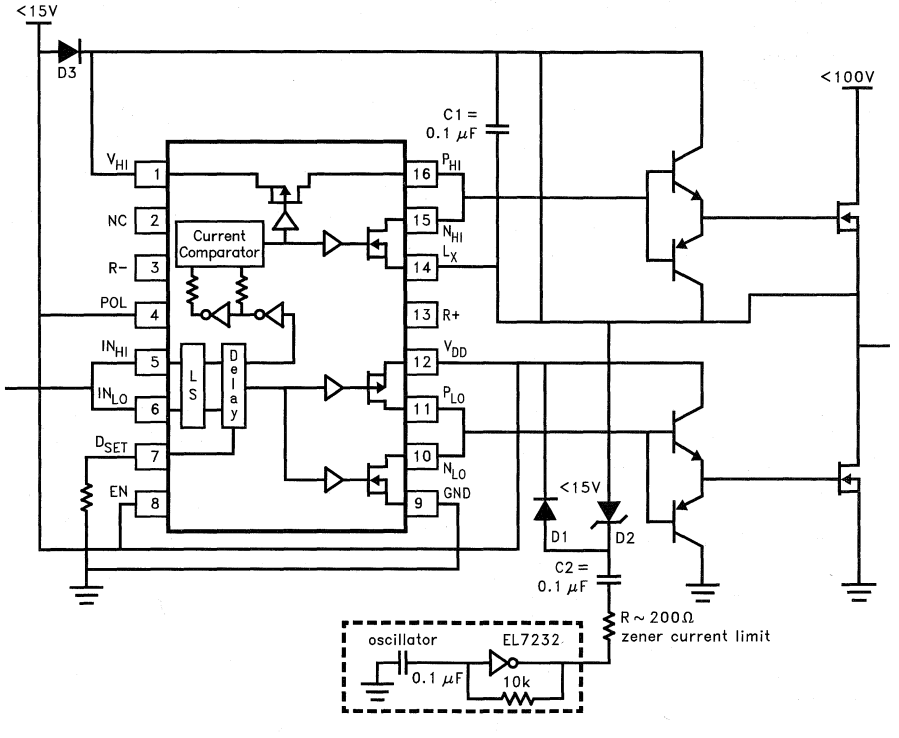


Figure 2. EL7661 Half Bridge Driver DC Stabilized with Output Current Boost

25 kHz Electronic Ballast Using The EL7981 Delay Driver

by Bruce Rosenthal

Introduction

Electronic ballasts are rapidly gaining market acceptance, as ballast prices drop, electrical rates increase, and performance improves. Their primary advantages are: (1) the elimination of flicker, and noise (hum), (2) increased efficiency resulting in a cost advantage, and (3) reduces size and weight. The EL7981 is particularly well suited for this application by using the programmable delay and high current drive features.

System Operation

The ballast, in many respects, resembles an OFF-LINE Switch-Mode Power Supply. The 120 VAC line is rectified and doubled, developing ≅ 300 VDC rail-to-rail. When the intensity switch is set to "Low", the doubler is eliminated, and 150 VDC is produced. A "half bridge" configuration, using (2) Power MOSFET's drives an LC resonant circuit, with sufficient "Q" to develop the necessary starting voltage. The resulting current and voltage to the lamp are sinusoidal. Isolated drive to the FET's is provided with a transformer coupled from EL7981 Dual Delay Driver. The delay function allows for the "Recovery Time" of the parasitic diodes in the Power Mosfet's. A 555 timer generates the desired clock frequency. The clock can be tuned to the resonant frequency of the series L-C network. For tutorial reasons, auxillary power for the clock and driver were supplied externally, however, in practice a simple charge-pump can be used to develop the 10V supply.

Lamp

The "F40" 40 watt, 48" flourescent lamp was selected for its popularity, and low cost. Above 20 kHz, these flourescent lamps behave like a 300Ω resistor because the plasma is maintained. The "striking" voltage for a cold tube is around 400V, however, this can be reduced by supplying current to the starter filament. Additional lamps can be added, but require separate L-C networks. 25 kHz operation was chosen, because it's above the audible range, yet not so high, that switching losses would be of concern. Increased lamp life has been reported by operating at these frequencies compared to 50 Hz–60 Hz.

EL7981

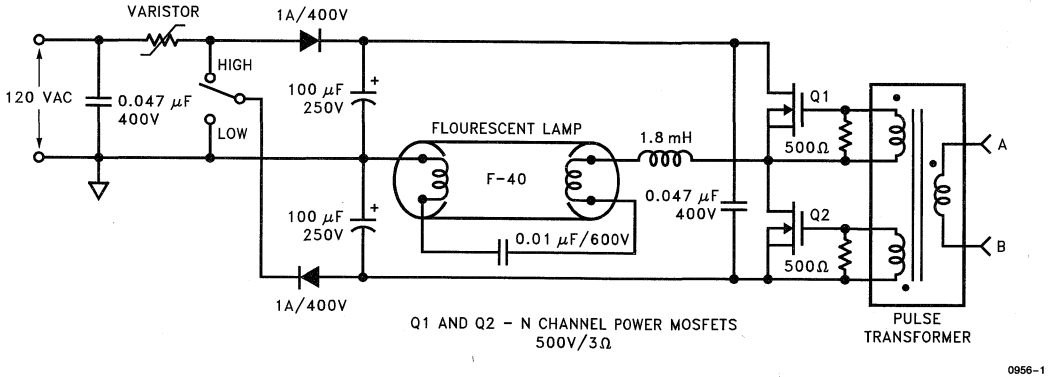
The EL7981 Dual Delay Driver generates a programmable delay to the rising edge of the output waveforms. Each output has a nominal "ON" resistance of 5Ω, and can source and sink 1A. With R_{SET} = 300 kΩ, the delay is about 1.5 μs, which provides sufficient time for the parasitic diodes in the FET's to recover. The strong output devices are suitable for driving the "Gate" transformer directly. The resulting gate drive waveform has (3) distinct levels: −10V, 0V, +10V.

Magnetics

The two magnetic components of the Ballast are (1) the gate transformer, and (2) the output resonating inductor. The output inductor is rated at 1.8 mH (Magnetic Circuit Elements Inc. #OC25BL25). The gate transformer is wound 1:1:1 and is tightly coupled to provide fast switching. (Magnetic Circuit Elements Inc. #0-1853T1). For further information on these components, contact John Conklin at Magnetic Circuit Elements (408) 757-8752.

25 kHz Electronic Ballast Using The EL7981 Delay Driver

Electronic Ballast (Power Mesh)



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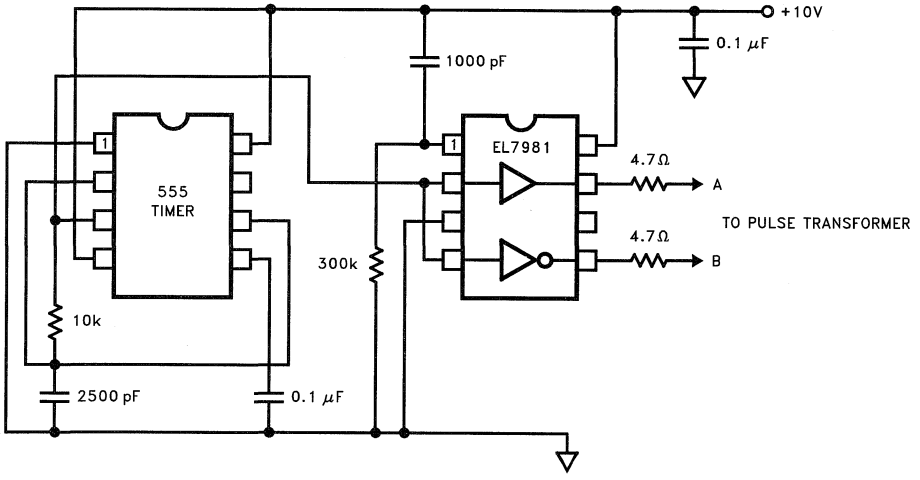
Electronic Ballast (Gate Drive Circuit)



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Technical assistance for a new application is a toll free phone call away. Call 1 (800) 333-6314 and touch or request extension 311. Probably the most important information that Elantec needs to assist you is a clear picture of what the circuit needs to do. What we mean by that is the cost and performance objectives of the circuit or system. If you have a preliminary topology or schematic, feel free to FAX that to the Factory at 1 (408) 945-9305 in confidence. The following is a check list which will expedite our assistance to you:

What does the circuit need to do?

What power supply voltages are available?

What is the temperature range?

What is the load?

What are the key specs: bandwidth, slew rate, settling time, noise, output voltage, etc. and what are your expectations?

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Applications assistance for an existing application is a toll free phone call away. Call 1 (800) 333-6314 and touch or request extension 311. Probably the most important information that Elantec needs to assist you is a clear picture of what the circuit is doing or not doing. The following is a check list which will expedite our assistance to you:

What is the part number?

What is the device's date code?

What are the symptoms?

Are scope photos or frequency plots available?

How many devices are involved?

Unreleased Product

As a general rule, Elantec does not sample new devices that have not completed our rigorous formal release cycle. However, occasionally we will "beta " site customers with advanced Engineering samples. We view this as a productive exchange between our Factory and customer Engineering teams to pin point problems and issues. In all instances, these devices will be marked "Engineering Sample." If you are interested in such a device, call your nearest Elantec sales office, local sales representative, or the Factory at 1 (800) 333-6314 and touch or request extension 252.

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Package Outlines

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Soldering Packages to PC Boards

DIP Packages

Wave soldering is recommended for DIP packages. Elantec's DIP packages will survive a peak temperature of 300°C (at leads) for 10 seconds. Solder plated are recommended. Rosin mildly activated (RMA) flux or organic flux is needed. Wave soldering using a dual wave system at 250°C ±10°C for 2 seconds per wave is preferable. Thorough cleaning of boards after soldering is required.

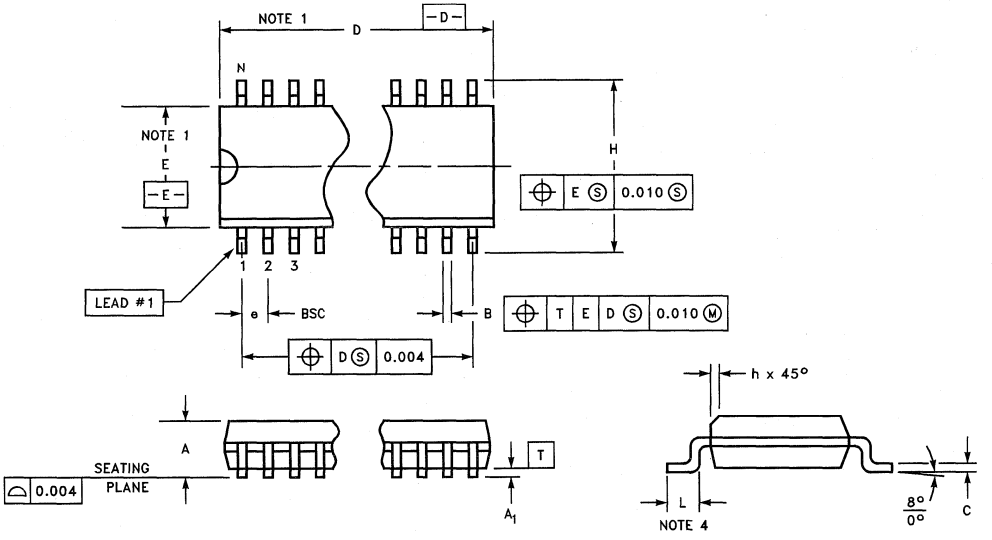
Surface Mount Packages

Wave soldering and vapor phase or infrared (IR) reflow can be used for soldering surface mount packages. Elantec's surface mount packages will withstand 260°C for 10 seconds. Solder plated boards are recommended for wave soldering and vapor phase or IR reflow methods.

Wave Soldering: Adhesive is used to hold components on the boards during wave soldering. Place components on the board and cure adhesive before wave soldering. Rosin mildly activated (RMA) flux or organic flux is needed. Wave soldering using a dual wave system at 250°C ±10°C for 2 seconds per wave is preferable. Thorough cleaning of boards after soldering is required.

Reflow Soldering: Screen solder paste on board and attach components to board. Solder paste with RMA flux is recommended. Bake the boards at 65°C–90°C for 15 minutes. Reflow solder paste with vapor phase or IR reflow systems. The solder paste temperature must be maintained at or above 200°C for at least 30 seconds. Clean boards to remove flux.

Package Outlines

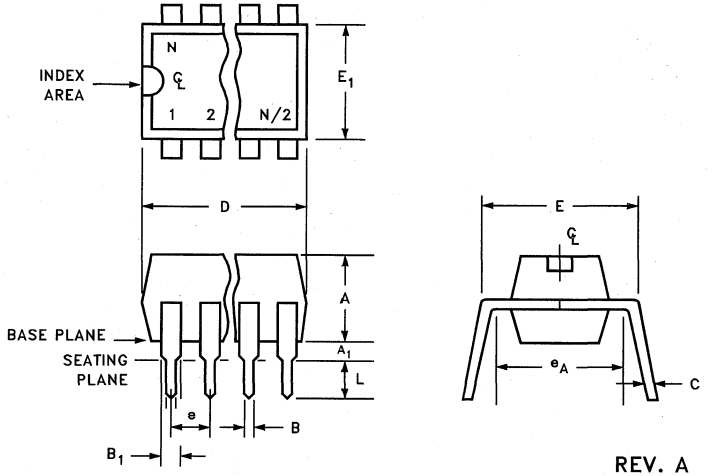


REV. C

Note 1: These dimensions do not include mold flash or protrusions. Mold flash protrusion shall not exceed .006" on any side.
Note 2: 8 and 14 leads are narrow body.
Note 3: Dimensions and tolerancing per ANSI Y14.5M-1982.
Note 4: Flat area of lead foot.
Note 5: SOL-24T2 (thermal package) has 2 fused leads on each side of package.

MDP0027 Rev. C
Package Outline—SOIC
Lead Finish—Solder Plate

Symbol	Lead Count													
	SOL-28		SOL-20		SOL-16		SO-16		SO-14		SO-8		SOL-24	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.096	0.104	0.096	0.104	0.096	0.104	0.061	0.068	0.061	0.068	0.061	0.068	0.096	0.104
A_1	0.004	0.011	0.004	0.011	0.004	0.011	0.004	0.010	0.004	0.010	0.004	0.010	0.004	0.011
B	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019
C	0.009	0.012	0.009	0.012	0.009	0.012	0.008	0.010	0.008	0.010	0.008	0.010	0.009	0.012
D	0.696	0.712	0.498	0.510	0.397	0.430	0.386	0.394	0.337	0.344	0.189	0.196	0.598	0.614
E	0.291	0.299	0.291	0.299	0.291	0.299	0.150	0.157	0.150	0.157	0.150	0.157	0.291	0.299
e	0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC	
H	0.398	0.414	0.398	0.414	0.398	0.414	0.230	0.244	0.230	0.244	0.230	0.244	0.398	0.414
h	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016
L	0.016	0.024	0.016	0.024	0.016	0.024	0.016	0.024	0.016	0.024	0.016	0.024	0.016	0.024



MDP0031 Rev. A
Plastic Package
Lead Finish—Hot Solder DIP

Common Dimensions	Min	Max	Min	Max	Min	Max	Min	Max
A_1	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040
A	0.125	0.145	0.125	0.145	0.125	0.145	0.125	0.145
B	0.016	0.020	0.016	0.020	0.016	0.020	0.015	0.021
B_1	0.050	0.070	0.050	0.070	0.050	0.070	0.050	0.070
C	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
D	0.350	0.385	0.750	0.770	0.745	0.755	0.925	1.045
E	0.290	0.310	0.300	0.320	0.300	0.325	0.300	0.320
E_1	0.245	0.255	0.245	0.255	0.245	0.255	0.245	0.255
e	0.100 Typ		0.100 Typ		0.100 Typ		0.100 Typ	
e_A	0.300 Ref		0.300 Ref		0.300 Ref		0.300 Ref	
L	0.130	0.150	0.115	0.150	0.125	0.150	0.130	0.150
N	8		14		16		20	

Ordering Information

élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Ordering Information

In North America, Elantec has three levels of sales support. Regional Sales Managers are located in the Boston and San Jose areas. Field Applications Engineers are located in the Boston and San Jose offices. Elantec also maintains a network of sales representatives covering the United States and Canada. Finally, major nationwide and regional distributors provide local stock. Elantec maintains an up-to-date distributor inventory status and provides an inventory referral service through Distribution Sales in San Jose. Orders may be placed through the sales representatives or distributors. A list of sales representatives and distributors is included with this Elantec 1994 Databook, or please contact any of the regional sales offices.

In Europe, Elantec has a Regional Sales Office in London. Local sales support is provided through stocking representatives in all of the major countries. A current list of representatives and distributors may be obtained from the London office.

Elantec has stocking agents in all Pacific Rim Countries, Australia, and New Zealand. A list may be obtained from Elantec's headquarters in Milpitas, California.

In Asia, Elantec has a regional sales office in Tokyo. Local sales support is provided through stocking representatives in all of the major countries. A current list of representatives may be obtained by contacting the Tokyo sales office.

Elantec Proprietary and NSC Alternate Source

E L 2006 A G /883B

PREFIX
ELANTEC

FAMILY
LH NSC Alternate Source
L Proprietary Linear
P PNP Array
N NPN Array

PART NUMBER

OPTIONAL SUFFIX
A Selected Electrical Performance
C −0°C to +75°C or −40°C to +85°C
E −40°C to +150°C
None −55°C to +125°C

RELIABILITY PROGRAM
/883B 100% MIL-STD-883 Class B, Current Revision Processing

PACKAGE
B Sidebraze
G TO-8 Metal Can
H TO-5 or TO-99 Metal Can
J CerDIP
K TO-3
N Plastic DIP
T TO-220
M Large Body SOIC
S Narrow Body SOIC

Terms and Conditions of Sale

élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

ELANTEC, INCORPORATED ("SELLER") TERMS AND CONDITIONS OF SALE

1. ACCEPTANCE OF ORDER

THIS ACKNOWLEDGEMENT AND ACCEPTANCE IS EXPRESSLY LIMITED TO AND MADE CONDITIONAL UPON THE TERMS AND CONDITIONS CONTAINED HEREIN AND ANY OF THE BUYER'S TERMS AND CONDITIONS WHICH ARE IN ADDITION TO OR DIFFERENT FROM THOSE CONTAIN HEREIN WHICH ARE NOT SEPARATELY AND SPECIFICALLY AGREED TO IN WRITING ARE HEREBY OBJECTED TO AND SHALL BE OF NO EFFECT.

Only those orders accepted by Seller as its home office in Milpitas, California shall be binding upon Seller.

2. PRICES

Irrespective of any prices quoted by Seller or listed on Buyer's order, Seller's acceptance of any order is subject to the prices shown on Seller's acknowledgment. Said prices are firm and are not subject to adjustment other that "precious metals adjustments" or "precious metals surcharges" at Seller's option to cover Seller's cost of fluctuations in the price of precious metals utilized in the manufacture of Seller's products.

3. TAXES

All prices are exclusive of all federal, state and local excise, sales, use and similar taxes. Such taxes shall be paid by Buyer, or in lieu thereof Buyer shall provide Seller with a tax exemption certificate acceptable to the taxing authorities. When applicable, such taxes will appear as separate additional items on the invoice unless Seller receives a proper tax-exemption certificate from Buyer prior to shipment.

4. PAYMENT

Unless Seller has extended credit to Buyer as described below, Buyer shall pay Seller, at Seller's option either by: Cash with Order, C.O.D., Letter of Credit or Sight Draft.

Should Seller elect to extend credit to Buyer, payment shall be made in full within thirty (30) days of the date of Seller's invoice. Seller reserves the right at any time to change the amount of or to withdraw any credit extended to Buyer.

Any payments made in excess of thirty (30) days may be subject to late charges.

5. TITLE AND DELIVERY

Seller shall deliver products sold hereunder to Buyer F.O.B. Seller's factory. Partial deliveries shall be permitted. Upon such delivery to a carrier at Seller's factory, title to the products and all risk of loss or damage shall pass to Buyer.

6. SHIPMENT

All shipping charges and expenses shall be paid by Buyer. Seller will not insure the products sold hereunder unless requested by Buyer in which case Buyer will pay for such insurance.

Shipments will be made, at Seller's option, either by Parcel Post, Railway Express. Air Express, Air Freight, or as otherwise determined by Seller.

Shipping dates are approximate and are dependent upon Seller's prompt receipt of all necessary information from Buyer.

7. PATENTS

With respect to products manufactured soley to Seller's designs and specifications, Seller shall defend any suit or proceeding brought against Buyer insofar as such suit or proceeding is based on a claim that any such products furnished hereunder infringe any patent of the United States. If Seller is notified promptly in writing of such suit or proceeding and given full and complete authority, information, and assistance by Buyer for such defense, Seller shall pay all damages and costs finally awarded against Buyer in any such suit or proceeding, but Seller shall not be responsible for any compromise thereof made by Buyer without the written consent of Seller. In the event that such products are held in such suit or proceeding to infringe a patent of the United States and their use is enjoined, or if in the opin-

Terms and Conditions

ion of Seller such products are likely to become the subject of a claim of infringement of a patent of the United States, Seller, in its sole discretion and at its won expense, may either: (a) procedure for Buyer the right to continue using such products with noninfringing products; or (b) modify such products so that they become noninfringing; or (c) replace such products with noninfringing products; or (d) accept the return of such products, granting Buyer a refund therefor equal to the depreciated value thereof.

Seller shall have no liability to Buyer under any provision hereof if any patent infringement or claim thereof is based upon (a) a modification of the products not introduced by or approved by Seller; or (b) the interconnection or use of the products in combination with products with other devices not made by Seller; or (c) the use of the products in other than an application recommended by Seller.

The foregoing states the entire liability of Seller for infringement of patents by Seller's products or any part(s) thereof.

8. INDEMNITY

Buyer shall indemnify, defend, and hold Seller harmless from and against any and all liability, damages, expenses, costs or losses resulting from any suit or proceeding brought for infringement of a patent(s), copyright(s), or trademark(s), or for a misappropriation of use of any trade secret(s), or for unfair competition arising from Seller's compliance with Buyer's design, specifications or instructions.

9. SECURITY INTEREST

Notwithstanding passage of title of products sold hereunder to Buyer F.O.B. Seller's factory, Seller shall retaln a security interest in the products until payment has been made in full by Buyer for such products. Buyer shall perform all acts necessary to perfect and maintaln such security interest.

10. WARRANTIES

Seller warrants to Buyer that Seller's standard products sold hereunder (and any services furnished therewith) which are not used in any medical or life support application shall be free from defects in material and workmanship and shall conform to the applicable specifications (if any) for a period of one year from the date of shipment. For products which are not standard products of Seller, such as dice and developmental or custom designed products. Seller warrants to Buyer that such products sold hereunder (and any services furnished therewith) shall be free from defects in material and workmanship and shall conform to the applicable specifications (if any) for a period of thirty (30) days from the date of shipment.

Should products sold hereunder fall to meet the above applicable warranty, Seller, at its option, shall repair or replace such products or issue Buyer a credit provided that (a) Seller is notified in writing by Buyer within thirty (30) days after discovery of such failure; (b)Buyer obtains a Return Material Authorization from Seller prior to returning any defective products to Seller; (c) the defective products are returned to Seller, transportations charges prepaid by Buyer; (d) the defective products are received by Seller for adjustment no later than four (4) weeks following the last day of the warranty period, and (e) Seller's examination of such products shall disclose, to its satisfaction, that such failures have not been caused by misuse, abuse, neglect, improper installation or application repair, alteration, accident or negligency in use, storage, transportation or handling.

In the event of failure to meet the above applicable warranty with respect to products sold hereunder cannot be corrected by Seller's reasonable efforts, the Seller and Buyer shall negotiate an equitable adjustment in price.

The foregoing warranty provisions set forth the Seller's sole liability and the Buyer's exclusive remedies for claims (except as to title) based on defects in or failure of any products sold hereunder or services furnished hereunder whether the claim is based in contact, tort, (including negligence), warranty or otherwise and however instituted. Upon the expiration of the applicable warranty for any products sold hereunder, all such liability shall terminate.

The above warranty periods shall not be extended by the repair or replacement of products pursuant to any of the above warranties. The above warranties shall apply only to Buyer and shall not apply to Buyer's customers or any other third parties.

SELLER PRODUCTS ARE NOT DESIGNED FOR AND SHOULD NOT BE USED WITHIN LIFE SUPPORT SYSTEMS WITHOUT THE SPECIFIC WRITTEN CONSENT OF THE PRESIDENT OF ELANTEC. LIFE SUPPORT SYSTEMS ARE EQUIPMENT INTENDED TO SUPPORT OR SUSTAIN LIFE AND WHOSE FAILURE TO PERFORM WHEN PROPERLY USED IN ACCORDANCE WITH INSTRUCTIONS PROVIDED CAN BE REASONABLY EXPECTED TO RESULT IN SIGNIFICANT PERSONAL INJURY OR DEATH. USERS CONTEMPLATING APPLICATION OF SELLER PRODUCTS IN LIFE SUPPORT SYSTEMS ARE REQUESTED TO CONTACT SELLER FACTORY HEADQUARTERS TO ESTABLISH SUITABLE TERMS AND CONDITIONS FOR THESE APPLICATIONS. SELLER'S WARRANTY IS LIMITED TO REPLACEMENT OF DEFECTIVE COMPONENTS AND DOES NOT COVER INJURY TO PERSONS OR PROPERTY OR OTHER CONSEQUENTIAL DAMAGES.

11. LIMITATION OF LIABILITY

In no event, whether as a result of breach of contract, warranty or tort (including negligence) or otherwise shall Seller be liable for any special, consequential, incidental or penal damages, including but not limited to, loss of profit or revenues, loss of the product or any associated equipment, damaged to associated equipment, cost of captial, cost of substitute products, facilities, service or replacement power, down time costs or claims of Buyer's customers for such damages. If Buyer transfers title to or leases products sold hereunder to any third party, Buyer shall obtain from such third party a provision affording the Seller the protection of the preceding sentence.

Except as provided in the above "Patents" article, whether a claim is based in contract, tort (including negligence) or otherwise, the Seller's liability for any loss or damage arising out of, or resulting from any products sold hereunder or services furnished hereunder shall in no case exceed the price of the specific product(s) or service(s) which gives rise to the claim. Except as to title, any such liability shall terminate upon the expiration of the applicable warranty period specified in the above "Warranties" article.

12. U.S. GOVERNMENT CONTRACTS

If the products to be furnished hereunder are to be used in the performance of a U.S. Government contract or subcontract, no Government requirments or regulations shall be binding upon Seller unless specifically agreed to by Seller in writing.

If the Government terminates such a contract or subcontract in whole or in part through no fault of or failure to perform by Buyer, this order may be canceled in writing in the same proportion, and the liability of Buyer for termination allowances shall be determined by the then applicable regulations of the Government regarding termination of contracts.

13. EXCUSABLE DELAYS

Seller shall not be liable for delays in delivery or performance due to any cause beyond its reasonable control, including, without limitation, acts of God, acts of Buyer, strikes or other labor disturbances, inability to obtain necessary materials, components, services or facilities.

14. CANCELLATIONS OF STANDARD PRODUCTS

Should Buyer terminate any order accepted hereunder or should Seller terminate any order accepted hereunder due to Buyer's nonperformance of its obligations hereunder, then Buyer shall pay Seller its reasonable termination charges within fifteen (15) days from the date of invoice of same.

Buyer may request rescheduling or cancellation by providing thirty (30) days written notice to Elantec provided however, that elantec is not obligated to accept such notice, but if such notice is given and accepted by Elantec, then Elantec has the right to deliver and be paid by Buyer for:

1. 100% of quantity of devices scheduled for delivery within thirty (30) days following receipt of said notice.

2. 50% of quantity of devices scheduled for delivery within 30–60 days following receipt of said notice.

15. CANCELLATION OF PRODUCTS MANUFACTURED TO BUYER'S DESIGN/SPECIFICATIONS INCLUDING ALL NON-STANDARD AND DISK DRIVE PRODUCTS

Charge for engineering, design, generation of data, lot charges or any other special charges that are not for product are non-cancelable except with prior written permission from Seller.

Buyer may request rescheduling or cancellation of product by providing 60 day notice to Elantec provided, however, that Elantec is not obligated to accept such notice but if such notice is given and is accepted by Elantec, then Elantec has the right to deliver and be paid by the Buyer for:

1. 100% quantity within 60 days following written receipt of said notice;
2. All additional work in process scheduled within the 16 week delivery time period shall be paid for by Buyer at a price based on the percentage of completion of such inventory applied to the price for the finished product. Buyer shall also promptly pay to Elantec; (a) costs of settling and paying claims arising out of termination of work under Elantec's subcontracts or vendors; (b) reasonable costs of settlement, including engineering, development, accounting, legal and clerical costs; (c) twenty percent (20%) of the purchase price of the purchase order to be canceled.

16. ASSIGNMENT

Any assignment by Buyer of this order or of any rights or obligations in connection therewith shall be void without the written prior consent of the Seller.

17. EXPORT TO NON-APPROVED COUNTRIES

Buyer agrees to take all reasonable and necessary precautions to prevent ultimate exportation of Elantec products to countries prohibited by rules or regulations of the United States Government, and to obtain all export licenses and other governmental approvals necessary prior to the export of any Elantec products.

18. MISCELLANEOUS

The validity, performance and construction of these terms and conditions of sale and any sale hereunder shall be governed by the laws of the state of California.

The invalidity, in whole or in part, of a y provision herein shall not affect the validity or enforce ability of any other provision herein.

Any representation, warranty, course of dealing or trade usage not contained or referenced herein shall not be binding on Seller.

No modification, amendment, recision, waiver or other change in these terms and conditions shall be binding on Seller unless assented to in writing by Seller's duly authorized representative.

Seller reserves the right to manufacture and/or assemble its products in any of its worldwide facilities unless otherwise agreed to in writing with Buyer.

Sales Representatives and Distributors

élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

United States Manufacturers Representatives

ALABAMA
Group 2000 Sales, Inc
655 Gallatin St #100
Huntsville, AL 35801
PHONE 205-536-2000
FAX 205-533-5525

ARIZONA
Reptronix, Ltd
1661 E. Camelback Rd
Phoenix, AZ 85016
PHONE 602-230-2630
FAX 602-230-7730

CALIFORNIA
Bestronics
9683 Tierra Grande St #102
San Diego, CA 92126
PHONE 619-693-1111
FAX 619-693-1963

Brooks Technical Group
883 North Shoreline Blvd
Mountain View, CA 94043
PHONE 415-960-3880
FAX 415-960-3615

Parsons Technical Marketing
10112 Fair Oaks Blvd #4
Fair Oaks, CA 95628
PHONE 916-965-3255
FAX 916-965-4204

Westrep
2557 West Woodland Dr
Anaheim, CA 92801
PHONE 714-527-2822
FAX 714-527-3868

COLORADO
Thom Luke Sales
9000 E. Nichols Ave #240
Englewood, CO 80112
PHONE 303-649-9717
FAX 303-649-9719

CONNECTICUT
John E. Boeing
101 Harvest Pk No Bldg 1A
Wallingford, CT 06492
PHONE 203-265-1318
FAX 203-265-0235

FLORIDA
Naltron Corp
Lincoln Center
5401 W. Kennedy Blvd #992
Tampa, FL 33609
PHONE 813-287-1433
FAX 813-287-1746

GEORGIA
Group 2000 Sales, Inc
655 Engineering Dr #140
Norcross, GA 30092
PHONE 404-729-1889
FAX 404-729-1896

IDAHO
First Source
10451 W. Garverdale Ct #209
Boise, ID 83704
PHONE 208-378-4680
FAX 208-323-9386

ILLINOIS
Mid Star Technologies
2268 B Landmeier Rd
Elk Grove Village, IL 60007
PHONE 708-427-2300
FAX 708-427-0121

INDIANA
Mohrfield Marketing
4173 Millersville Rd
Indianapolis, IN 46205
PHONE 317-546-6969
FAX 317-545-4504

United States Manufacturers Representatives — Contd.

INDIANA — Contd.

Morfield Marketing, Inc
9415 Teke Dr
Leo, IN 46765
PHONE 219-627-5355
FAX 219-627-2953

KANSAS

Midtec Associates, Inc
11900 W. 87th St Pkwy #220
Lenexa, KS 66215
PHONE 913-541-0505
FAX 913-541-1729

KENTUCKY

Mohrfield Marketing, Inc
191 W. Lowry Ln #A
Lexington, KY 40504
PHONE 606-277-7990
FAX 606-278-1278

MARYLAND

DGR
1447 York Rd #401
Lutherville, MD 21093
PHONE 410-583-1360
FAX 410-825-5579

MASSACHUSETTS

John E. Boeing
10 North Rd
Chelmsford, MA 01824
PHONE 508-256-5800
FAX 508-256-8939

MICHIGAN

Electronic Sources Inc
8002 W. Grand River Ave #B
Brighton, Ml 48116
PHONE 810-227-3598
FAX 810-227-5655

MINNESOTA

High Technology Sls
4801 W. 81st St #115
Bloomington, MN 55437
PHONE 612-844-9933
FAX 612-844-9930

MISSOURI

Midtec Associates, Inc
55 Westport Plaza #614
St. Louis, MO 63146
PHONE 314-275-8666
FAX 314-275-8859

NEW JERSEY

BGR Associates
525 Route 73 Suite 100
Marlton, NJ 08053
PHONE 609-983-1020
FAX 609-983-1879

NEW MEXICO

Reptronix Ltd.
237 C Eubank North East
Albuquerque, NM 87123
PHONE 505-292-1718
FAX 505-299-1611

NEW YORK

Astrorep Inc
103 Cooper St
Babylon, NY 11702
PHONE 516-422-2500
FAX 516-422-2504

CTC Associates
1063 Killoe Rd
Baldwinsville, NY 13027
PHONE 315-638-9232
FAX 315-638-7410

NORTH CAROLINA

Group 2000 Sales, Inc
875 Walnut St #310
Cary, NC 27511
PHONE 919-481-1530
FAX 919-481-1958

OHIO

Mid Star Technologies
35 Compark Rd #204
Centerville, OH 45458
PHONE 513-439-5700
FAX 513-439-5657

United States Manufacturers Representatives — Contd.

OREGON

Electronic Solutions
P.O. Box 91428
Portland, OR 97291
PHONE 503-292-8204
FAX 503-423-8005

TEXAS

O M Associates
690 W. Campbell Rd #150
Richardson, TX 75080
PHONE 214-690-6746
FAX 214-690-8721

O M Associates
20405 S.H. 249 #170
Houston, TX 77070
PHONE 713-376-6400
FAX 713-376-6490

O M Associates
11044 Research Blvd #A103
Austin, TX 78759
PHONE 512-794-9971
FAX 512-794-9987

UTAH

First Source
2688 Willow Bend
Sandy, UT 84093
PHONE 801-943-6894
FAX 801-943-6896

WASHINGTON

E2
13333 Bel-Red Rd Suite 239
Bellevue, WA 98005
PHONE 206-637-0302
FAX 206-646-8893

WISCONSIN

Selective Sales
143 E. Capital Dr
Hartland, WI 53029
PHONE 414-367-1133
FAX 414-367-3842

Canadian Manufacturers Representatives

BRITISH COLUMBIA

Leister Blake Enterprises Ltd
570 Ballantree Rd
West Vancover, B. C. V7S 1W3
PHONE 604-926-6127
FAX 604-926-0372

ONTARIO

Har-Tech Electronics Ltd
390 Bradwick Dr #3 and #4
Concord, Ontario, Canada L4K 2W4
PHONE 905-660-3419
FAX 905-660-5102

Har-Tech Electronics Ltd
One Bonner St
Nepean, Ontario, Canada K2H 7S9
PHONE 613-726-9410
FAX 613-726-8834

QUEBEC

Har-Tech Electronics Ltd
6600 Trans-Canada Hwy #460
Pointe Claire, Quebec, Canada H9R 4S2
PHONE 514-694-6110
FAX 514-694-8501

United States Distributors

ALABAMA

Insight Electronics Inc
4835 University Square #19
Huntsville, AL 35816
PHONE 205-830-1222
FAX 205-830-1225

Marshall Industries
3313 Memorial Pkwy South
Huntsville, AL 35801
PHONE 205-881-9235
FAX 205-881-1490

Nu Horizons
4801 University Square #11
Huntsville, AL 35816
PHONE 205-722-9330
FAX 205-722-9348

ARIZONA

Insight Electronics Inc
1515 W. University #103
Tempe, AZ 85281
PHONE 602-829-1800
FAX 602-967-2658

Marshall Industries
9830 S. 51st St #C107-109
Phoenix, AZ 85044
PHONE 602-496-0290
FAX 602-893-9029

CALIFORNIA

Insight Electronics Inc
2 Venture Plaza #340
Irvine, CA 92718
PHONE 714-727-3291
FAX 714-727-1804

Insight Electronics Inc
9980 Huennekens St
San Diego, CA 92121
PHONE 619-587-1100
FAX 619-587-1380

Insight Electronics Inc
1295 Oakmead Parkway
Sunnyvale, CA 94086
PHONE 408-720-9222
FAX 408-720-8390

Insight Electronics Inc
4333 Park Terrance Dr #101
Westlake Village, CA 91361
PHONE 818-707-2101
FAX 818-707-0321

Marshall Industries
9320 Telstar Ave
El Monte, CA 91731-3004
PHONE 818-307-6000
FAX 818-307-6297

Marshall Industries
One Morgan
Irvine, CA 92718-1994
PHONE 714-458-5395
FAX 714-581-5255

Marshall Industries
336 Los Coches St
Milpitas, CA 95035
PHONE 408-942-4600
FAX 408-262-1224

Marshall Industries
5961 Kearny Villa
San Diego, CA 92123
PHONE 619-627-4140
FAX 619-627-4163

Marshall Industries
3039 Kilgore Ave #140
Rancho Cordova, CA 95670
PHONE 916-635-9700
FAX 916-635-6044

Marshall Industries
26637 W. Agoura Rd
Calabasas, CA 91302
PHONE 818-876-7000
FAX 818-880-6846

United States Distributors — Contd.

CALIFORNIA — Contd.

Zeus Electronics
6 Cromwell St #100
Irvine, CA 92718
PHONE 714-581-4622
FAX 714-454-4355

Zeus Electronics
6276 San Ingacio Ave #E
San Jose, CA 95119
PHONE 408-629-4789
FAX 408-629-4792

COLORADO

Insight Electronics
384 Inverness Dr S. #105
Englewood, CO 80112
PHONE 303-649-1800
FAX 303-649-1818

Marshall Industries
12351 N Grant
Thornton, CO 80241
PHONE 303-451-8383
FAX 303-457-2899

CONNECTICUT

Marshall Industries
20 Sterling Dr
Wallingford, CT 06492-0200
PHONE 203-265-3822
FAX 203-284-9285

FLORIDA

Insight Electronics Inc
17757 U.S. 19 North #520
Clearwater, FL 34624
PHONE 813-532-8850
FAX 813-532-4252

Insight Electronics Inc
621 NW 53rd St #240
Boca Raton, FL 33487
PHONE 407-995-1486
FAX 407-995-1487

Insight Electronics Inc
600 Northlake Blvd #250
Altamonte Springs, FL 32701
PHONE 407-834-6310
FAX 407-834-6461

Marshall Industries
2840 Scherer Dr #410
St. Petersburg, FL 33716
PHONE 813-573-1399
FAX 813-573-0069

Marshall Industries
2700 W. Cypress Creek Rd #D114
Ft. Lauderdale, FL 33309
PHONE 305-977-4880
FAX 305-977-4887

Marshall Industries
380-S Northlake Blvd #1024
Altamonte Springs, FL 32701-5260
PHONE 407-767-8585
FAX 407-767-8676

Nu Horizons
600-S Northlake Blvd #270
Altamonte Springs, FL 32701
PHONE 407-831-8008
FAX 407-831-8862

Nu Horizons
3421 NW 55th St
Ft. Lauderdale, FL 33309
PHONE 305-735-2555
FAX 305-735-2880

United States Distributors — Contd.

FLORIDA — Contd.

Zeus Electronics
37 Skyline Dr Bldg D #1301
Lake Mary, FL 32746
PHONE 407-333-3055
FAX 407-333-9681

GEORGIA

Insight Electronics Inc
3005 Breckinridge Blvd #210-A
Duluth, GA 30136
PHONE 404-717-8566
FAX 404-717-8588

Marshall Industries
5300 Oakbrook Pkwy #140
Norcross, GA 30093-9990
PHONE 404-923-5750
FAX 404-923-2743

Nu Horizons
5555 Oakbrook Pkwy #340
Norcross, GA 30093
PHONE 404-416-8666
FAX 404-416-9060

ILLINOIS

Insight Electronics
1365 Wiley Rd #142
Schaumburg, IL 60173
PHONE 708-885-9700
FAX 708-885-9701

Marshall Industries
50 E. Commerce Unit 1
Schaumburg, IL 60173
PHONE 708-490-0155
FAX 708-490-0569

INDIANA

Marshall Industries
6990 Corporate Dr
Indianapolis, IN 46278
PHONE 317-297-0483
FAX 317-297-2787

KANSAS

Marshall Industries
10413 W. 84th Terrace
Lenexa, KS 66214
PHONE 913-492-3121
FAX 913-492-6205

MARYLAND

Insight Electronics
9101 Guilford Rd
Columbia, MD 20146
PHONE 301-490-8080
FAX 301-490-8081

Marshall Industries
2221 Broadbirch Dr #G
Silver Springs, MD 20904
PHONE 301-622-1118
FAX 301-622-0451

Nu Horizons
8975 Guilford Rd #120
Columbia, MD 21046
PHONE 410-995-6330
FAX 410-995-6332

MASSACHUSETTS

Gerber Electronics
128 Carnegie Row
Norwood, MA 02062
PHONE 617-769-6000
FAX 617-762-8931

Insight Electronics
55 Cambridge St #301
Burlington, MA 01803
PHONE 617-270-9400
FAX 617-270-3279

Marshall Industries
33 Upton Dr
Wilmington, MA 01887
PHONE 508-658-0810
FAX 508-657-5931

United States Distributors — Contd.

MASSACHUSETTS — Contd.

Nu Horizons
107 Audubon Rd Bldg 1
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Insight Electronics Inc
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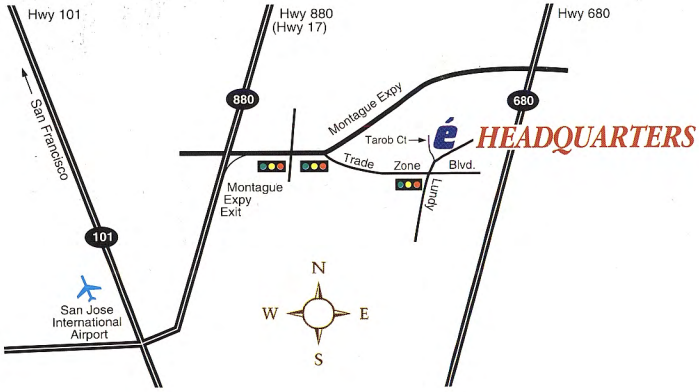

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